



REALTEK

ALC5686-CG
ALC5686-CGT

High Performance USB I/F
Audio CODEC

Datasheet

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USING THIS DOCUMENT

This document is intended for the hardware and software engineer’s general information on the Realtek ALC5686 Audio Codec IC.

Though every effort has been made to ensure that this document is current and accurate, more information may have become available subsequent to the production of this guide. In that event, please contact your Realtek representative for additional information that may help in the development process.

REVISION HISTORY

Revision	Release Date	Summary
0.10	2019/2/25	Preliminary version release.

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1. General Description

The ALC5686 is a highly-integrated USB audio solution which is specifically designed for high-end USB type-C headset/headphone and other USB-to-3.5mm jack audio applications. The ALC5686 mainly combines USB 2.0/ADC 3.0 digital audio interface, I²S/I²C interfaces, embedded flash for saving more PCB size, and stereo Hi-Fi quality headphone amplifiers. The ALC5686 features a stereo low power cap-free Class-G headphone amplifier with 124dB SNR and 95dB THD+N performance, providing longer battery life and Hi-Fi listening experiences.

In terms of audio jack detection features, the embedded Jack detection function can automatically detect whether the accessory is a headset (4 segments) or a headphone (3 segments) and plug-in/plug-out status. Meanwhile, the build-in global headset function can automatically sense and support both OMTP and CTIA headset pinouts with automatic switch for microphone and ground signals. On top of that, the ALC5686 features auto impedance sense function which can recognize the jack impedance into 9 sections from 0Ohm to >50kOhm load, distinguishing between the headset and line-in. Besides, using 3-button, 4-button, or even multi-button headsets are also detected and fully supported through the ALC5686. All the features shown above meet the latest Google Wired Audio Headset Specification. These features make ALC5686 also a best solution for USBC to 3.5mm jack audio adapter.

Besides, ALC5686 integrates high efficient DC-DC buck converter for power of the system with wide input voltage, 3.0V~5.0V. The buck converter will automatically switch between PWM and PFM modes while chip operating with different power loading for better efficiency.

2. System Applications

- USB or USB Type-C handset & headphone
- USB or USB Type-C audio accessory

3. Features

- USB 2.0 interface for the audio codec
 - ◆ Support USB FS and HS Mode
 - ◆ USB audio input / output interface
 - Support PCM streams on USB
 - Non-crystal design
 - Support full-speed and high-speed transfer mode
 - Support UAC1.0/2.0 and ADC3.0 with LPM/L1 feature
 - External flash supported
 - Audio data supports up to 32-bits data length and 8k~384k sampling rate
- Ultra low power consumption when jack unplug on USB to 3.5mm dongle application
 - VBUS < 100uA
- Embedded 256kB flash memory
- Master I²S interface
 - ◆ Only support master mode
 - ◆ Support 48kHz sample rate
 - ◆ Support 16/20/24/32-bits data length
- Master I²C interface
 - ◆ Up to 2MHz clock rate
- Embedded DC to DC step down type switching regulator
 - ◆ Input voltage range: 3.0V ~ 5.5V
 - ◆ Output voltage: 1.8V~2.0V (Configurable)
 - ◆ Efficiency
 - > 80% at 100uA output current
 - Maximum efficiency up to 85%
 - ◆ Driving current: 200mA
 - ◆ Low output voltage ripple

■ Stereo Class-G headphone output

- ◆ SNR = 124dBA (32ohm, 30mW reference signal, 20~20KHz)
- ◆ DNR = 113dBA (Input=-60dBFS, 32ohm, 30mW reference signal, 20~20KHz)
- ◆ THD+N = -95dB (32ohm, 20mW, 20~20KHz)
- ◆ FSOV = 1Vrms
- ◆ Crosstalk < -100dB (32/600 Ohm, 20~20kHz)
- ◆ Impedance sensing
 - Support multi-step impedance sense (0 ~ 8ohm / 9 ~ 23ohm / 23 ~ 41ohm / 23 ~ 41ohm / 42 ~ 75ohm / 76 ~ 150ohm / 151 ~ 450ohm / 451 ~ 1Kohm / 1K ~ 5Kohm / 5K ~ 50Kohm / > 50Kohm)
- ◆ De-pop function
 - DC offset < 100uV
 - Smart hot USB unplug detection for avoiding headphone pop noise

■ One analog microphone input

- ◆ One analog input port for recording on the microphone of CTIA or OMTP type headset
 - Single-ended analog microphone inputs with boost pre-amplifiers and low noise microphone bias
 - SNR = 99dBA (MIC input to ADC with 0dB gain, Vref=0.5Vrms, 20 ~ 20kHz)
 - THD+N = -90dB (MIC input to ADC with 0dB gain, Vref=0.5Vrms, 20 ~ 20kHz)
 - AMIC input to ADC with 50dB boost, SNR>66dBA, THD+N<-65dB
 - Microphone boost gain range: 0/13/20/30/35/40/44/50/52dB

■ Two jack detection (JD) pins

- ◆ JD pin to support high voltage threshold ($V_{th}=0.9*V_{BAT}$)
- ◆ Low power consumption JD pins to support wake-up function

■ Headset/headphone detection and ground auto switch

- ◆ In-line command detection. Support headset (4 segment) /headphone (3 segment) detection, jack insert and remove detection
- ◆ Feedback compensation for headphone crosstalk issue
- ◆ CTIA/OMTP/TRS type detection

■ MICBIAS1/2

- ◆ Multi-outputs MICBIAS: 2.7V/2.4V/2.25V/1.8V
- ◆ Low noise design for better recoding quality

- Crystal Oscillator
 - ◆ Optional clock source
 - ◆ Support external clock source input
- Headset multi-buttons detection
 - ◆ Programmable threshold for high precision button detection
 - ◆ Support Google 4 buttons detection
- Parametric 12 bands (6+6 bands) equalizer shared for playback or record path
 - ◆ 6 bands (1*1st LPF + 1*1st HPF + 3*2nd BPF + 1*Biquad Filter)
- Sidetone function
- PWM Generator for LED dimming control
- Others:
 - ◆ Zero detection and soft volume for pop noise suppression
 - ◆ Power management and enhanced power saving
- QFN48 (Size=6.5mm*5mm, Pitch=0.4mm) package

4. Function Block

4.1. Function Block

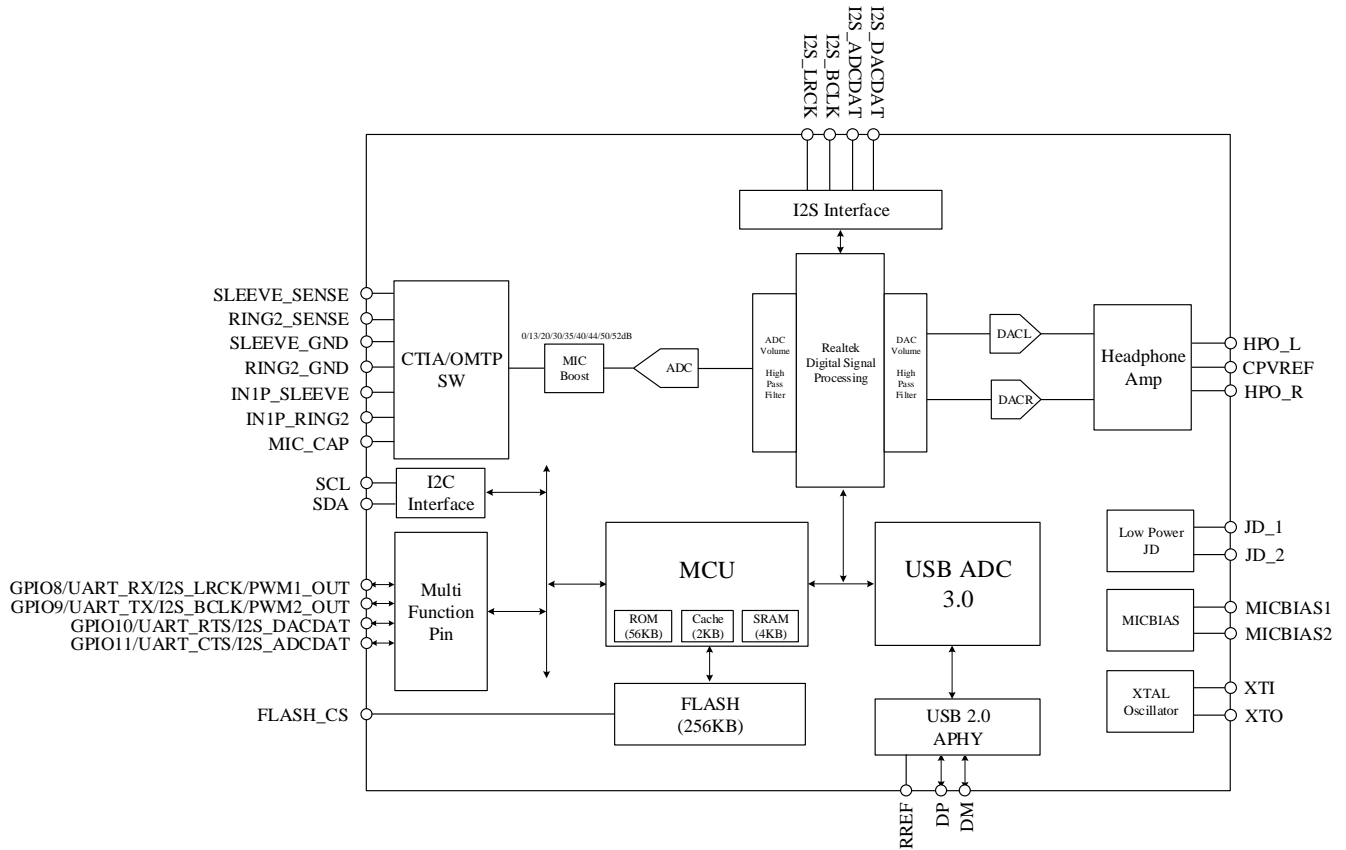


Figure 1. Function Block

4.2. Power Block

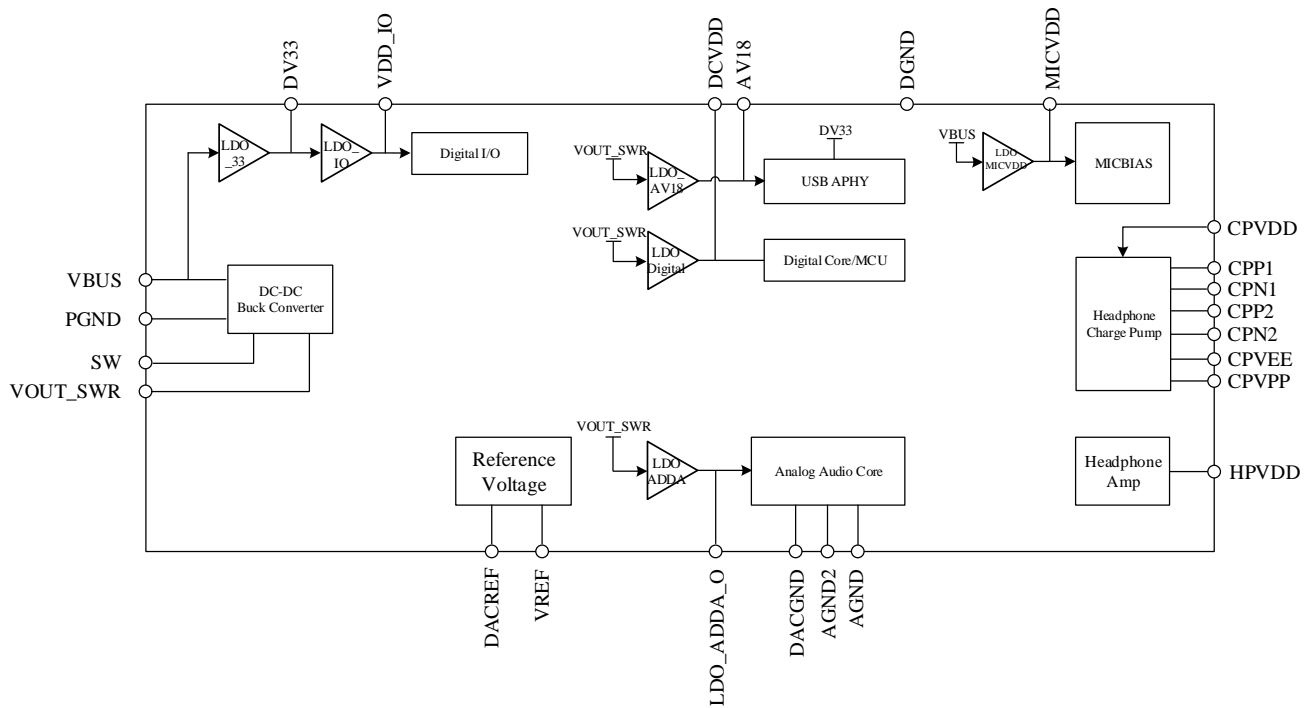


Figure 2. Power Block

4.3. Analog Audio Mixer Path

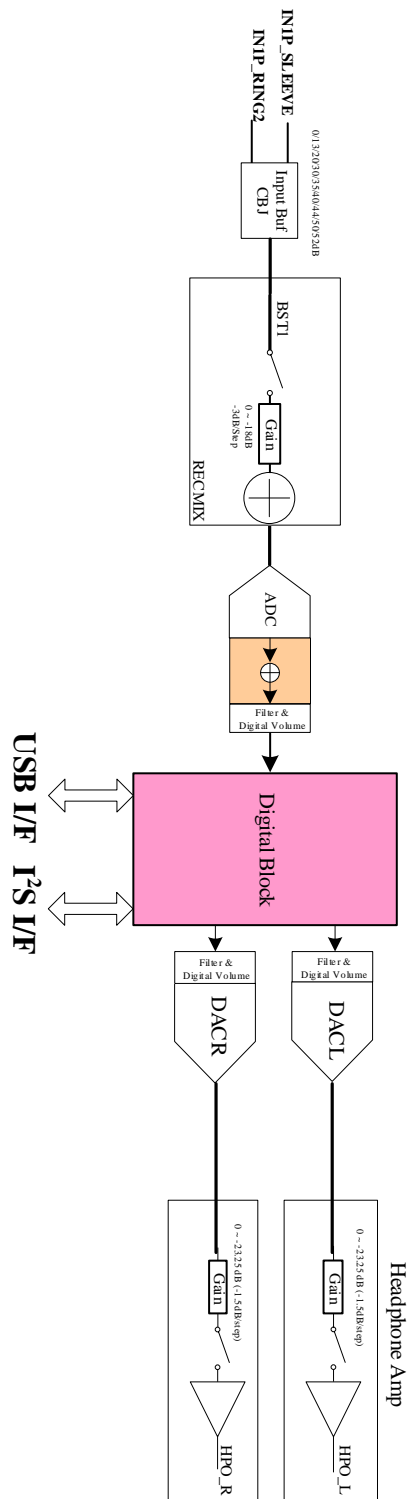


Figure 3. Analog Mixer Path

The diagram illustrates the internal architecture of the ADC module. At the top, the **USB 2.0 Controller** is connected to the **USB Bus** and the **UAC IN** and **UAC OUT** Endpoints. The **UAC IN** Endpoint is connected to the **UAC1 DAC Selection** block, which routes signals to **UAC1 DAC 0** and **UAC1 DAC 1**. The **UAC1 DAC Selection** block also receives signals from **UAC1 DAC 0** and **UAC1 DAC 1**. The **UAC1 DAC 0** and **UAC1 DAC 1** are connected to the **ADC** module via a multiplexer. The **ADC** module includes a **USB 2.0 Controller** and a **USB Bus** interface. The **ADC** module also includes a **UAC1 DAC Selection** block, which routes signals to **UAC1 DAC 0** and **UAC1 DAC 1**. The **UAC1 DAC 0** and **UAC1 DAC 1** are connected to the **ADC** module via a multiplexer. The **ADC** module also includes a **USB 2.0 Controller** and a **USB Bus** interface.

Figure 4. Digital Mixer Path

5. Pin Assignment

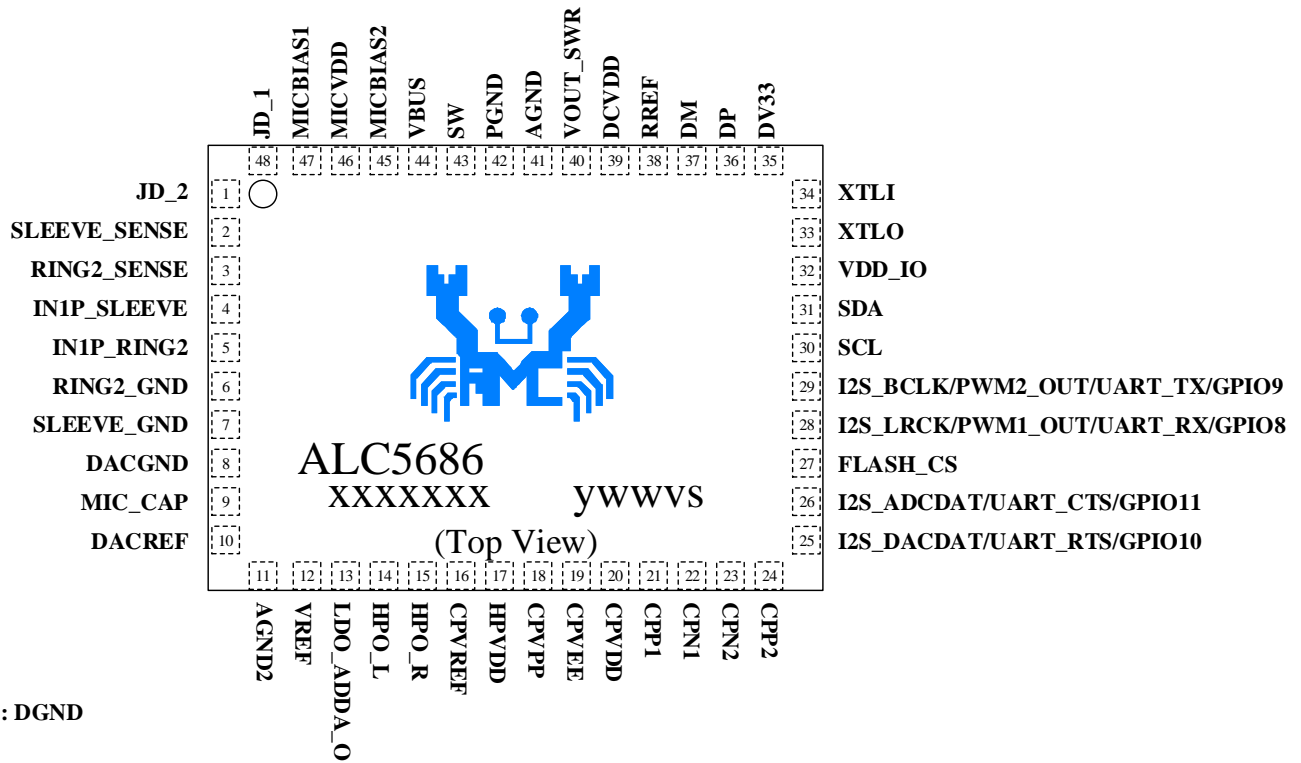


Figure 5. QFN48 Pin Assignment

6. Pin Description

6.1. Digital I/O Pins

Table 1. Digital I/O Pins

Name	Type	Pin	Description	Characteristic Definition
DP	I/O	36	USB data plus	Differential type signal Default state: weakly pull-low Full Speed mode: 120MHz High Speed mode: 480MHz
DM	I/O	37	USB data minus	Differential type signal Default state: weakly pull-low Full Speed mode: 120MHz High Speed mode: 480MHz
SCL	I/O	30	Master I ² C Serial Clock	Open Drain
SDA	I/O	31	Master I ² C Serial Data	Open Drain
I2S_LRCK/PWM1_OUT/UART_RX/GPIO8	I/O	28	I ² S interface synchronous signal PWN Generator UART receiver data GPIO function	Output: $V_{OL}=0.1*VDD_IO$, $V_{OH}=0.9*VDD_IO$ Input: Schmitt trigger $V_{IL}=0.35*VDD_IO$ $V_{IH}=0.65*VDD_IO$ Default Status: Output Type
I2S_BCLK/PWM2_OUT/UART_TX/GPIO9	I/O	29	I ² S interface serial bit clock PWN Generator UART transmitter data GPIO function	Output: $V_{OL}=0.1*VDD_IO$, $V_{OH}=0.9*VDD_IO$ Input: Schmitt trigger $V_{IL}=0.35*VDD_IO$ $V_{IH}=0.65*VDD_IO$ Default Status: Output Type
I2S_DACDAT/UART_RTS/GPIO10	I	25	I ² S interface serial data input UART request to send GPIO function	Output: $V_{OL}=0.1*VDD_IO$, $V_{OH}=0.9*VDD_IO$ Input: Schmitt trigger $V_{IL}=0.35*VDD_IO$ $V_{IH}=0.65*VDD_IO$ Default Status: Input Type (Floating)
I2S_ADCDAT/UART_CTS/GPIO11	O	26	I ² S interface serial data output UART clear to send GPIO function	Output: $V_{OL}=0.1*VDD_IO$, $V_{OH}=0.9*VDD_IO$ Input: Schmitt trigger $V_{IL}=0.35*VDD_IO$ $V_{IH}=0.65*VDD_IO$ Default Status: Output Type
FLASH_CS	I	27	Flash chip selection	Pull high 100k to VDD_IO

6.2. Analog I/O Pins

Table 2. Analog I/O Pins

Name	Type	Pin	Description	Characteristic Definition
MICBIAS1	O	47	Microphone bias output	3mA driving current
MICBIAS2	O	45	Microphone bias output	3mA driving current
JD_1	I	48	Jack detection pin	$V_{th}=0.9*VBUS$
JD_2	I	1	Jack detection pin	$V_{th}=0.9*VBUS$
HPO_L	O	14	Headphone output left channel	Analog output
HPO_R	O	15	Headphone output right channel	Analog output
IN1P_SLEEVE	I	4	Analog microphone input for combo jack mode	Analog input
IN1P_RING2	I	5	Analog microphone input for combo jack mode	Analog input
XLTI	I	34	XTAL Input	Analog input
XLTO	O	33	XTAL Output	Analog output

6.3. Filter/Reference/Not Connected Pins

Table 3. Reference Pins

Name	Type	Pin	Description	Characteristic Definition
RREF	R	38	External reference for USB function	6.25KOhm resistor with 1% precision is required
CPVREF	R	16	Headphone amplifier feedback reference	
SLEEVE_SENSE	R	2	Headphone amplifier feedback reference for combo jack mode	
RING2_SENSE	R	3	Headphone amplifier feedback reference for combo jack mode	
SLEEVE_GND	R	7	Reference ground for combo jack mode	
RING2_GND	R	6	Reference ground for combo jack mode	
MIC_CAP	R	9	Analog microphone input reference for combo jack mode	
SW	R	43	DC-DC Buck converter feedback signal	
VREF	R	12	Analog I/O reference	
DACREF	R	10	Analog DAC reference	
CPP1	R	21	Charge pump bucket capacitor pin	
CPN1	R	22	Charge pump bucket capacitor pin	
CPP2	R	24	Charge pump bucket capacitor pin	
CPN2	R	23	Charge pump bucket capacitor pin	

6.4. Power & Ground Pins

Table 4. Power/GND Pins

Name	Type	Pin	Description	Characteristic Definition
VBUS	P	44	USB Type-C VBUS power	Supply range: 3.0V ~ 5.5V
VOUT_SWR	P	40	DC-DC Buck converter output	1.8V ~ 2.0V
LDO_ADDA_O	P	13	Analog power	1.6V ~ 1.98V
HPVDD	P	17	Headphone amplifier power	1.71V ~ 1.98V
CPVDD	P	20	Charge pump power	1.71V ~ 1.98V
CPVPP	P	18	Charge pump positivity voltage output	
CPVEE	P	19	Charge pump negative voltage output	
MICVDD	P	46	MICBIAS power	3.0V ~ 5.0V
DCVDD	P	39	Digital core power	1.6V ~ 1.98V
VDD_IO	P	32	Digital IO power	1.8V ~ 3.3V
DV33	P	35	3.3V LDO output	3.3V
PGND	G	42	DC-DC Buck converter ground	
DACGND	G	8	Analog DAC ground	
AGND	G	41	Analog ground	
AGND2	G	11	Analog ground	
EPAD	G	49	Digital ground	

7. Function Description

7.1. System Connection

7.1.1. USB Type-C Headset

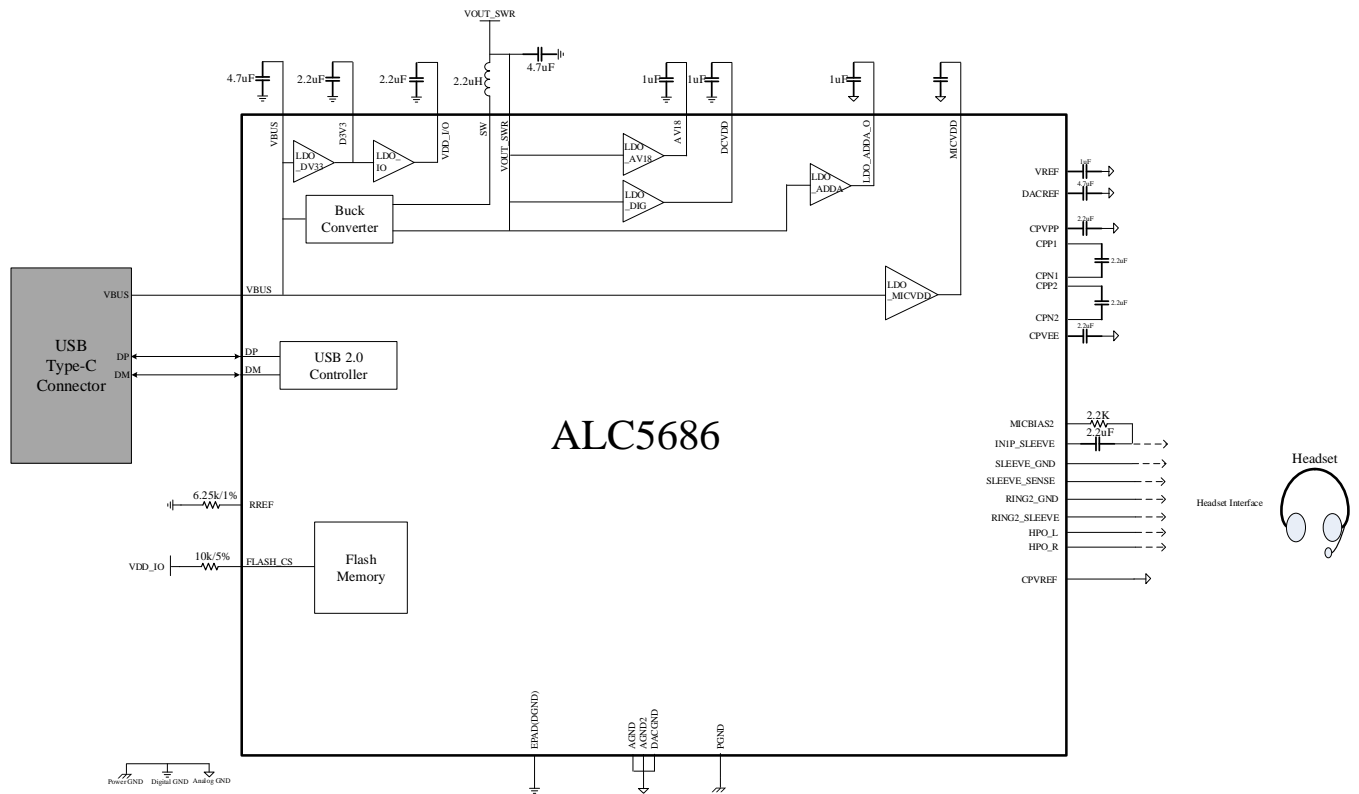


Figure 6. System Connection of USB Type-C Headset

8. Electrical Characteristics

8.1. Absolute Maximum Ratings

Table 5. Absolute Maximum Ratings

Parameter	Symbol	Min	Typ	Max	Units
Power Supplies USB Power	VBAT	-0.3	-	7 ¹	V
Operating Ambient Temperature	Ta	-25	-	+85	°C
Storage Temperature	Ts	-55	-	+125	°C
ESD Protection Human Body Model (HBM)	All Pins Pass +/-3500V				

Note:

1. VBUS =5V with 3.5% duty cycle power bouncing up to 7V is acceptable.
2. VBUS is the power source of the whole chip's power rail.

8.2. Power/Ground Recommended Operating Conditions

Table 6. Power/Ground Operaton Conditions

Power Type	Description	MIN	TYP	MAX	Unit
VBUS	USB VBUS Power	3.0	5.0	5.5	V
The below power rails could be supplied internally.					
VOUT_SWR ^②	DC-DC Buck Converter Output	1.8	1.9	2.0	V
MICVDD ^①	MICBIAS Power	3.0	3.3	5.5	V
VDD_IO ^①	Digital I/O Power	1.71	1.8/3.3	3.6	V
DV33 ^①	USB Power	3.0	3.3	3.6	V
DCVDD ^①	Digital Core Power	1.6	1.8	1.9	V
LDO_ADDA_O ^①	Analog Core Power	1.71	1.8	1.9	V
CPVDD ^②	Charge Pump Power	1.71	1.8	1.9	V
HPVDD ^①	HP Amplifier Power	1.71	1.8	1.9	V
DGND	Digital Ground		0		V
AGND/AGND2/DACGND	Analog Ground		0		V
PGND	Buck Converter Power Ground		0		V

① These power pins could be supplied by internal LDO.

② These power pins could be supplied by internal DC-DC Buck.

8.3. Static Characteristics

Table 7. Static Characteristics

Parameter	Symbol	Min	Typ	Max	Units
Input Voltage Range	V_{IN}	-0.30	-	$V_{DD_IO}+0.30$	V
Low Level Input Voltage	V_{IL}	-	-	$0.35 \cdot V_{DD_IO}$	V
High Level Input Voltage	V_{IH}	$0.65 \cdot V_{DD_IO}$	-	-	V
High Level Output Voltage	V_{OH}	$0.9 \cdot V_{DD_IO}$	-	-	V
Low Level Output Voltage	V_{OL}	-	-	$0.1 \cdot V_{DD_IO}$	V
Output Buffer High Drive Current	-	0.6	4	8	mA
Output Buffer Low Drive Current	-	0.7	4	8	mA
Input Buffer Pull-Up Resistor	-	55	110	270	$K\Omega$
Input Buffer Pull-Down Resistor	-	63	130	300	$K\Omega$

8.4. Analog Performance Characteristics

Table 8. Analog Performance Characteristics

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
DAC to Headphone Output (Loading = 32 Ohm)						
Full Swing Output Voltage	FSOV	Digital Input=0dBFS	-	0.94	-	Vrms
Signal to Noise Ratio	SNR	A-Weighting Reference: FSOV	-	124	-	dBrA
Dynamic Range	DNR	A-Weighting Reference: FSOV Input=-60dBFS,	-	113	-	dBrA
Total Harmonic Distortion Plus Noise	THD+N	Po=20mW	-	-94	-	dB
		Po=10mW	-	-94	-	dB
Crosstalk	Xtalk	Po=20mW	-	-100	-	dB
Output Noise Floor	N	A-Weighting	-	580	-	nV
Power Supply Rejection Ratio (CPVDD, AVDD)	PSRR	100mVrms 217Hz~4kHz	60	-	78	dB
DAC to Headphone Output (Loading = 16 Ohm)						
Full Swing Output Voltage	FSOV	Digital Input=0dBFS	-	0.9	-	Vrms
Signal to Noise Ratio	SNR	A-Weighting Reference: FSOV	-	124	-	dBrA
Dynamic Range	DNR	A-Weighting Reference: FSOV Input=-60dBFS,	-	113	-	dBrA
Total Harmonic Distortion Plus Noise	THD+N	Po=30mW	-	-92	-	dB
		Po=20mW	-	-92	-	dB
Crosstalk	Xtalk	Po=20mW	-	-90	-	dB
Output Noise Floor	N	A-Weighting	-	580	-	nV
Power Supply Rejection Ratio (CPVDD, AVDD)	PSRR	100mVrms 217Hz~4kHz	60	-	78	dB
DAC to Headphone Output (Loading = 10k Ohm)						
Full Swing Output Voltage	FSOV	Digital Input=0dBFS	-	0.94	-	Vrms
Signal to Noise Ratio	SNR	A-Weighting Reference: FSOV	-	124	-	dBrA
Dynamic Range	DNR	A-Weighting Reference: FSOV Input=-60dBFS,	-	113	-	dBrA
Total Harmonic Distortion Plus Noise	THD+N	Digital Input=0dBFS	-	-95	-	dB
Crosstalk	Xtalk	Output=1Vrms	-	-100	-	dB
Output Noise Floor	N	A-Weighting	-	580	-	nV
Power Supply Rejection Ratio (CPVDD, AVDD)	PSRR	100mVrms 217Hz~4kHz	60	-	78	dB

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Mic Input to ADC (Single Mode)						
Maximum Input Voltage	FSIV	Digital Input=0dBFS	-	550	-	Vrms
Signal to Noise Ratio	SNR	A-Weighting Reference: FSIV BST Gain=0dB	-	98	-	dBrA
		A-Weighting Reference: FSIV BST Gain=20dB	-	90	-	dBrA
		A-Weighting Reference: FSIV BST Gain=30dB	-	81	-	dBrA
		A-Weighting Reference: FSIV BST Gain=40dB	-	72	-	dBrA
Total Harmonic Distortion Plus Noise	THD+N	-	87	90	93	dB
Power Supply Rejection Ratio (AVDD)	PSRR	100mVrms 217Hz~4kHz	-	70	-	dB

Note: Standard test conditions:

$T_{ambient}=25^{\circ}\text{C}$

$V_{BUS}=5\text{V}$

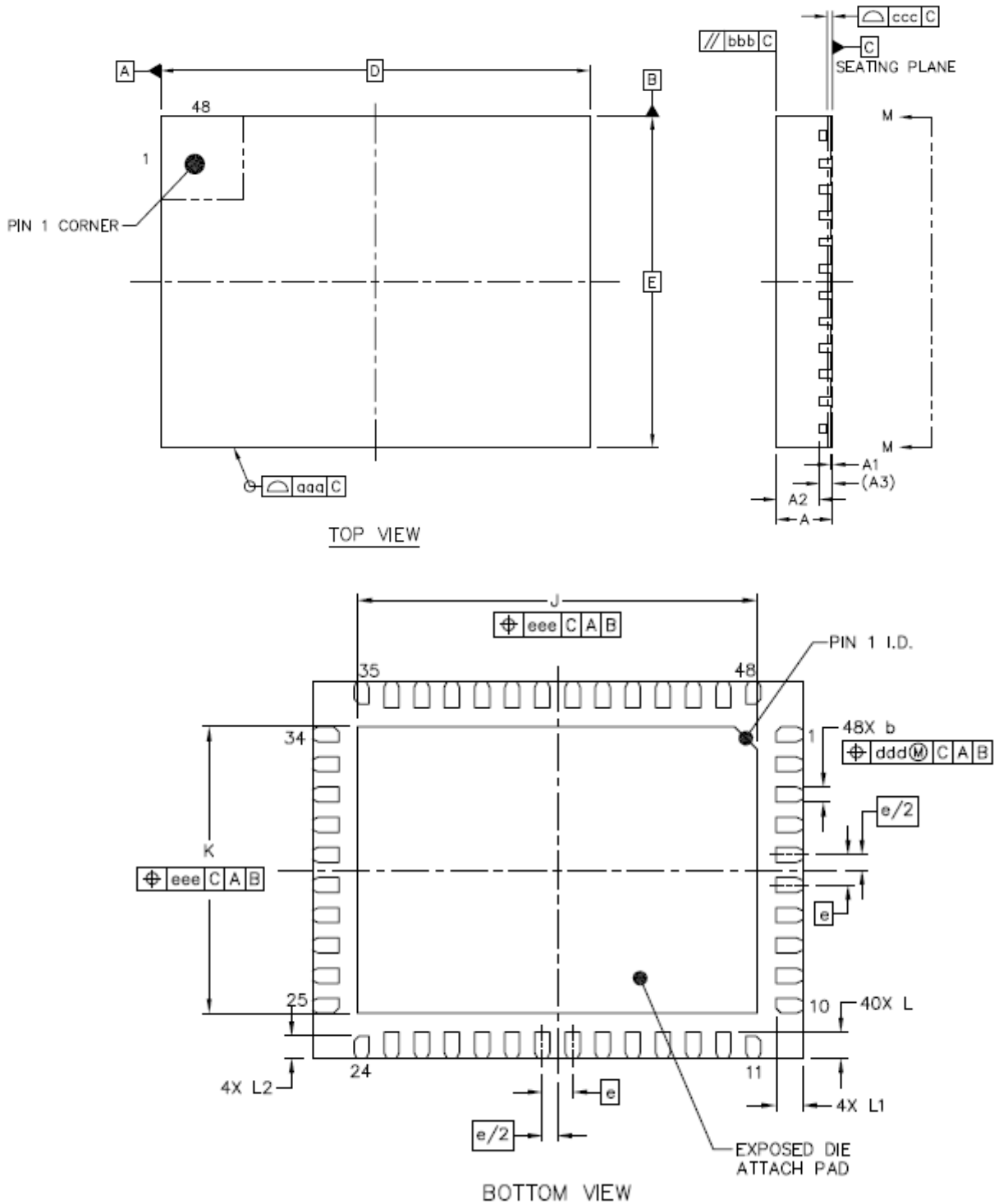
1kHz input sine wave; 24Bits Data Length PCM Sampling frequency=48kHz; Test bench Characterization BW:

10Hz~22kHz, 0dB attenuation

dBA: with A-Weighting

9. Package Information

9.1. Mechanical Dimensions



		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	0.8	0.85	0.9
STAND OFF		A1	0	0.035	0.05
MOLD THICKNESS		A2	---	0.65	---
L/F THICKNESS		A3	0.203 REF		
LEAD WIDTH		b	0.15	0.2	0.25
BODY SIZE	X	D	6.5 BSC		
	Y	E	5 BSC		
LEAD PITCH		e	0.4 BSC		
EP SIZE	X	J	5.2	5.3	5.4
	Y	K	3.7	3.8	3.9
LEAD LENGTH		L	0.3	0.35	0.4
		L1	0.25	0.35	0.4
		L2	0.2	0.3	0.35
PACKAGE EDGE TOLERANCE		aaa	0.1		
MOLD FLATNESS		bbb	0.1		
COPLANARITY		ccc	0.08		
LEAD OFFSET		ddd	0.1		
EXPOSED PAD OFFSET		eee	0.1		

Figure 8. Package Dimension