POWER-SWITCHING CONVERTERS

Second Edition

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Preface to the Second Edition

In this second edition, Dr. Simon Ang welcomes co-author, Dr. Alejandro Oliva of the Universidad Nacional del Sur, Argentina. Much new material and many references have been added. Several chapters have been completely revised, and two new chapters on interleaved converters and switched capacitor converters have been added. The discrete-time modeling method has been included in the dynamic analysis of switching converters. Design case studies have been replaced with new cases.

This book is intended to be used as a textbook for a senior-level electrical engineering course on switching converters. The introductory course would cover the basic switching converter topologies described in Chapters 1 to 4, followed by an introduction to basic control techniques presented in Chapter 5. The instructor may choose to skip to Chapters 7 and 8 on interleaved converters and switching capacitor converters, respectively.

Chapter 6 covers the closed-loop control and stability considerations in the design of switching converters. It discusses the dynamic analysis of switching converters based on state–space averaging and linearization. This chapter is divided into two parts. The first part covers continuous-time

models and control techniques, while the second part introduces discrete-time models based on sampled-data modeling. Many of the topics presented in this chapter can be skipped and covered later in a more advanced level course.

Chapter 9 provides tools for the simulation of switching converters. It introduces both PSpice and MATLAB simulations of switching converters. This chapter may be partially taught after Chapter 2 and concurrently with Chapters 4 to 6. The discussion of switching converters is not complete until a switching converter is analyzed, designed, and finally prototyped. Chapter 10 contains complete design examples, including experimental designs, which may be used as technical reference or for a class project.

Supplementary information and material, updated periodically, are available on the download page at *http://www.crcpress.com*. These include class slides, selected PSpice examples, and MATLAB scripts. The PSpice examples are designed to run on the OrCAD 10.0 demo software.

Several individuals have contributed to this second edition of *Power-Switching Converters* by providing assistance, suggestions, and criticisms. We appreciate the collaboration of Dr. Juan Carlos Balda for his detailed and constructive criticism, which improve the accuracy and content of Chapter 6. We would like to thank Dr. Roberto M. Schupbach for his thorough reading and error detection in the MATLAB code. Graciela Rodríguez (Mrs. Oliva) gave up her vacations to offer invaluable help with the figures and equations. Several design case studies in Chapter 10 were adapted from the class projects of our former graduate students at the University of Arkansas, in particular, those of Kien Truong and Lan Phuong Bui Pham. We gratefully acknowledge Claudio Frate for preparing most of the figures in the text. Finally, we like to sincerely express our gratitude to our families for their support and love.

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Editors

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1

Introduction to Switching Converters

1.1 INTRODUCTION

A switching converter or switch-mode power converter is a power electronic system, which converts one level of electrical energy into another level of electrical energy at the load, by switching action. Switching converters have been in existence since the 1950s. However, the unavailability of reliable and low-cost power switching transistors had limited their usage primarily to the military and space applications. The advances and availability of modern power semiconductor devices in the early 1970s have made the switching converter a popular choice in power supplies. In DC–DC switching converter circuits, semiconductor switches control the dynamic transfer of power, from the input direct current (DC) source to the load, by connecting the source to the load for some predetermined duration. These switching converters find applications in high-efficiency power supplies and DC motor drives. In comparison to linear voltage converters, or linear voltage regulators, switching power supplies have higher energy efficiency and a higher power packing density. New and

improved power semiconductor devices such as power MOSFETs and insulated-gate bipolar transistors (IGBTs), integrated magnetics, newer topologies, and VLSI pulse-width-modulating integrated circuits, which pack more control and supervisory features in a smaller volume, have contributed to the increased power packing density of switching converters.

1.2 INDUSTRY TRENDS

Over the past few years, the DC–DC switching converter technology has undergone tremendous changes. The required supply voltage for many integrated circuits and their associated electronic systems decreases from the historic 5 V standard to less than 1.5 V. At the same time, the load current levels have simultaneously risen to levels that would have been unimaginable just a few years ago. Some electronic systems are now requiring 2.5 V at 60 A, 1.8 V at 60 A or 1 V at 100 A from the power supply. In the near future, supply voltages for some microprocessors will move towards 0.5 V and currents up to 400 A are expected. A normal dynamic requirement for a DC–DC switching converter is to provide a peak output voltage in response to a load transient of 75–100–75 A at a slew rate of 100 A/μsec with only 60 mV of deviation. At the same time, the converter should recover to within $\pm 1.5\%$ of output voltage in less than 4 μsec. These requirements are making it very difficult to deliver high current, low voltage power from a centralized power supply. Designers are now increasingly turning to distributed power supply architectures to provide lower voltages at high currents from a DC–DC converter to power today's complex loads.

A distributed power system generates a high-voltage DC bus (e.g., 48 V) and distributes this voltage at a lower current around the electronics system to the various loads. Near each load, one or more modular DC–DC switching converters convert the bus voltage to a low-voltage source (e.g., 1 V) needed by the load circuitry. Besides reducing the voltage, the modular DC–DC switching converter also provides electrical isolation and increased load transient performance. Distributed power systems eliminate the mechanical and cost problems of the thick copper buses required in a centralized power supply system. The lower voltage draws a larger current and has less tolerance for deviations in its voltage [1].

In 1999, the measure for *high density* was 25 W/in.^{3} at 5 V. By 2001, this had increased to 40 W/in.^{3} at 3.3 V. Nowadays, power densities of greater than 50 W/in.^{3} are achievable, while high-power density is considered to be around 90 W/in.^{3} The continuing evolution in magnetic components and its integration with passives has played a key role in increasing the power

density without sacrificing performance [2]. A dramatic increase in converter efficiency and power density was accomplished by synchronous rectification, especially for low-voltage converters. The combination of synchronous rectifiers and interleaving techniques led to commercial converters that can achieve efficiencies higher than 92%, while efficiencies of 85% are routinely obtainable [1].

Interleaving (or multiphase) converters offer several advantages over a single power stage, including lower current ripple on the input and output capacitors, faster transient response to load changes, and improved power handling capabilities at greater than 90% power efficiency. Commercial controllers can operate each phase at a switching frequency in the MHz range, resulting in effective size reduction [3]. The new generation of switching converter controllers is based on DSP technology to implement the digital control, monitoring, and communication functions into a single DSP chip, simplifying designs and resulting in a considerable part count reduction. This simplified design allows for the control of multiple power supply products with a single control architecture, which is customized for each power supply through software. The computational power of the DSP can be used to achieve higher efficiencies, by implementing soft-switching techniques, such as zero-voltage switching (ZVS) and zero-current switching (ZCS). In addition, more efficient topologies that take advantage of advanced nonlinear digital control techniques may be used to obtain optimum performance over the complete operating range of the power supply [4].

1.3 LINEAR CONVERTER

There are two types of linear converters or voltage regulators: series and shunt. They differ only in the way that their output voltage is regulated.

1.3.1 Linear Series-Pass Regulator

The series-pass regulator shown in Figure 1.1 is essentially an electrically variable resistance in the form of a transistor operating in its linear mode in series with the output load.

An error amplifier senses the DC output voltage across a sampling resistor network R_1 and R_2 and compares it with a reference voltage V_{ref}. The error amplifier output voltage drives the base of the series-pass NPN transistor via a current amplifier. The output voltage is regulated by modulating the base-drive of the series-pass NPN transistor. An increase in the sampling voltage across R_2 decreases the base drive of the series-pass

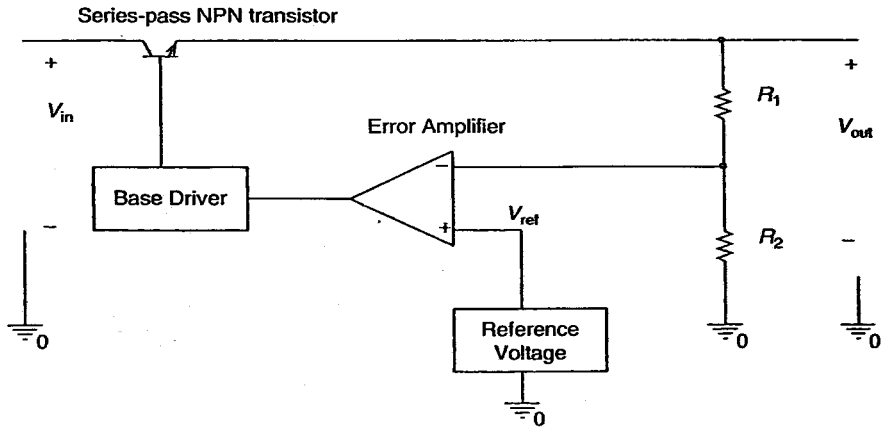

Figure 1.1 Series-pass voltage regulator.

transistor such that a smaller current is delivered to the output and hence, the output voltage drops. The regulated output voltage, V_{out}, is

$$V_{out} = V_{ref}\left(1 + \frac{R_1}{R_2}\right). \tag{1.1}$$

This is the relationship of a noninverting operational amplifier circuit, assuming that the series-pass transistor is ideal. A change in the input voltage results in a change in the equivalent resistance R_s of the series-pass transistor. The product of this resistance and the load current, I_{load}, creates a changing differential voltage, V_{diff}, which compensates for a changing input voltage ΔV_{in}. The output voltage can be expressed as

$$V_{out} = V_{in} - V_{diff}, \tag{1.2}$$

and

$$V_{diff} = I_{load}R_s, \tag{1.3}$$

or

$$V_{out} = V_{in} - I_{load}R_s. \tag{1.4}$$

Thus, for a changing input voltage

$$\Delta R_s = \frac{\Delta V_{in}}{I_{load}}, \tag{1.5}$$

assuming that V_{out} and V_{in} are fixed, and for a changing load current

$$\Delta R_s = \frac{-R_s \Delta I_{load}}{I_{load}}. \tag{1.6}$$

Any change in the input voltage will essentially be absorbed across the series-pass transistor. The stability of the output voltage is mainly determined by the gain of the open-loop feedback amplifier. A series-pass regulator provides a simple and inexpensive way to obtain a source of regulated voltage. However, it can only provide a lower regulated voltage than its input source voltage. Even though its output voltage always has one DC common with the input voltage, frequently DC isolation between input and output is required. The major drawback of the series-pass regulator is the excessive power dissipation in the series-pass transistor in high-current applications. The power dissipated across the collector–emitter junction of the series-pass transistor is

$$P_{diss} = (V_{in} - V_{out})I_{load}. \tag{1.7}$$

It is evident that as the input voltage increases for a constant regulated output voltage, the power dissipated in the series-pass transistor increases. The efficiency of this regulator, disregarding any fluctuations of the input and output voltages, is

$$\eta = \frac{P_{out}}{P_{in}} = \frac{V_{out}I_{load}}{V_{in}I_{load}} = \frac{V_{out}}{V_{in}}. \tag{1.8}$$

This is plotted in Figure 1.2 for a 5-V regulator and assuming a "drop-out" voltage of 2.5 V. The "drop-out" voltage is the minimum magnitude of input voltage above the regulated output voltage required for voltage regulation. Low drop-out (0.5 to 1 V) regulators are usually designed with a PNP series-pass transistor. As can be seen, the maximum efficiency of a 5-V series-pass regulator is about 67%. The efficiency drops as the input voltage increases. It is only 42% with a 12-V input voltage. It is evident that its efficiency increases with increasing output voltage.

1.3.2 Linear Shunt Regulator

The shunt regulator employs a shunt element that varies its shunt current requirement to account for varying input voltages or changing load conditions. A basic shunt regulator is shown in Figure 1.3.

The output voltage of the shunt regulator is given by

$$V_{out} = V_{in} - (I_{load} + I_s)R_s, \tag{1.9}$$

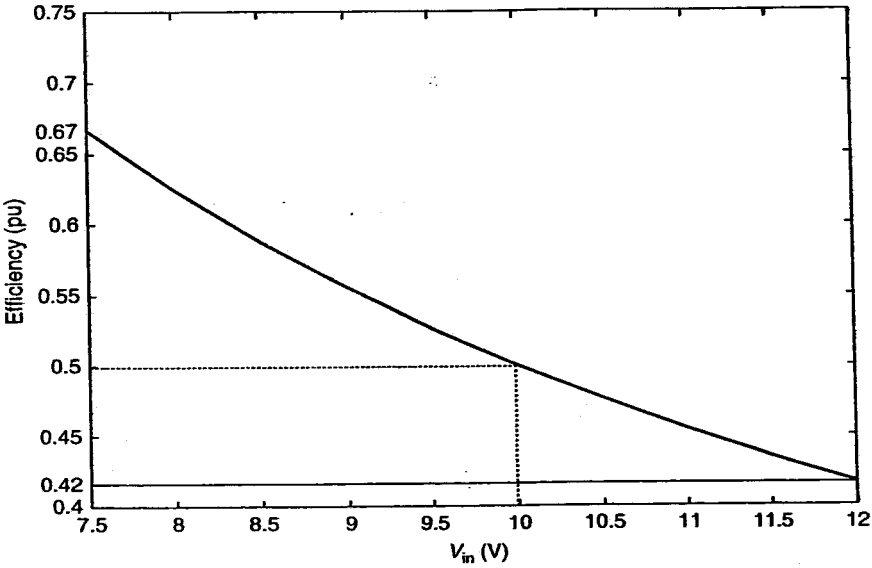

Figure 1.2 Efficiency versus input voltage for a 5-V series-pass regulator with a drop-out voltage of 2.5 V.

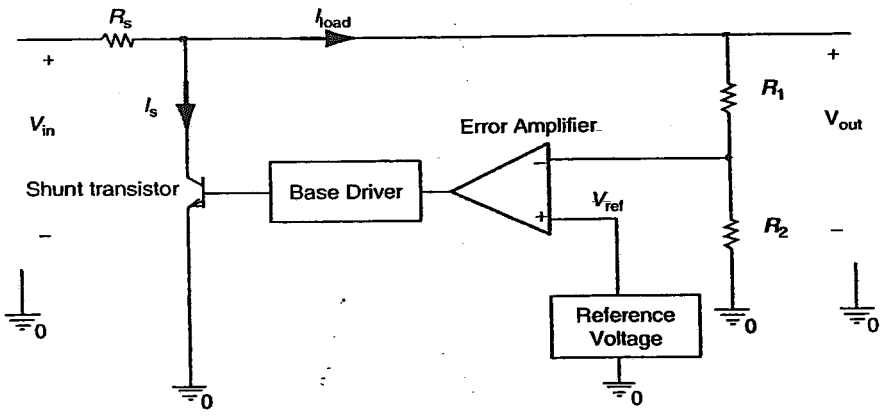

Figure 1.3 Shunt voltage regulator.

where I_s is the shunt current. The shunt regulator is less sensitive to input voltage transients, therefore, it does not reflect load current transients back to the source, and it is inherently short-circuit proof. The efficiency of the linear shunt regulator is

$$\eta = \frac{V_{out} I_{load}}{V_{in}(I_{load} + I_s)} = \frac{I_{load}}{I_{load} + I_s} - \frac{I_{load} R_s}{V_{in}}. \tag{1.10}$$

As can be seen, the efficiency of the linear shunt regulator decreases with increasing R_s due to larger power dissipation in R_s. The efficiency also decreases with increasing shunt current, I_s. In general, the efficiency of the shunt regulator is smaller than that of the series-pass regulator.

Despite many drawbacks, linear voltage regulators such as the 1.5-A, 5-V UA7805CKC series regulator and TL431CP shunt regulator are commercially available at relatively low costs. They are most cost effective for low-power applications. However, power dissipation becomes a major problem for applications above an output current of about 5 A.

1.4 SWITCHING CONVERTERS

A simple DC–DC switching converter circuit consists of two semiconductor switches (usually one switching transistor and one switching diode), one inductor, and one capacitor, as shown in Figure 1.4. The arrangement of these switches and storage elements defines the topology of the switching converter. In the case that the load is a direct-current motor, the DC–DC switching converter is commonly known as a chopper or a DC motor drive system. The principal merits of the switching converter are its high conversion efficiency and its high power packing density, which result in significant weight reduction. However, switching converters often require complex control circuits, and noise or electromagnetic interference (EMI) filters. An input line filter is often required in some applications.

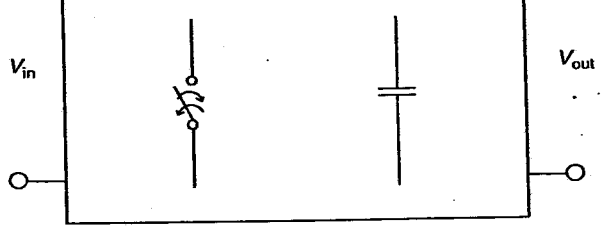

Figure 1.4 Basic switching converter components.

1.4.1 Basic Switching Converter with Resistive Load

The fundamental concept of the switching converter can be understood from the simple switching circuit shown in Figure 1.5(a). The switch opens and closes for durations of DT and $(1-D)T$, respectively. D, the duty cycle, is the ratio of the on-time t_{on} to the switching period T, viz.,

$$D = \frac{t_{on}}{T} = t_{on} f_s, \tag{1.11}$$

where f_s is the switching frequency.

During the interval DT, the load resistor is connected to the input power source V_s. However, the load resistor is disconnected from the input power source during the interval $(1-D)T$. The resulting voltage across the load resistor $v_{out}(t)$ is a chopped version of the input power source V_s as shown in Figure 1.5(b). The average output voltage V_a is given by

$$V_a = \frac{1}{T}\int_0^{DT} V_s dt = \frac{V_s DT}{T} = DV_s. \tag{1.12}$$

Thus, the average output voltage is proportional to the duty cycle D. When the duty cycle is one, the output voltage will be the same as the input voltage. In this case, there is no switching action and the switch is closed at all times. The average load current I_a is found from Ohm's law:

$$I_a = \frac{V_a}{R_L} = \frac{DV_s}{R_L}. \tag{1.13}$$

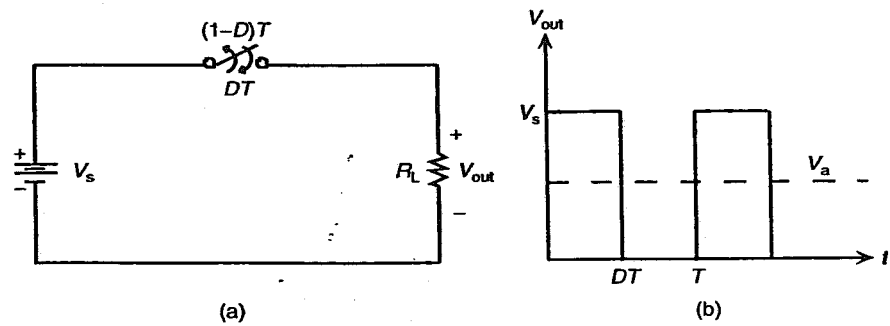

Figure 1.5 (a) Fundamental switching converter circuit. (b) Voltage waveform across output resistor, R_L.

The root-mean-square value of the output voltage is

$$V_{\text{out,rms}} = \sqrt{\frac{1}{T}\int_0^{DT} V_s^2 \mathrm{d}t} = V_s\sqrt{D}. \tag{1.14}$$

The average input power of this switching converter, assuming a V_{ce} drop across the switching transistor, is simply

$$P_{\text{in}} = \frac{1}{T}\int_0^{t_{on}} V_s i_a \mathrm{d}t = \frac{1}{T}\int_0^{t_{on}} \frac{V_s(V_s - V_{ce})}{R_L}\mathrm{d}t = \frac{V_s(V_s - V_{ce})t_{on}}{R_L T}. \tag{1.15}$$

The output power P_o is

$$P_o = \frac{1}{T}\int_0^{t_{on}} \frac{(V_s - V_{ce})^2}{R_L}\mathrm{d}t = \frac{t_{on}}{T}\frac{(V_s - V_{ce})^2}{R_L}. \tag{1.16}$$

Thus, the conversion efficiency is

$$\eta = \frac{P_o}{P_{\text{in}}} = \frac{V_s - V_{ce}}{V_s}. \tag{1.17}$$

As can be seen from Equation (1.17), the conversion efficiency increases with increasing input voltage, V_s. This is in contrast to the series-pass linear converter.

The output voltage can also be expressed in terms of a Fourier series as

$$V_{\text{out}}(t) = a_0 + \sum_{n=1}^{\infty} a_n \cos(2\pi n f_s t) + \sum_{n=1}^{\infty} b_n \sin(2\pi n f_s t), \tag{1.18}$$

where a_0 is the average value

$$a_n = \frac{1}{\pi}\int_0^{2\pi} f(t)\cos(2\pi n f_s t)\mathrm{d}(wt) \tag{1.19}$$

and

$$b_n = \frac{1}{\pi}\int_0^{2\pi} f(t)\sin(2\pi n f_s t)\mathrm{d}(wt). \tag{1.20}$$

Now consider the case $D = 0.5$; the cosine terms are zero since the voltage waveform is an odd function and the Fourier series reduces to

$$V_{out}(t) = DV_s + \sum_{n=1}^{\infty} \frac{V_s[1 - \cos(2Dn\pi)]\sin(2\pi n f_s t)}{n\pi}. \tag{1.21}$$

The first term in Equation (1.21) (i.e., DV_s) is the average, or DC value, of the output voltage. The magnitude of the fundamental component (f_s) of the output voltage is calculated as

$$V_{0,1} = \frac{V_s(1 - \cos\pi)}{\pi} = 0.637\,V_s, \tag{1.22}$$

or 63.7% of the input source voltage V_s. Similarly, the third harmonic ($3f_s$) is $0.21\,V_s$ or 21% of V_s. Figure 1.6 shows the harmonic spectrum of the output voltage of the fundamental switching converter with a 50% duty cycle. Since the current waveform follows the voltage waveform, the harmonic content is similar to the voltage waveform except that it is divided by the load resistance. The discontinuous input source current contributes to EMI. There is no practical application for this simple switching converter (except for resistive heating) due to the high harmonic contents of its output voltage. A typical switching converter would have a low-pass filter between the

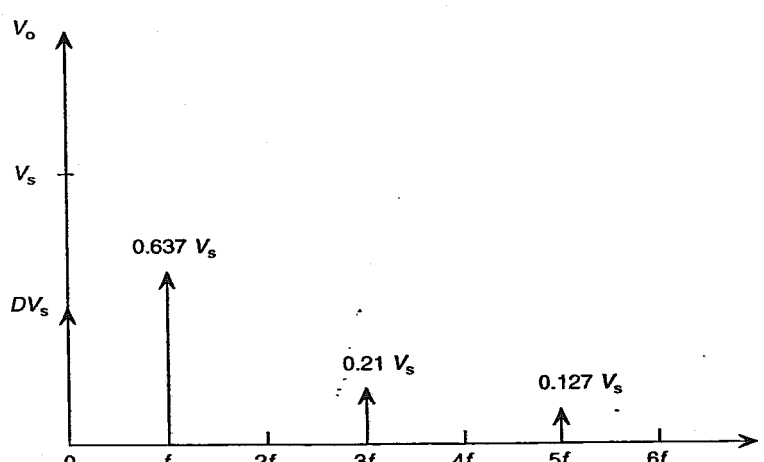

Figure 1.6 Harmonic spectrum of the output voltage for the fundamental switching converter.

switch and the load to filter out the frequency components starting at f_s and keeping only the DC component.

1.4.2 Basic Switching Converter with R_L Load

With an R_L load such as a DC motor and the addition of a second switch as shown in Figure 1.7 the current waveform flowing through the load can be made to be continuous. The second switch is necessary since the inductor current cannot be interrupted abruptly without causing high-voltage spikes.

The operation of this switching converter can be divided into two modes: S_1 on/S_2 off (mode 1) for $0<t<t_{on}$ and S_1 off/S_2 on (mode 2) for $t_{on}<t<T$. The equivalent circuit for mode 1 and the voltage across the R_L load are shown in Figure 1.8(a) and (b), respectively.

During mode 1, current flows from the input source V_s to the R_L load. Using Kirchoff's voltage law,

$$V_s = Ri_1(t) + L\frac{di_1(t)}{dt} + V_{emf}, \tag{1.23}$$

where V_{emf} is the back emf of the DC motor. The current $i_1(t)$ during this mode of operation can be solved using the Laplace transformation assuming that the initial current is I_1, i.e., $i_1(t=0)=I_1$. Taking the Laplace transformation of Equation (1.23) with the initial condition of I_1, we have

$$\frac{V_s}{s} = RI_1(s) + L[sI_1(s) - I_1] + \frac{V_{emf}}{s}. \tag{1.24}$$

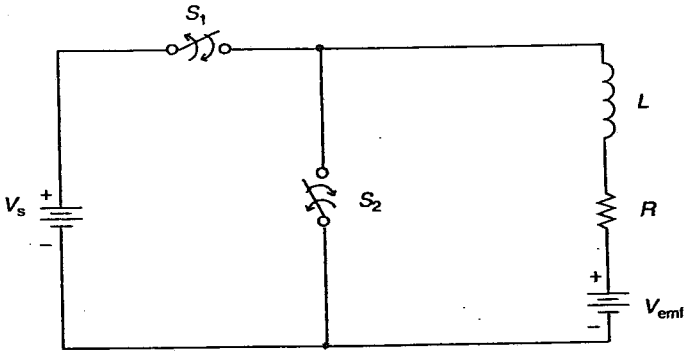

Figure 1.7 Simple switching converter with an R_L load.

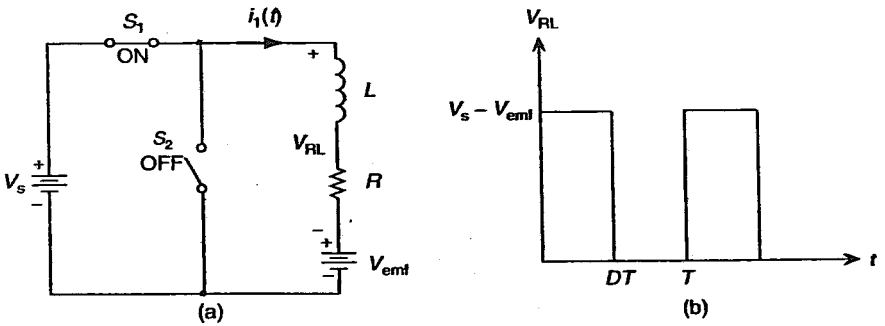

Figure 1.8 (a) Equivalent circuit for mode 1 with S_1 on/S_2 off. (b) Voltage waveform across the R_L load.

Solving for $I_1(s)$:

$$I_1(s) = \frac{(V_s - V_{emf})}{R}\left(\frac{1}{s} - \frac{1}{s + (R/L)}\right) + \frac{I_1}{s + (R/L)}. \tag{1.25}$$

Taking the inverse Laplace transform, the current $i_1(t)$ becomes

$$i_1(t) = \frac{(V_s - V_{emf})\left(1 - e^{-t\frac{R}{L}}\right)}{R} + I_1 e^{-t\frac{R}{L}} \tag{1.26}$$

for $0<t<t_{on}$. During mode 2, S_1 is switched off while S_2 is switched on. The equivalent circuit is shown in Figure 1.9(a). The load current, $i_2(t)$, continues to flow through S_2. From the Kirchoff's voltage law,

$$0 = Ri_2(t) + L\frac{di_2}{dt} + V_{emf}. \tag{1.27}$$

Assuming an initial current of i_2 and solving Equation (1.27), the current $i_2(t)$ is

$$i_2(t) = I_2 e^{-t\frac{R}{L}} - \frac{V_{emf}}{R}(1 - e^{-t\frac{R}{L}}). \tag{1.28}$$

For a large inductance value compared to the resistance value, or a large time constant (L/R), $i_2(t)$ decreases linearly. Hence, the current waveforms for $i_1(t)$ and $i_2(t)$ are almost linear as shown in Figure 1.9(b). Equations (1.26) and (1.28) are valid only for continuous current flow in the inductor. The load currents $i_1(t)$ and $i_2(t)$ would be continuous if the time constant, L/R is much greater than the switching period, T. This means that the switching frequency, f_s, of the switching converter must be much larger than R/L.

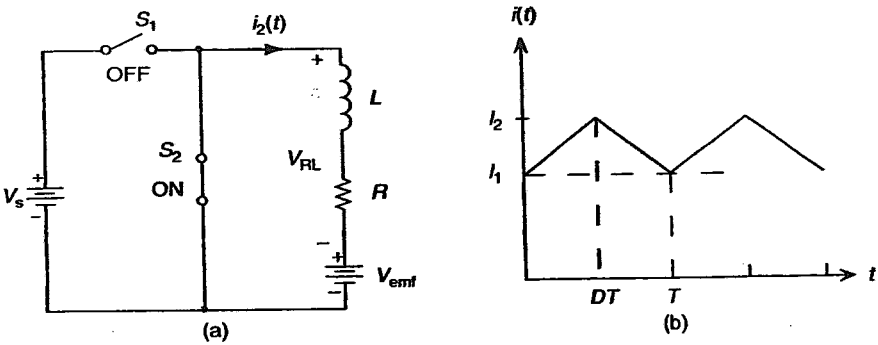

Figure 1.9 Equivalent circuit for mode 2 with S_1 off/S_2 on. (b) Current waveform through the *RL* load.

1.5 PRINCIPLES OF STEADY-STATE CONVERTER ANALYSIS

If the duty cycle D is held constant at a fixed switching frequency over a large enough number of switching cycles; for example, n cycles, then the current and voltage waveforms would reach a point where they would start repeating every T seconds. This means that the current and voltage waveforms become periodic, with period T; or $i((n+1)T) = i(nT)$ and $v((n+1)T) = v(nT)$. This condition is known as the steady state. There are two very important principles that describe the steady-state operation of switching converters: the *volt–second balance*–on the inductor and the *charge balance* on the capacitor. These two properties will be used throughout the book to analyze the steady-state operation of various switching converters.

1.5.1 Inductor Volt–Second Balance

The steady-state condition imposes a periodic behavior of the current flowing through the inductor; thus,

$$i_L(nT) = i_L((n+1)T). \tag{1.29}$$

Also,

$$v_L = L\frac{di_L}{dt}. \tag{1.30}$$

Integration over one switching period yields:

$$i_L((n+1)T) - i_L(nT) = \frac{1}{L}\int_{nT}^{(n+1)T} v_L(t)\mathrm{d}t \tag{1.31}$$

Since the left-hand side of Equation (1.31) is zero, then the right-hand side must be zero too, i.e.,

$$0 = \int_{nT}^{(n+1)T} v_L(t)\mathrm{d}t. \tag{1.32}$$

Equation (1.32) states that the integral of the voltage across the inductor along a switching period must be zero for the steady state. The integral has units of volts–second; giving the name of volt–second balance to this property. An intuitive analysis shows that if the integral of the voltage across the inductor along a switching period would not be zero, then the current amplitude would continuously increase.

1.5.2 Capacitor Charge Balance

A similar analysis can be applied to the capacitor. The equation defining the relationship between the voltage across and the current flowing through a capacitor is:

$$i_c(t) = c\frac{\mathrm{d}v_c(t)}{\mathrm{d}t}. \tag{1.33}$$

The integration of this equation over one switching period yields:

$$v_c((n+1)T) - v_c(nT) = \frac{1}{c}\int_{nT}^{(n+1)T} i_c(t)\mathrm{d}t. \tag{1.34}$$

Since the left-hand side of Equation (1.34) is zero, then the right-hand side must also be zero; i.e.,

$$0 = \int_{nT}^{(n+1)T} i_c(t)\mathrm{d}t. \tag{1.35}$$

Equation (1.35) states that the integral of the current flowing through the capacitor along a switching period must be zero for the steady state. The

integral has units of Ampere–second; giving the name of Amp–second balance (or charge balance) to this property. An intuitive analysis shows that if the integral of the current flowing through the capacitor (or the accumulated charge) over a switching period would not be zero, then its voltage amplitude would continuously increase.

PROBLEMS

1.1. A linear shunt regulator shown in Figure 1.3 has an input supply of 12 V. The load requirements are a constant 5-V supply to some logic circuitry at a current of 0.5 A. As an engineer, you are required to select the appropriate R_s value, given that the shunt current, I_s, is 10% of the load current, I_L. Determine the efficiency of the shunt regulator, neglecting the power dissipation across the sampling resistors R_1 and R_2. What effects do the choice of R_s have on the efficiency?

1.2. The fundamental switching converter shown in Figure 1.7 has a resistance value of 1 Ω and an inductance of 1 H, $V_s = 3.72$ V, and a $V_{ref} = 0$ V. During the interval of $0 < t \leq 1$ sec, S_1 is on and S_2 is off. S_1 is off and S_2 is on during the interval of $1 \leq t < 2$ sec. The current flowing through the inductor at the beginning of the switching cycle is 1 A. Determine the peak-to-peak ripple current in the inductor during the first switching cycle. Draw and label the waveforms for the current flowing through the inductor and the voltage across the resistor.

1.3. The fundamental switching converter of Figure 1.5 converter has a resistive load of 10 Ω and an input voltage of 48 V. The switching frequency is 1 kHz with a duty cycle of 50%. The semiconductor switch has a voltage drop of 1 V in its on-state. (a) Determine the average output voltage and the rms output voltage of this switching converter. (b) Using Fourier series, express the output voltage in terms of their fundamental component and the next two higher harmonics. Find the rms value of the fundamental component of the output voltage.

1.4. Determine the duty cycle for the maximum ripple current to occur in a fundamental switching converter shown in Figure 1.7 with an R_L load. Also determine the maximum ripple current for this converter.

1.5. For the converter of Problem 2, draw the voltage across the inductor and calculate its integral along a switching period.

1.6. Repeat Problem 2 for $D = 0.25$.

1.7. Consider a power converter that has reached the steady state. (a) Show that the average power absorbed by the inductor in one switching cycle is zero. (b) Show that the average power absorbed by the capacitor in one switching cycle is zero.

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2

Basic Switching Converter Topologies

2.1 INTRODUCTION

The word *topology* refers to the science of place. The topological properties of a circuit are those invariant with stretching, squeezing, bending, or twisting of the circuit graph. Two networks are topologically equivalent if they differ only in the circuit elements that make up their branches [1]. The switching converter consists of a number of storage elements and switches which are connected in a topology such that the periodic switching actions of the switches control the dynamic transfer of power from the input to the output to produce a desired DC conversion at the output. The storage elements (inductor and capacitor), in general, have to be connected in such a way that they form a low-pass filter to yield a low output ripple voltage. The two fundamental topologies of switching converters are the buck converter and the boost converter. Most of the other topologies are either buck-derived or boost-derived converters since they are the topological equivalent to the buck or the boost converter. The buck–boost converter is a unique cascade combination of the buck and boost converters that results in output voltage

inversion. The forward converter and the push–pull converter are examples of buck-derived switching converters. Flyback and Cûk switching converters are derived from the buck–boost converter. The resonant converter employs a resonating inductor–capacitor (LC) tank circuit to shape the voltage or current waveform of its switching transistor from the typical rectangular pulses into a sinusoidal waveform. Other topologies, such as the single-ended primary inductance converter (SEPIC), are a derivative of the Cûk converter.

The analyses of the buck, boost, buck–boost, Cûk, and resonant switching converters are performed in steady-state. *Steady-state* signifies that the duty cycle D is held constant at a fixed switching frequency over a sequence of switching cycles; for example, n cycles. This leads to the current and voltage periodicity requirements of $i(0) = i(nT)$ and $v(0) = v(nT)$, where n is the number of switching cycles during steady-state operation. It is important to realize that switching converters are inherently nonlinear electronic systems due to their switching actions. The linearization and state–space averaging technique for the small-signal analysis of the switching converter is presented in Chapter 6.

2.2 BUCK CONVERTER

The basic buck converter using a power MOSFET is shown in Figure 2.1. In a buck converter, the average output voltage V_a is lower than its input voltage, V_s. The operation of the buck converter can be divided into two modes, depending on the switching actions of its switching transistor. According to the continuity of the current flowing through the output inductor, the buck converter can be operating either in the continuous mode or in the discontinuous mode.

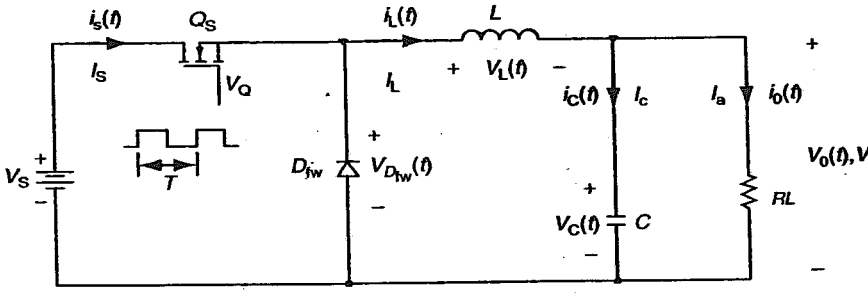

Figure 2.1 Circuit schematic of a buck converter.

2.2.1 Continuous Mode

Mode 1 ($0 < t \leq t_{on}$)

At the beginning of a switching cycle (at $t = 0$) during mode 1, the switching transistor Q_s is switched on. The equivalent circuit for mode 1 is shown in Figure 2.2. Since the input voltage (V_s) is greater than the average output voltage V_a, the current in the inductor $i_L(t)$ ramps upward during this interval. The voltage across the inductor L is related to the rate of rise of its current and is given by:

$$v_L(t) = L\frac{di}{dt}. \tag{2.1}$$

For a large inductance value, the inductor current $i_L(t)$ rises linearly from I_1 to I_2 during t_{on}, therefore,

$$V_s - V_a = L\frac{I_2 - I_1}{t_{on}} = L\frac{\Delta I}{t_{on}}, \tag{2.2}$$

and the duration of mode 1 is

$$t_{on} = \frac{L\Delta I}{(V_s - V_a)}. \tag{2.3}$$

Thus, mode 1 is characterized by the storage of energy in the magnetic field of the inductor.

Mode 2 ($t_{on} \leq t < T$)

Mode 2 begins when the switching transistor Q_s is switched off at $t = t_{on}$. Its equivalent circuit is shown in Figure 2.3.

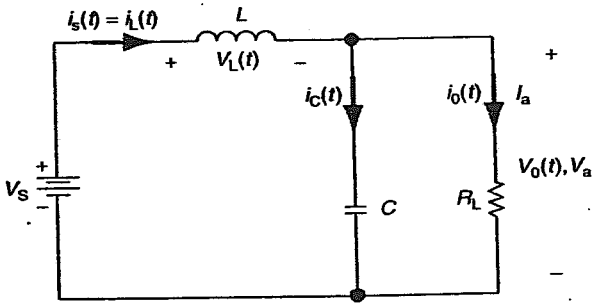

Figure 2.2 Mode 1 equivalent circuit for the buck converter ($0 < t \leq t_{on}$).

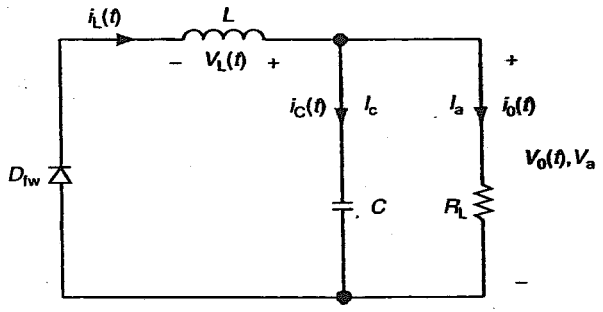

Figure 2.3 Mode 2 equivalent circuit for the buck converter ($t_{on} < t \leq T$).

Since it is not possible to change the current flowing through the inductor instantaneously, the voltage polarity across the inductor immediately reverses trying to maintain the same current I_2, which had been flowing just prior to switching off of the switching transistor Q_s. This phenomenon is called *inductive kick*. The freewheeling diode D_{fw} conducts since it is forward-biased just as the inductor voltage reverses its polarity. A high-negative voltage spike would appear at the source of the switching transistor Q_s if it were not for the presence of D_{fw}. The inductor current falls, as the energy stored in it is transferred to the capacitor and expended by the load. The voltage across the inductor $v_L(t)$ is now $-V_a$ and its current falls linearly from I_2 to I_1 in time t_{off},

$$-V_a = L\frac{I_1 - I_2}{t_{off}}, \tag{2.4}$$

or

$$V_a = L\frac{\Delta I}{t_{off}}. \tag{2.5}$$

The duration of mode 2 is

$$t_{off} = \frac{L\Delta I}{V_a}, \tag{2.6}$$

and the peak-to-peak current ripple in the inductor is

$$\Delta I = \frac{V_a t_{off}}{L}. \tag{2.7}$$

The peak-to-peak current ripple in the inductor, ΔI, is the same during $0 < t \leq t_{on}$ and $t_{on} \leq t < T$ for steady-state operation,

$$\Delta I = \frac{(V_s - V_a)t_{on}}{L} = \frac{V_a t_{off}}{L}. \tag{2.8}$$

Substituting $t_{on} = DT$ and $t_{off} = (1 - D)T$ into Equation (2.8) gives

$$(V_s - V_a)DT = V_a(1 - D)T \tag{2.9}$$

or

$$V_a = \frac{V_s DT}{T} = V_s D. \tag{2.10}$$

The average output voltage V_a of the buck converter is the product of the duty cycle D and the input voltage V_s. The duty cycle of a *voltage regulator* implemented with a buck converter is periodically changing in order to maintain a constant average output voltage V_a during a load change or an input voltage fluctuation. This periodic change in the duty cycle is accomplished using a negative feedback scheme with pulse-width modulation discussed in Chapter 5. The on time t_{on} and off time t_{off} are defined as

$$t_{on} = \frac{L\Delta I}{V_s - V_a}; \quad t_{off} = \frac{L\Delta I}{V_a}. \tag{2.11}$$

The switching period T is the sum of t_{on} and t_{off}:

$$T = \frac{1}{f_s} = t_{on} + t_{off} \tag{2.12}$$

$$T = \frac{L\Delta I}{V_s - V_a} + \frac{L\Delta I}{V_a} = \frac{LV_s\Delta I}{V_a(V_s - V_a)}. \tag{2.13}$$

The current ripple in the inductor, ΔI, can then be expressed as

$$\Delta I = \frac{V_a(V_s - V_a)T}{LV_s} = \frac{DV_s(1 - D)}{f_s L}. \tag{2.14}$$

Thus, the peak-to-peak current ripple in the inductor is inversely proportional to its inductance value and switching frequency f_s. Using Kirchoff's current law, the inductor current is

$$i_L = i_c + i_0. \tag{2.15}$$

The average capacitor current I_c is zero for a switching period since the output capacitor is charged and discharged by the same amount during steady-state operation. The average inductor current I_L is equal to the average output current I_a, then charging of the output capacitor occurs whenever $i_L(t)$ is greater than I_a (i.e., $i_c(t)$ is flowing into the capacitor) and discharging of the output capacitor occurs whenever $i_L(t)$ is less than I_a. The change in inductor current, assuming a constant load current, is

$$\Delta i_L = \Delta i_c + \Delta i_0 \simeq \Delta i_c. \tag{2.16}$$

The charging and discharging intervals, therefore, must be equal during a switching cycle and are both equal to half the switching period. The average charging or discharging current, which flows for $(t_{on}/2) + (t_{off}/2) = (T/2)$ is

$$I_c = \frac{\Delta I}{4}. \tag{2.17}$$

The capacitor voltage $v_c(t)$ is

$$v_c(t) = v_c(0) + \frac{1}{C}\int_0^{T/2} i_c(t)\mathrm{d}t \tag{2.18}$$

The capacitor ripple voltage Δv_c is given by:

$$\Delta v_c = v_c(t) - v_c(0) = \frac{1}{c}\int_0^{T/2} \frac{\Delta I}{4}\mathrm{d}t = \frac{T\Delta I}{8C} = \frac{\Delta I}{8f_s C}. \tag{2.19}$$

Substituting ΔI from Equation (2.14) into Equation (2.19), the capacitor ripple voltage is

$$\Delta v_c = \frac{DV_s(1-D)}{f_s L}\frac{1}{8f_s C} = \frac{V_s D(1-D)}{8f_s^2 LC}. \tag{2.20}$$

The capacitor ripple voltage Δv_c is also equal to the output ripple voltage Δv_o, since the output capacitor is connected directly across the load. It can be seen that the output ripple voltage is inversely proportional to f_s^2 and the LC product. Hence, to decrease the output ripple voltage, the product of LC should be large and the switching frequency should be high. Since the output inductor L, and the output capacitor, C, form a low-pass filter in the buck converter, the choice of the values of L and C determines

the cutoff frequency of the output low-pass filter and ultimately determines the amount of switching ripples and spikes in the output.

Switching waveforms for the buck converter operating in the continuous mode are shown in Figure 2.4. The input current is discontinuous, and a smoothing input filter, consisting of a series inductor and a shunt capacitor, is normally required to reduce electromagnetic interference (EMI). The output inductor current is continuous, due to the freewheeling action of the freewheeling diode. During the on-time, the output capacitor is initially discharged because the output inductor current is smaller than the required load current, $i_o(t)$. However, as the output inductor current increases beyond the current required by the load, the output capacitor is charged. The

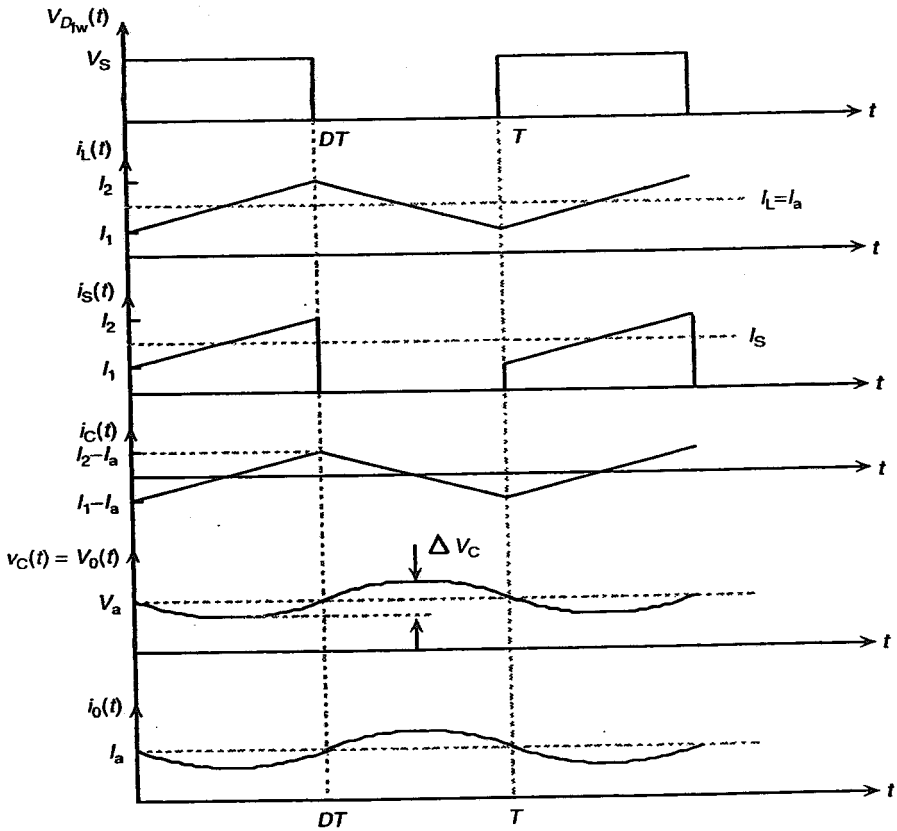

Figure 2.4 Buck converter switching waveforms.

maximum capacitor charging current, $I_2 - I_a$, occurs at the end of the on-time, i.e., DT. The maximum capacitor discharging current, $I_1 - I_a$, occurs at the end of the switching cycle. It should be noted that the capacitor ripple voltage lags its current by 90°.

Neglecting the switching losses, the efficiency of the buck converter can be calculated in terms of conduction losses in the NPN switching transistor Q_s and the freewheeling diode D_{fw}. The conduction losses are

$$P_{loss} = P_{Q_s} + P_{D_{fw}} = I_o^2 R_{on} \frac{t_{on}}{T} + I_o \left(1 - \frac{t_{on}}{T}\right) V_{D_{fw}}, \tag{2.21}$$

where R_{on} is the on-state resistance of the switching transistor Q_s and $V_{D_{fw}}$ is the diode forward drop, which is current dependent. Thus, the efficiency of the buck converter is

$$\eta = \frac{P_{out}}{(P_{out} + P_{loss})} = \frac{V_a}{(V_a + I_o R_{on} D + (1 - D) V_{D_{fw}})}. \tag{2.22}$$

It is evident that a higher efficiency is achieved by minimizing the R_{on} and the $V_{D_{fw}}$.

2.2.2 Discontinuous Mode

For a given value of load resistance, the ratio of the peak inductor current I_{L_p} to the average inductor current I_L becomes larger as the inductance becomes smaller according to Equation (2.14). The value of L for which $i_L = 0$ at one and only one point per cycle is defined as the *critical inductance*, L_c. When this happens, the stored energy in the inductor is completely expended just prior to the beginning of the next switching cycle. The peak inductor current, I_{L_p}, is twice the average inductor current, I_L, i.e.,

$$I_{L_p} = 2I_L = \Delta I = \frac{(V_s - V_a) t_{on}}{L_c} = \frac{(V_s - V_a) D}{f_s L_c}. \tag{2.23}$$

The critical inductance L_c can be found by assuming an ideal buck converter whereby the input power is equal to its output power. The input power is given as

$$P_{in} = V_s I_s = V_s I_L D. \tag{2.24}$$

since $I_s = DI_L$. The output power is

$$P_{out} = \frac{V_a^2}{R}, \tag{2.25}$$

therefore,

$$V_s I_L D = \frac{V_a^2}{R}. \tag{2.26}$$

The average inductor current I_L can be found from Equation (2.23), and is

$$I_L = \frac{\Delta I}{2} = \frac{(V_s - V_a)D}{2f_s L_c}. \tag{2.27}$$

Substituting I_L from Equation (2.27) into Equation (2.26) results in

$$V_s \frac{(V_s - V_a)D^2}{2f_s L_c} = \frac{V_a^2}{R}. \tag{2.28}$$

Substituting $D = (V_a/V_s)$ into the numerator of the left-hand side of the above equation yields

$$\frac{V_s^2(1 - D)D^2}{2f_s L_c} = \frac{V_a^2}{R}, \tag{2.29}$$

simplifying gives

$$\frac{(1 - D)D^2 V_s^2}{2f_s L_c} = \frac{V_s^2 D^2}{R}. \tag{2.30}$$

The critical inductance L_c is then

$$L_c = \frac{R(1 - D)}{2f_s}. \tag{2.31}$$

As can be seen, the critical inductance L_c is directly proportional to the load resistance R and inversely proportional to the switching frequency f_s. As f_s increases, L_c decreases. Increasing the load current or decreasing the load resistance R also reduces L_c. It is important for the inductance not to go below L_c when designing for a large load swing. The inductor current $i_L(t)$ is not continuous when L is less than L_c. The buck converter is said to be operating in its discontinuous conduction mode when this occurs. For a constant inductance L, the buck converter will be operating in the discontinuous mode if the load resistance R is greater than its critical load resistance R_c. Thus,

$$R_c = \frac{R_{nom}}{1 - D}; \quad R_{nom} = 2f_s L, \tag{2.32}$$

where R_{nom} is a design parameter and is defined in Ref. 2. This design parameter is evident from Equation (2.31).

It is necessary to modify the mode 2 equivalent circuit to account for the energy in the inductor expended before the start of the next switching cycle. Figure 2.5(a) and (b) shows the mode 2 equivalent circuits for the buck switching converter operating in the discontinuous mode.

Define t_2, which is less than the switching period T, as the time at which $i_L(t)$ goes to zero as shown in Figure 2.6. From the finite current constraint [1] or the constant volt-second requirement in an inductor, the

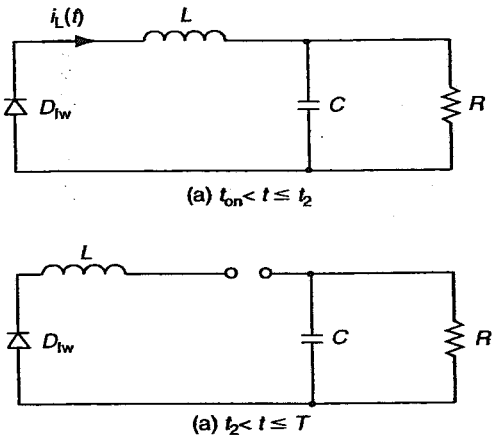

Figure 2.5 Discontinuous mode 2 equivalent circuits for the buck converter.

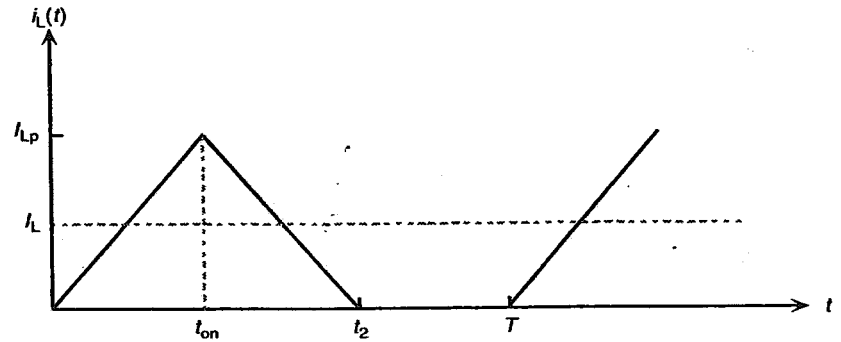

Figure 2.6 Discontinuous-mode inductor current waveform.

average inductor voltage per cycle for the buck converter operating in the discontinuous mode is zero in accordance with the equation:

$$(V_s - V_a)t_{on}f_s - V_a(t_2 - t_{on})f_s = 0. \tag{2.33}$$

Since the average capacitor current I_C per switching cycle is zero, for steady-state operation, then the average inductor current I_L is equal to the average output current I_a:

$$\frac{I_{Lp}t_2 f_s}{2} = \frac{V_a}{R}. \tag{2.34}$$

The voltage across the inductor is related to the rate of increase of its current, thus

$$(V_s - V_a) = L\frac{I_{L_p}}{t_{on}}. \tag{2.35}$$

Simplifying (2.33) and multiplying by f_s gives

$$V_s t_{on} f_s - V_a t_2 f_s = 0. \tag{2.36}$$

Solving for $t_2 f_s$ in Equation (2.34) and I_{L_p} in Equation (2.35) and substituting into Equation (2.36), we have

$$V_a^2 + V_a V_s \frac{D^2 L_c}{(1-D)L} - V_s^2 \frac{D^2 L_c}{(1-D)L} = 0. \tag{2.37}$$

The open-loop voltage conversion ratio V_a/V_s of the buck converter in the discontinuous mode of operation can be obtained by solving the above quadratic equation:

$$\frac{V_a}{V_s} = \frac{D\left[\sqrt{(4L(1-D)/L_c) + D^2} - D\right]}{2L(1-D)/L_c} \tag{2.38}$$

or

$$\frac{V_a}{V_s} = \frac{2}{1 + \sqrt{1 + (4L(1-D)/D^2 L_c)}}, \quad L < L_c. \tag{2.39}$$

Figure 2.7 shows the voltage conversion ratio versus the duty cycle of the buck converter operating in the continuous and discontinuous modes for several values of L/L_c.

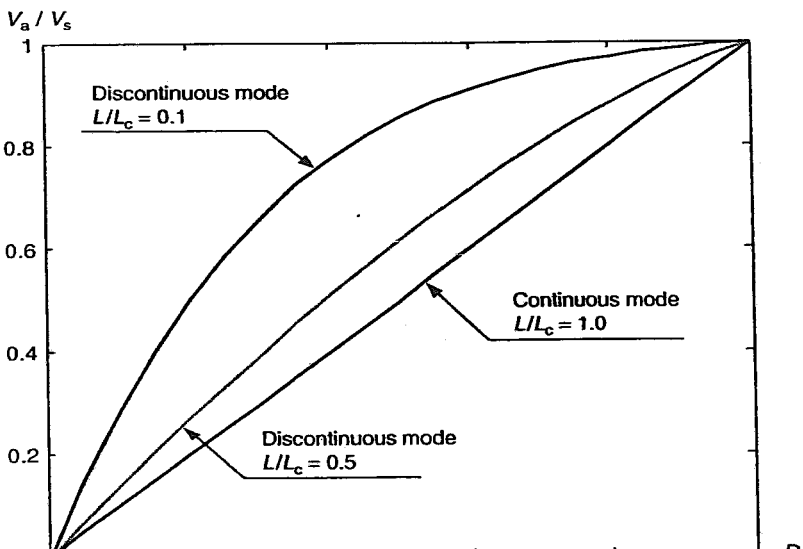

Figure 2.7 Open-loop voltage conversions ratio versus duty cycle of the buck converter operating in continuous and discontinuous modes.

In the discontinuous mode of operation, the average output voltage increases rapidly at small L/L_c values with increasing duty cycle and then asymptotically reaches the input supply voltage V_s. As the L/L_c value approaches 1, the voltage conversion ratio versus duty cycle plot becomes more linear. The voltage conversion ratio versus duty cycle in the continuous mode of operation ($L/L_c > 1$) is linear with a slope equal to 1. The time t_2 at which the inductor current reduces to zero can be obtained by substituting Equation (2.38) into Equation (2.36). Thus,

$$t_2 = \frac{(2L(1-D)/L_c f_s)}{\sqrt{(4L(1-D)/L_c) + D^2} - D} \quad \text{for } L < L_c. \tag{2.40}$$

Figure 2.8 shows the t_2/T ratio versus the duty cycle of the buck converter in the discontinuous mode of operation.

As shown, t_2/T decreases with decreasing L/L_c values for a constant duty cycle. Furthermore, t_2/T decreases more rapidly for small L/L_c values, as the duty cycle decreases. The energy stored in the inductor is less because of small L/L_c values in the discontinuous mode; therefore, the discharge time

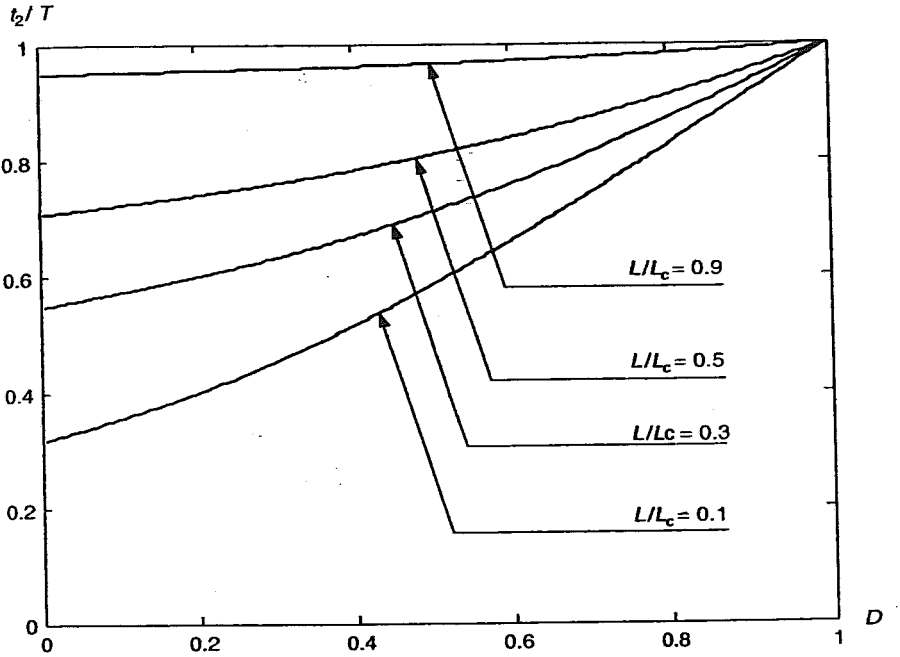

Figure 2.8 The t_2/T versus duty cycle of the buck converter in the discontinuous mode of operation.

t_2 is smaller. Using L'Hôpital's rule in Equation (2.38), it can be shown that as the inductor value reduces to zero, the average output voltage V_a approaches the input voltage V_s. The switching waveforms for a discontinuous mode of operation are shown in Figure 2.9.

Discontinuous mode of operation is frequently used at low power levels, especially where large output load ranges are possible. It is common practice to design the switching converter to operate either in the continuous or the discontinuous mode, avoiding the change from one mode of operation into the other during normal operation. This is to avoid changes in the switching converter model that may lead to serious regulation or stability problems. If the load of a buck converter is suddenly removed, the output voltage of an open-loop buck converter will rise to the same level as the input voltage. In a closed-loop buck converter, the output voltage will fall to zero with a time constant dependent on the values of the output capacitance and any leakage resistance inherent in the circuit. The advantages of the buck converter are its ability to easily control output voltages and currents during turn-on and turn-off and

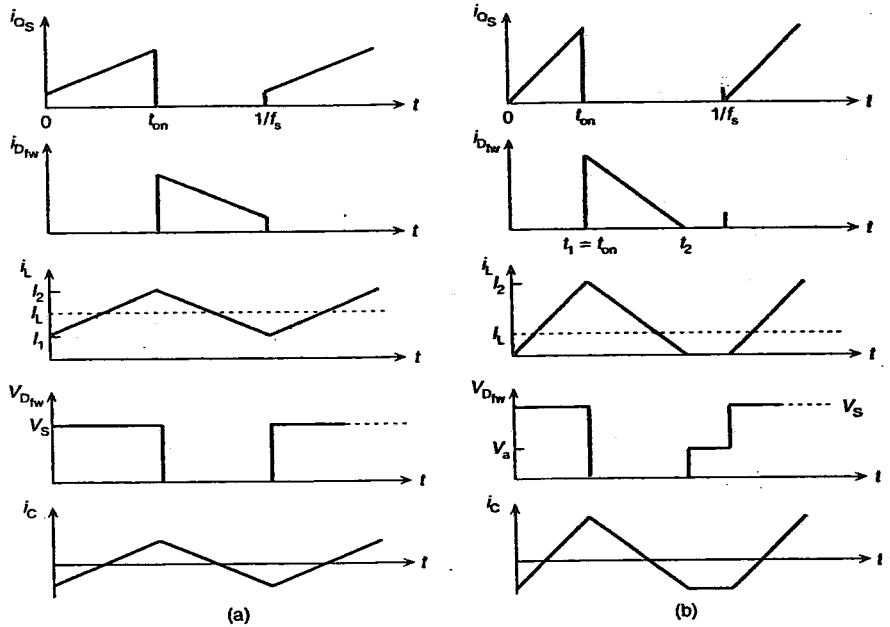

Figure 2.9 Buck converter waveforms for (a) $L > L_c$ and (b) $L < L_c$.

under fault conditions. The boost converter, however, does not possess such advantageous properties.

Example 2.1. The buck converter shown in Figure 2.1 has an input voltage of 10 V. The switching frequency is 1 kHz. The load requires an average voltage of 5 V with a maximum ripple voltage of 20 mV. The maximum ripple current of the output inductor is 0.2 A. Determine: (a) the duty cycle, (b) the output inductance, (c) the output capacitance, and (d) the output capacitance if the switching frequency is increased to 10 kHz.

Solution. The given parameters for the buck converter are: $V_s = 10\,\text{V}, f_s = 1\,\text{kHz}$, $V_a = 5\,\text{V}$, $\Delta V_a = 20\,\text{mV}$, and $\Delta I_L = 0.2\,\text{A}$.

(a) From Equation (2.10),

$$D = \frac{V_a}{V_s} = \frac{5}{10} = 0.5.$$

(b) From Equation (2.14),

$$L = \frac{DV_s(1-D)}{f_s \Delta I} = \frac{0.5(10)(0.5)}{1000(0.2)} = 0.0125\,\text{H} = 12.5\,\text{mH}.$$

(c) From Equation (2.20),

$$C = \frac{V_s D(1-D)}{8 f_s^2 L \Delta V_a} = \frac{10(0.5)(0.5)}{8(1000)^2 0.0125(0.02)} = 1250\,\mu\text{F}.$$

(d) The duty cycle does not change since the output voltage remains at 5 V. The output inductance is

$$L = \frac{0.5(10)(0.5)}{10000(0.2)} = 0.00125\,\text{H}.$$

Thus, the output capacitance is

$$C = \frac{10(0.5)(0.5)}{8(10000)^2 0.00125(0.02)} = 125\,\mu\text{F}.$$

This example illustrates that increasing the switching frequency by an order of magnitude decreases the values of both the output inductor and capacitor by an order of magnitude. Hence, increasing the switching frequency of the buck converter, assuming that increased switching losses do not degrade its performance, decreases its size, weight, and cost.

2.3 SYNCHRONOUS RECTIFIER

The current technology in computer microprocessors and peripherals requires power supply voltages of 1.2 V at high currents. An important limitation in efficiency is the voltage drop across the diode, V_d. When the output voltage of a buck converter is calculated, considering V_d yields:

$$V_a = DV_s - (1-D)V_d. \tag{2.41}$$

It is obvious that the larger the voltage drop across the diode is, the smaller is the resulting output voltage. The ability of the MOSFET channel to conduct current in both directions makes it possible to replace the Schottky diode by a synchronous rectifier, which is gated when the diode should conduct. The gate signal to this device is complementary to that of the main switch M_1. Figure 2.10 shows an example of a buck converter with a synchronous rectifier M_2.

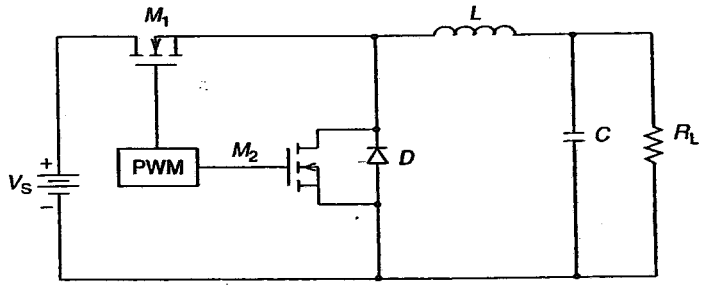

Figure 2.10 Synchronous rectifier.

Sometimes, the MOSFET may not be fast enough, and a Schottky diode is connected in parallel to assist during the turn on. Once M_2 is completely on, the voltage drop across its channel resistance may be much smaller than the forward voltage drop of the diode and it will take on all the current.

The synchronous rectification enables the current through the inductor to reverse its direction; thus, the synchronous buck converter of Figure 2.10 works only in the continuous conduction mode.

2.4 BOOST CONVERTER

The boost converter is capable of providing an output voltage, which is greater than the input voltage. It is also known as a *ringing choke* or a step-up converter. A boost converter using a power MOSFET as the switching transistor is shown in Figure 2.11.

Its switching waveforms are shown in Figure 2.12. The operation of the boost converter can also be divided into two modes, depending on the switching actions of its switching transistor. Similar to the buck converter,

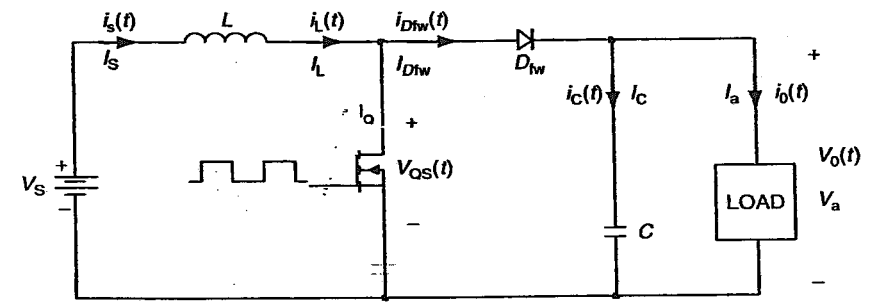

Figure 2.11 Circuit schematic of a boost converter.

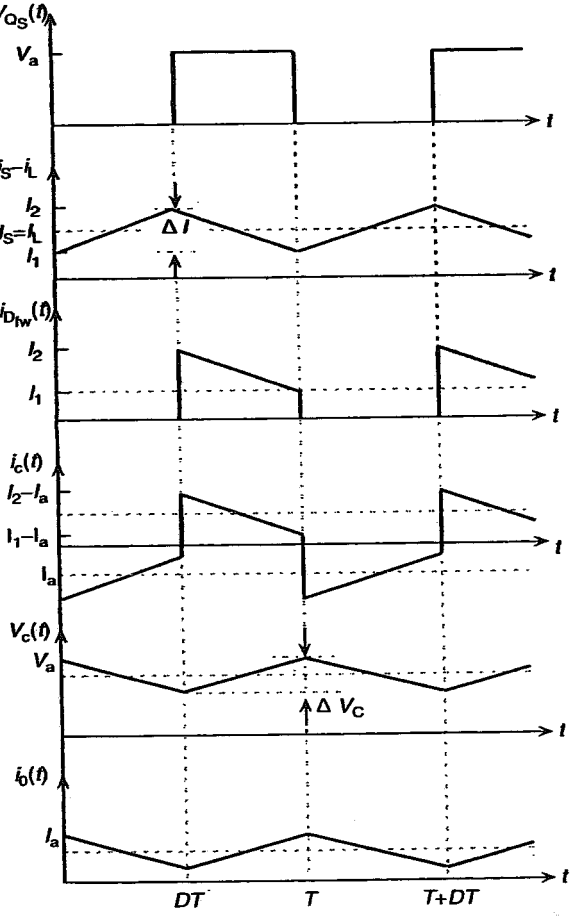

Figure 2.12 Waveforms for the boost converter.

the boost converter can either be operating in the continuous or discontinuous mode.

2.4.1 Continuous Mode

Mode 1 ($0 < t \leq t_{on}$)

Mode 1 begins when the switching transistor Q_s is switched on at $t = 0$ and it terminates at $t = t_{on}$ (i.e., $0 < t \leq t_{on}$). The equivalent circuit for mode 1 is shown in Figure 2.13.

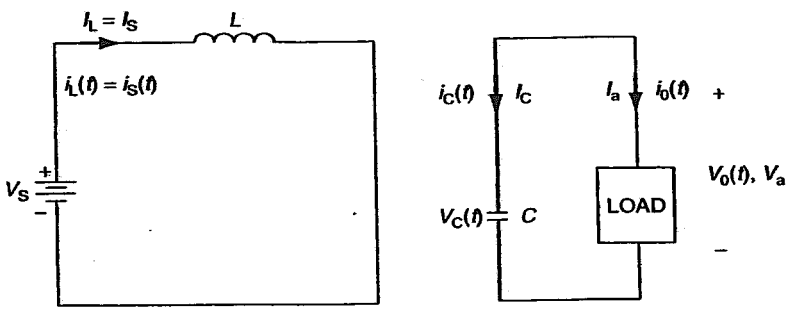

Figure 2.13 Mode 1 equivalent circuit for the boost converter ($0 < t \leq t_{on}$).

The diode D_{fw} is reverse biased since the voltage drop across the switching transistor Q_s is smaller than the output voltage. The inductor current $i_L(t)$ ramps up linearly from I_1 to I_2 in time t_{on}:

$$V_s = L\frac{I_2 - I_1}{t_{on}} = L\frac{\Delta I}{t_{on}}. \tag{2.42}$$

The duration of this interval t_{on} can be expressed as

$$t_{on} = \frac{L\Delta I}{V_s}. \tag{2.43}$$

The energy stored in the inductor is

$$E = \frac{1}{2}L(\Delta I)^2 = \frac{1}{2L}V_s^2 t_{on}^2. \tag{2.44}$$

The output current during this interval is supplied entirely from the output capacitor C, which is chosen large enough to supply the load current during the on-time, t_{on}, with a minimum specified droop in output current.

Mode 2 ($t_{on} \leq t < T$)

Mode 2 begins when the switching transistor Q_s is switched off at $t = t_{on}$. The equivalent circuit for this mode is shown in Figure 2.14. Since the current in the inductor cannot change instantaneously, the voltage in the inductor reverses its polarity in an attempt to maintain a constant current. The current, which was flowing through the switching transistor Q_s, would now flow through L, C, diode D_{fw}, and the load. The inductor current falls

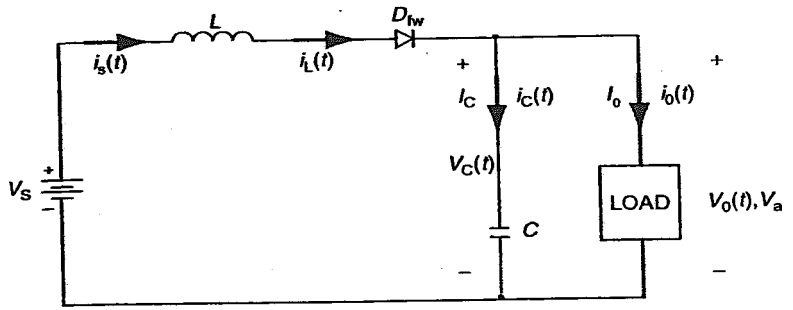

Figure 2.14 Mode 2 equivalent circuit for the boost converter ($t_{on} < t \leq T$).

until the switching transistor Q_s is turned on again in the next cycle. The inductor delivers its stored energy to the capacitor C and charges it up via D_{fw} to a higher voltage than the input voltage, V_s. This energy supplies the current and replenishes the charge drained away from the capacitor C when it alone was supplying the load current during the on-time. The voltage across the inductor is $(V_s - V_a)$ and its current falls linearly from I_2 to I_1 in time t_{off}:

$$V_s - V_a = L\frac{I_1 - I_2}{t_{off}} \tag{2.45}$$

or

$$V_a - V_s = L\frac{\Delta I}{t_{off}}. \tag{2.46}$$

The duration of the interval t_{off} can then be expressed as

$$t_{off} = \frac{L\Delta I}{V_a - V_s}. \tag{2.47}$$

Since the change in the peak-to-peak current ΔI is the same during t_{on} and t_{off} for steady-state operation, it can be shown from Equations (2.43) and (2.47) that

$$\Delta I = \frac{V_s t_{on}}{L} = \frac{(V_a - V_s)t_{off}}{L}. \tag{2.48}$$

Substituting $t_{on} = DT$ and $t_{off} = (1 - D)T$ into Equation (2.47), we have

$$V_s DT = (V_a - V_s)(1 - D)T = V_a(1 - D)T - V_s(1 - D)T. \tag{2.49}$$

Simplifying the above equation,

$$V_s DT = V_a(1 - D)T - V_s T + V_s DT \tag{2.50}$$

or

$$V_s = V_a(1 - D). \tag{2.51}$$

The average output voltage V_a for a boost converter is

$$V_a = \frac{V_s}{1 - D}. \tag{2.52}$$

Thus, the average output voltage V_a is inversely proportional to $(1-D)$. It is obvious that the duty cycle D cannot be equal to 1 because there would not be any energy transfer to the output. Assuming a lossless boost converter, then

$$V_s I_s = V_a I_a = \frac{V_s I_a}{(1 - D)}. \tag{2.53}$$

The average input current I_s can be expressed as

$$I_s = \frac{I_a}{(1 - D)}. \tag{2.54}$$

Note that the average output current I_a is reduced by the factor of $(1-D)$ from the average input current since the output power can only be at best equal to the input power. The switching period T is the sum of t_{on} and t_{off}:

$$T = \frac{1}{f_s} = t_{on} + t_{off} = \frac{L\Delta I}{V_s} + \frac{L\Delta I}{V_a - V_s} = \frac{L\Delta I V_a}{V_s(V_a - V_s)}. \tag{2.55}$$

The peak-to-peak inductor current ripple ΔI is

$$\Delta I = \frac{V_s(V_a - V_s)T}{LV_a} = V_s \frac{(V_s/(1 - D)) - V_s}{f_s L V_a}. \tag{2.56}$$

Simplifying the above equation, we have

$$\Delta I = \frac{V_s D}{f_s L}. \tag{2.57}$$

Thus, the magnitude of the peak-to-peak inductor current ΔI is inversely proportional to the switching frequency f_s and the inductance L.

Comparatively speaking, ΔI is larger in magnitude for the boost converter than the peak-to-peak current ripple in the buck converter, as shown in Figure 2.15. For a constant V_s/f_sL, the peak-to-peak inductor current ripple in the buck converter is smaller than the peak-to-peak inductor current ripple in the boost converter by a factor of $(1-D)$.

When the switching transistor Q_s is switched on, the capacitor supplies the load current for the entire on-time. Thus, the average capacitor current, I_c, is equal to the average output current I_a during this interval. During the off-time interval, the output capacitor is charged. The capacitor charging current decreases linearly from an initial value of $I_2 - I_a$ to a final value of $I_1 - I_a$ as shown in Figure 2.12. For steady-state operation, the average capacitor charging current during the off-time interval must be equal to the average capacitor discharging current during the on-time interval. The capacitor ripple voltage can be found by recognizing that the average capacitor current during the on-time is equal to the average output current I_a. Thus,

$$\Delta v_c = v_c - v_c(0) = \frac{1}{C}\int_0^{t_{on}} I_a dt = \frac{I_a t_{on}}{C}. \tag{2.58}$$

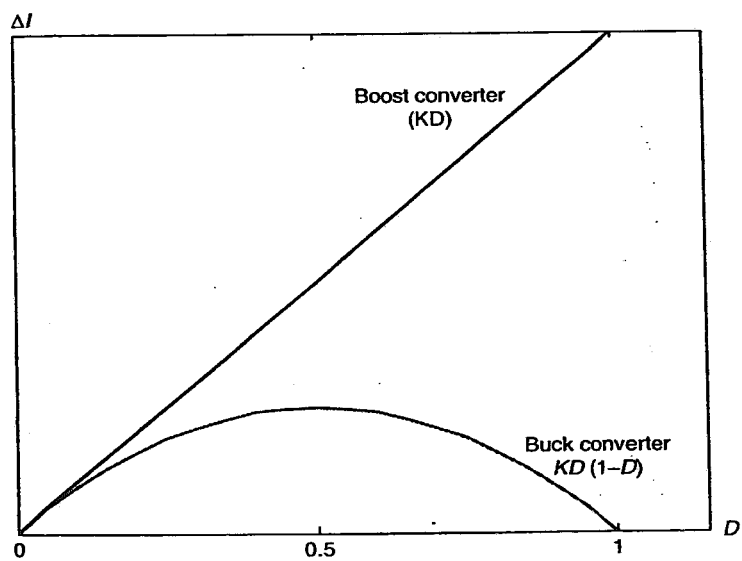

Figure 2.15 A comparison of the peak-to-peak inductor ripple current versus the duty cycle for the buck and boost converters at a constant $K = V_s/f_sL$.

From Equation (2.50)

$$V_a = \frac{V_s}{1-D} = \frac{V_s T}{T - DT} = \frac{V_s T}{T - t_{on}} \tag{2.59}$$

or

$$T - t_{on} = \frac{V_s T}{V_a}. \tag{2.60}$$

The on-time, t_{on}, can also be expressed as

$$t_{on} = T - \frac{V_s T}{V_a} = \frac{V_a - V_s}{f_s V_a}. \tag{2.61}$$

Substituting Equation (2.61) into Equation (2.58),

$$\Delta v_c = \frac{I_a(V_a - V_s)}{V_a f_s C} = \frac{I_a(V_a - V_s)}{\frac{V_s}{1-D} f_s C} \tag{2.62}$$

Simplifying the above equation,

$$\Delta v_c = \frac{I_a((V_s - V_s + DV_s)/(1-D))}{(V_s/(1-D))f_s C} = \frac{I_a D}{f_s C}. \tag{2.63}$$

The peak-to-peak output ripple voltage, Δv_o, is equal to the capacitor peak-to-peak ripple voltage, Δv_c. It is evident that Δv_o can be reduced by either increasing the switching frequency or the capacitance of the output capacitor. The inductor is used for energy storage, and it does not act as a part of the output filter. Therefore, the peak-to-peak output ripple voltage of the boost converter is generally larger than that of the buck converter.

2.4.2 Discontinuous Mode

If the current flowing through the inductor has fallen to zero before the next turn-on of the switching transistor Q_s, the boost converter is said to be operating in the discontinuous mode. The critical inductance, L_c, can be derived by assuming that the input power of the boost converter is equal to the output power:

$$V_s I_s = \frac{V_a^2}{R}. \tag{2.64}$$

The average inductor current is

$$I_L = \frac{\Delta I}{2} = \frac{V_s D}{2 f_s L_c}. \tag{2.65}$$

Since the average input current, I_s, is also equal to the average inductor current, I_L, then

$$V_s \frac{V_s D}{2 f_s L_c} = \frac{V_a^2}{R}. \tag{2.66}$$

The critical inductance, L_c, is

$$L_c = \frac{RD(1-D)^2}{2 f_s}. \tag{2.67}$$

The boost converter will be operating in the discontinuous mode if the load resistance, R, is greater than its critical resistance, R_c, given by

$$R_c = \frac{R_{nom}}{D(1-D)^2}, \tag{2.68}$$

where R_{nom} is a design parameter equal to $2 f_s L$[2].

Figure 2.16 shows the mode 2 equivalent circuits of the boost converter operating in the discontinuous mode. The voltage conversion ratio of the boost converter for the discontinuous mode of operation can be derived by imposing a constant volt-second requirement on its inductor. The average voltages across the inductor are V_s and $(V_a - V_s)$ during the DT and D_2T intervals as shown in Figure 2.17, respectively.

Thus

$$V_s D - (V_a - V_s) D_2 = 0, \tag{2.69}$$

where D_2 is defined as $(t_2 - t_{on})/T$.

The average input current, I_s, is equal to the average inductor current, I_L, in the boost converter, where

$$I_L = \frac{I_{L_p}}{2} = \frac{V_s D}{2 L f_s}. \tag{2.70}$$

$$I_a = \frac{1}{T} \int_{t_{on}}^{t_2} I_L \mathrm{d}t = \frac{t_2 - t_{on}}{T} I_L. \tag{2.71}$$

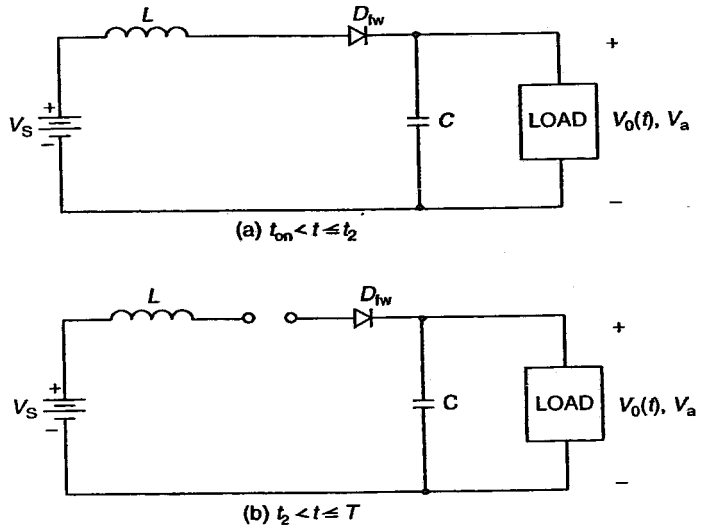

Figure 2.16 Discontinuous mode 2 equivalent circuits for the boost converter.

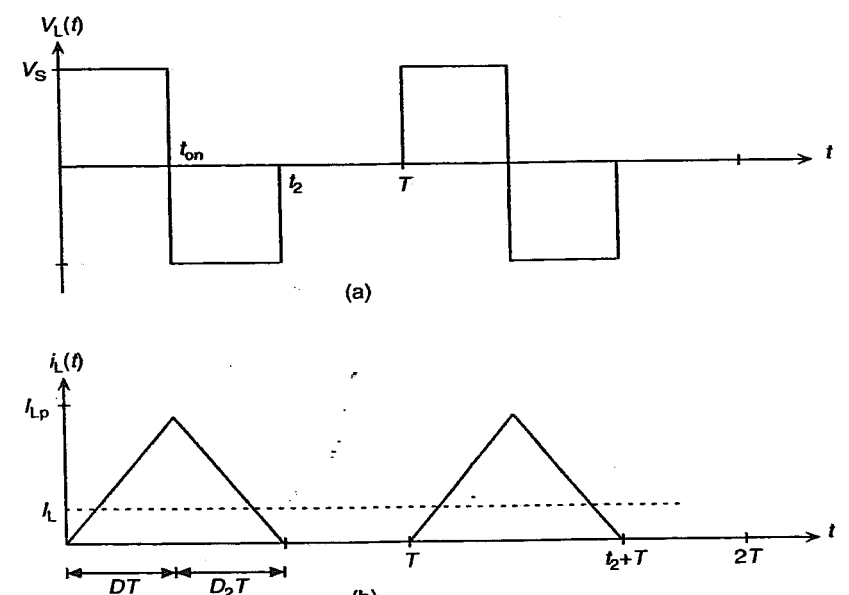

Figure 2.17 Waveforms for (a) voltage across and (b) current flowing through the inductor for a boost converter in the discontinuous mode of operation.

The average output current, I_a, is related to the average inductor current, I_L, by a factor D_2, viz.,

$$I_a = \frac{V_a}{R} = I_L D_2. \tag{2.72}$$

Substituting Equations (2.70) and (2.72) into Equation (2.69) yields a quadratic equation:

$$V_a^2 - V_s V_a - \frac{V_s^2 D L_c}{L(1-D)^2} = 0. \tag{2.73}$$

The open-loop voltage conversion ratio, V_a/V_s, in the discontinuous mode of operation can be found by solving the quadratic equation:

$$\frac{V_a}{V_s} = \frac{1 + \sqrt{1 + (4DL_c/L(1-D)^2)}}{2} \quad \text{for } L \leq L_c. \tag{2.74}$$

Figure 2.18 shows the open-loop voltage conversion ratio versus duty cycle of the boost converter operating in both the continuous and discontinuous modes. As shown, the voltage conversion characteristics of the two modes of operation differ from each other only in the rate of increase of the average output voltage. In the discontinuous mode of operation, the voltage conversion ratio increases at a much faster rate compared to the voltage conversion ratio in the continuous mode of operation. Thus, the discontinuous mode of operation of a boost converter yields a larger average output voltage at a smaller duty cycle compared to the continuous mode of operation. The discontinuous-mode switching waveforms of a boost converter are shown in Figure 2.19.

The input current of the boost converter is continuous. At the initial turn-on of the boost converter, an inrush current with an amplitude of several times the steady-state input current is flowing through the switching transistor. The switching transistor must be able to handle this initial switching stress. It is also important to limit the inrush current so as not to saturate the input inductor. Otherwise, a higher inrush current limited only by the source impedances and parasitic resistances will flow. The output current is always pulsating in both the continuous and discontinuous modes of operation. The output voltage is very sensitive to changes in duty cycle; therefore, the design of the feedback circuitry is critical. The effects of component parasitic resistances become quite noticeable when the average output voltage V_a is greater than three times the input voltage V_s. The boost converter must always have a load connected to its output; otherwise, the

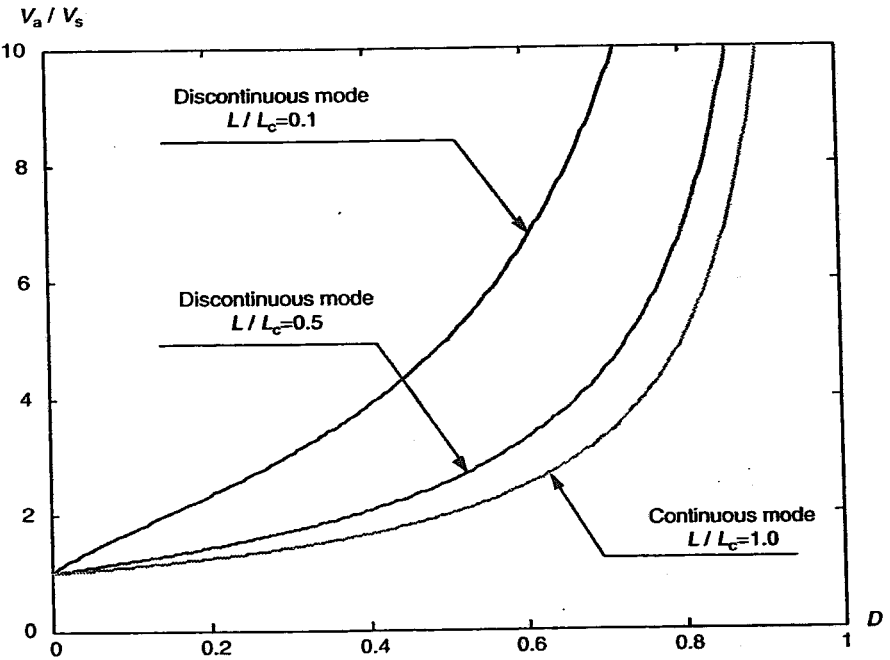

Figure 2.18 Open-loop voltage conversion ratio versus duty cycle of the boost converter operating in the continuous and discontinuous modes.

output voltage will continue to rise until a component (usually the output capacitor) fails. If the output of the boost converter is shorted, simply reducing the duty cycle of the switching transistor will not limit the amount of current drawn from the input supply. This is because the switching transistor is not in series with the output. An additional switching transistor in series with the input supply must be added if an overload protection is desired.

2.5 BUCK–BOOST CONVERTER

The buck–boost converter is a special cascade combination of a buck converter and a boost converter which provides an output voltage that may be less than or greater than the input voltage, with a polarity opposite to that of the input voltage. As such, it is also known as an inverting converter. The

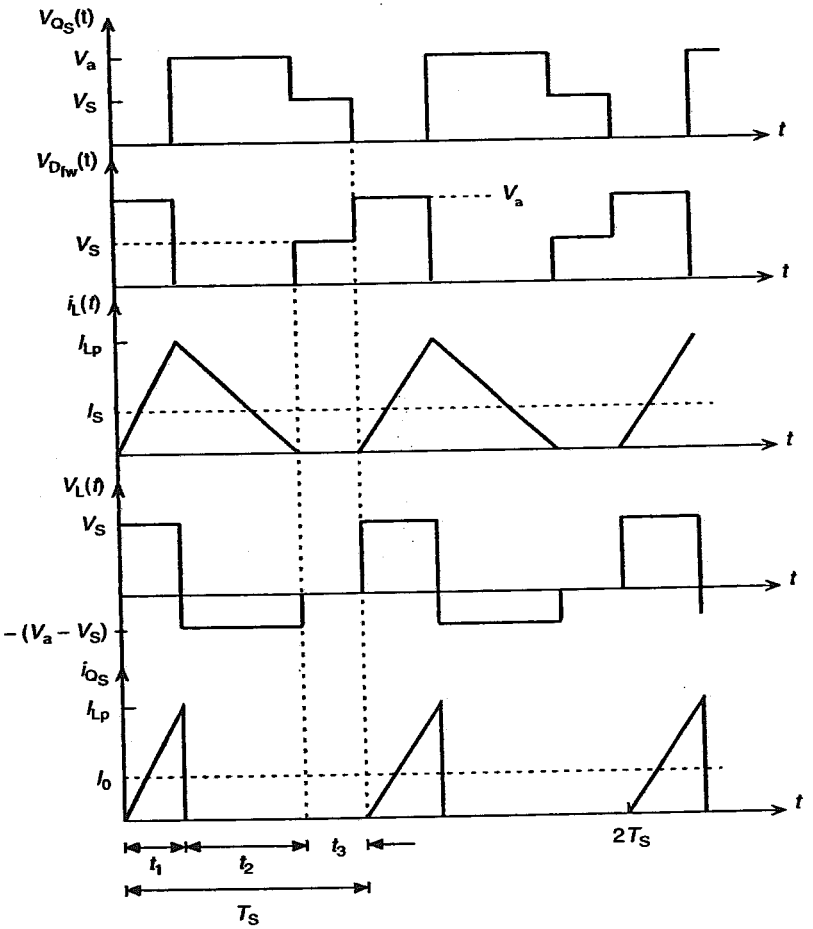

Figure 2.19 Waveforms for the discontinuous-mode boost converter.

basic circuit for a buck–boost converter is shown in Figure 2.20. Its switching waveforms are shown in Figure 2.21. The operation of this converter can also be divided into two modes, depending on the switching actions of its switching transistor. Depending on the continuity of the current flowing through the inductor, the operation of the buck–boost converter can also be classified as the continuous or discontinuous mode.

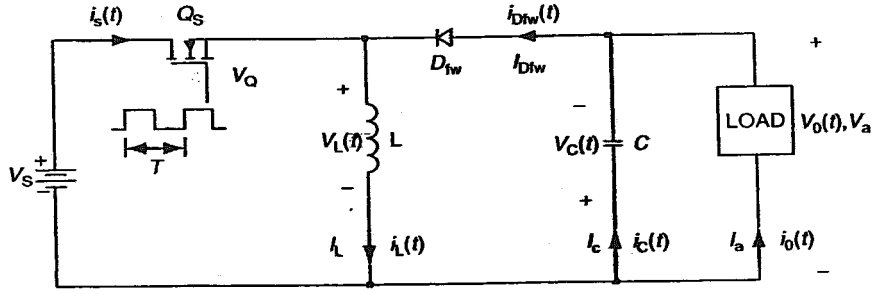

Figure 2.20 Circuit schematic of a buck–boost converter.

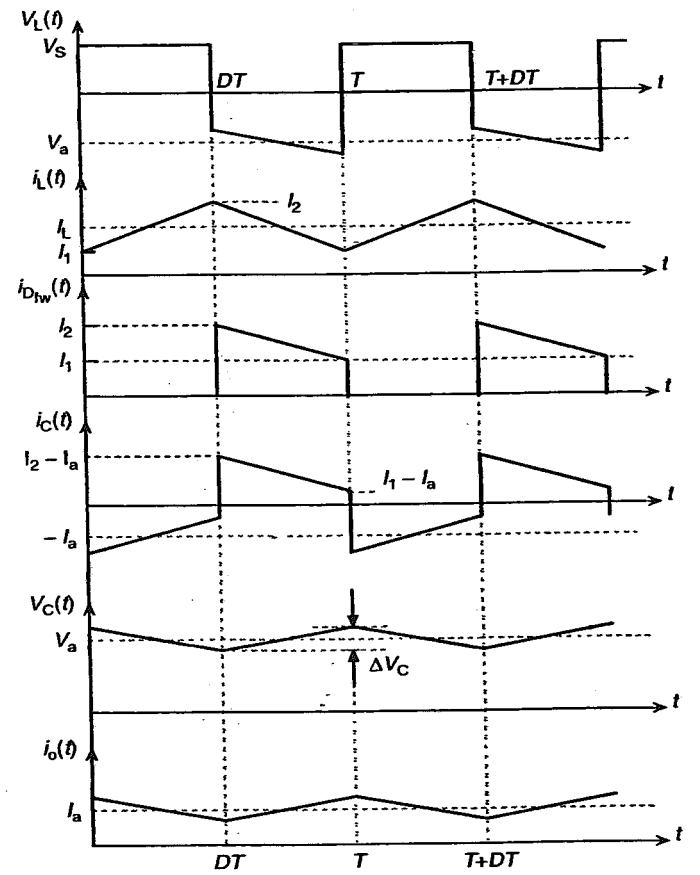

Figure 2.21 Buck–boost converter waveforms.

2.5.1 Continuous Mode

Mode 1 ($0 < t \leq t_{on}$)

Mode 1 begins when the switching transistor, Q_s, is turned on at $t = 0$. Its equivalent circuit is shown in Figure 2.22. The freewheeling diode, D_{fw}, is reverse-biased since the voltage across the inductor is near the input voltage, V_s, assuming that the output voltage, $v_o(t)$, is of negative polarity. The inductor current rises linearly from I_1 to I_2 in the time t_{on}:

$$V_s = L\frac{I_2 - I_1}{t_{on}} = L\frac{\Delta I}{t_{on}}. \tag{2.75}$$

The duration of mode 1, t_{on}, can be expressed as

$$t_{on} = \frac{L\Delta I}{V_s}, \tag{2.76}$$

and the energy stored in the inductor is

$$E_L = \frac{1}{2}L\left(\frac{V_s t_{on}}{L}\right)^2 = \frac{1}{2L}V_s^2 t_{on}^2. \tag{2.77}$$

Mode 2 ($t_{on} \leq t < T$)

Mode 2 begins when the switching transistor, Q_s, is switched off at t_{on}. Its equivalent circuit is shown in Figure 2.23. The polarity of the voltage across the inductor reverses in an attempt to keep its current from changing. Thus, at the instant of turning off, the current that was flowing through the inductor would now flow through L, C, D_{fw} and the load. This current

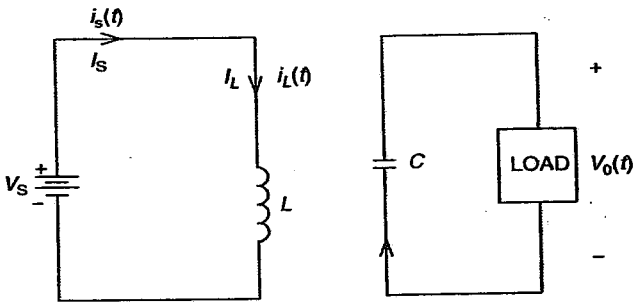

Figure 2.22 Mode 1 equivalent circuit of the buck–boost converter ($0 < t \leq t_{on}$).

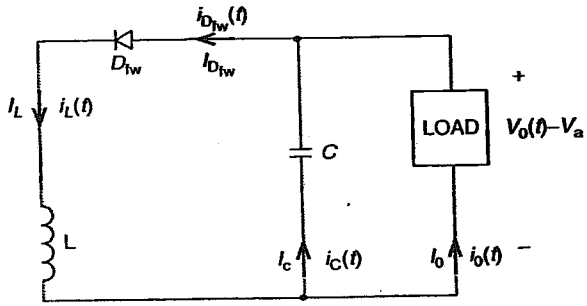

Figure 2.23 Mode 2 equivalent circuit for the buck–boost converter ($t_{on} < t \leq T$).

flowing upward through the output capacitor charges the top end of the capacitor to a negative voltage as previously assumed. The energy stored in inductor L is transferred to the load and the inductor current falls until the switching transistor, Q_s, is switched on again in the next cycle. Assuming the inductor current falls linearly from I_2 to I_1 in time t_{off}:

$$V_a = -L\frac{\Delta I}{t_{off}}. \tag{2.78}$$

The duration of this interval, t_{off}, can then be expressed as

$$t_{off} = -\frac{L\Delta I}{V_a}. \tag{2.79}$$

Since the peak-to-peak inductor ripple currents present during the t_{on} and t_{off} intervals are the same for steady-state operation, it can be shown from Equations (2.76) and (2.79) that

$$\Delta I = \frac{V_s t_{on}}{L} = -\frac{V_a t_{off}}{L}. \tag{2.80}$$

Rearranging the above equation,

$$V_s t_{on} = -V_a t_{off}. \tag{2.81}$$

Substituting $t_{on} = DT$ and $t_{off} = (1-D)T$ into the above equation,

$$V_s DT = -V_a(1 - D)T. \tag{2.82}$$

Simplifying, we get

$$V_s = -\frac{V_a(1-D)}{D}. \tag{2.83}$$

The average output voltage, V_a, is then

$$V_a = -\frac{V_s D}{1-D}. \tag{2.84}$$

As can be seen, V_a has an opposite polarity to the input voltage V_s. The numerator D is the output conversion factor of a buck converter while the denominator $(1-D)$ is the output conversion factor for a boost converter. Assuming a lossless buck–boost converter, the input power, $(V_s I_s)$, is equal to the output power $(V_a I_a)$:

$$V_s I_s = V_a I_a = \frac{I_a(-V_s D)}{1-D}. \tag{2.85}$$

The average input current, I_s, can be expressed as

$$I_s = -\frac{I_a D}{1-D}. \tag{2.86}$$

The switching period, T, is the sum of t_{on} and t_{off}:

$$T = t_{on} + t_{off} = \frac{\Delta IL}{V_s} - \frac{\Delta IL}{V_a} = \frac{\Delta IL(V_a - V_s)}{V_s V_a}. \tag{2.87}$$

The peak-to-peak inductor ripple current, ΔI, is then

$$\Delta I = \frac{V_s V_a T}{L(V_a - V_s)} = \frac{V_s V_a}{f_s L(V_a - V_s)}. \tag{2.88}$$

Simplifying the above equation, we obtain

$$\Delta I = \frac{V_s(-V_s D/(1-D))}{f_s L((-V_s D/(1-D)) - V_s)} = \frac{V_s D}{f_s L}. \tag{2.89}$$

The peak-to-peak inductor ripple current is, therefore, similar to that of the boost converter. When the switching transistor is switched on, the output capacitor supplies the load current for the entire on-time interval. The average discharging current of the capacitor is equal to I_a. During the off-time interval, the output capacitor is charged by the stored energy in the inductor. The capacitor charging current decreases linearly from $I_2 - I_a$ to

$I_1 - I_a$ during this interval. For steady-state operation, the average capacitor charging current during the off-time interval must be equal to the average capacitor discharging current during the on-time interval. The peak-to-peak ripple capacitor voltage, Δv_c, can be found by integrating the average capacitor discharging current during the on-time interval:

$$\Delta v_c = \frac{1}{C}\int_0^{t_{on}} I_c dt = \frac{1}{C}\int_0^{t_{on}} I_a dt = \frac{I_a t_{on}}{C}. \tag{2.90}$$

t_{on} can be expressed in terms of the input voltage, switching frequency, and average output voltage. From Equation (2.84), with $t_{on} = DT$

$$V_a = -\frac{V_s(t_{on}/T)}{1-(t_{on}/T)} = \frac{V_s(t_{on}/T)}{(t_{on}/T)-1}. \tag{2.91}$$

Multiplying both sides of the above equation by its denominator gives

$$\left(\frac{t_{on}}{T} - 1\right) V_a = V_s \frac{t_{on}}{T} \tag{2.92}$$

or

$$\frac{t_{on}}{T} V_a - \frac{t_{on}}{T} V_s = V_a \tag{2.93}$$

or

$$t_{on}\left(\frac{V_a - V_s}{T}\right) = V_a. \tag{2.94}$$

The on-time, t_{on}, can be expressed as

$$t_{on} = \frac{V_a T}{V_a - V_s} = \frac{V_a}{(V_a - V_s) f_s}. \tag{2.95}$$

Substituting Equation (2.95) into Equation (2.90), we have

$$\Delta v_c = \frac{I_a V_a}{(V_a - V_s) f_s C}. \tag{2.96}$$

Substituting Equation (2.85) into Equation (2.96), the peak-to-peak capacitor ripple voltage is

$$\Delta v_c = \frac{I_a(-V_s D/(1-D))}{((-V_s D/(1-D)) - V_s) f_s C} = \frac{I_a D}{f_s C}. \tag{2.97}$$

The above result can also be found by recognizing that $t_{on} = D/f_s$. As can be seen, the expression for the output ripple voltage, Δv_o, is similar to that for the boost converter and its magnitude can be decreased by either increasing the switching frequency f_s or increasing the output capacitor value. Again, the input inductor is used for energy storage and it does not act as part of the output filter.

2.5.2 Discontinuous Mode

If the current flowing through the inductor has fallen to zero before the next turn-on of the switching transistor, the buck–boost converter is said to be operating in the discontinuous mode. The boundary between the continuous and discontinuous modes in an open-loop configuration is determined by the critical inductance, L_c. The critical inductance can be derived by assuming an ideal buck–boost converter with the input power equal to its output power:

$$V_s I_s = \frac{V_a^2}{R}. \tag{2.98}$$

The average inductor current is

$$I_L = \frac{I_{Lp}}{2} = \frac{V_s D}{2 f_s L_c}. \tag{2.99}$$

The average input current I_s is related to the average inductor current I_L by

$$I_s = \frac{1}{T}\int_0^{t_{on}} I_L \, dt = \frac{t_{on}}{T} I_L \tag{2.100}$$

or

$$I_s = I_L D. \tag{2.101}$$

Substituting Equation (2.99) into Equation (2.101) and then into Equation (2.98), we get:

$$\frac{V_s^2 D^2}{2 f_s L_c} = \frac{V_a^2}{R}. \tag{2.102}$$

The critical inductance, L_c, is

$$L_c = \frac{RD^2V_s^2}{2f_sV_a^2} = \frac{R(1-D)^2}{2f_s}. \tag{2.103}$$

The open-loop conversion ratio V_a/V_s can be found from Equation (2.102):

$$\frac{V_a^2}{V_s^2} = \frac{RD}{2f_sL} \tag{2.104}$$

or

$$\frac{V_a}{V_s} = \sqrt{\frac{RD^2}{2f_sL}} = \frac{-D}{(1-D)}\sqrt{\frac{L_c}{L}} \text{ for } L \le L_c. \tag{1.105}$$

Figure 2.24 shows the open-loop voltage conversion ratio versus duty cycle of the buck–boost converter for the two modes of operation. As shown, the

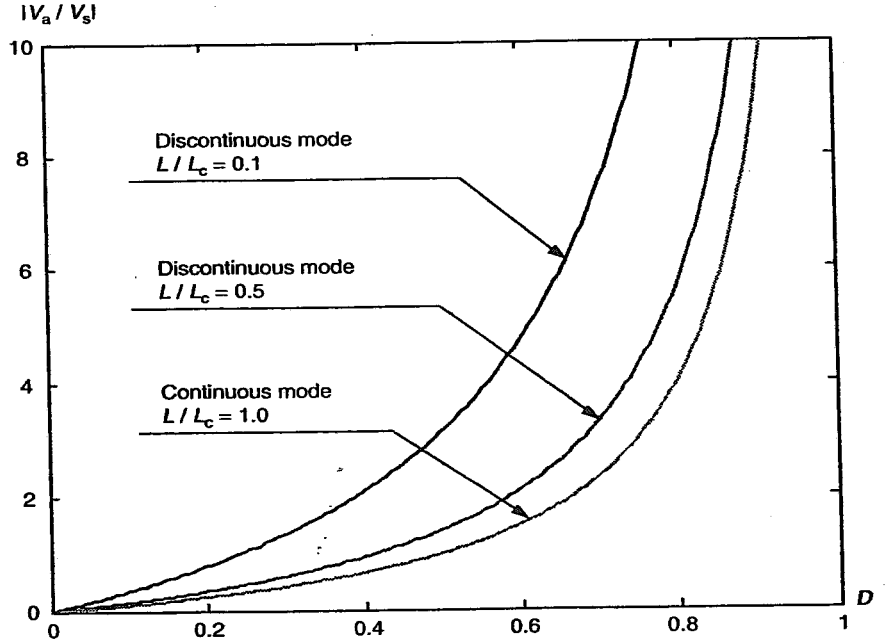

Figure 2.24 Open-loop voltage conversion ratio versus duty cycle of the buck–boost converter operating in the continuous and discontinuous modes.

voltage conversion ratio increases more rapidly for smaller L/L_c values. Thus, the discontinuous mode of operation of a buck–boost converter yields a larger average output voltage V_a compared to the continuous mode of operation for a similar duty cycle.

The output voltage of the buck–boost converter has the opposite polarity with respect to the input voltage. The input current in the buck–boost converter is pulsating. As in the boost converter, a high inrush current is flowing during initial turn-on of the switching transistor. The switching transistor, therefore, must be capable of handling this initial switching stress.

Comparisons of the voltage conversion ratio V_a/V_s for the three types of switching converters are shown in Figure 2.25. As shown previously, a linear relationship between the input and output voltages are a characteristic of the buck switching converter. The rapid changing output voltage, when operating at above 50% duty cycle in the boost and the buck–boost switching converters, presents some challenging stability problems in the designing of these switching converters.

Example 2.2. The buck–boost converter shown in Figure 2.20 has an input voltage of 12 V and a load resistance of 24 Ω. The switching frequency is 10 kHz. The values of the inductor and output capacitor are 1 mH and 100 μF, respectively. If the output voltage is required to be twice that of the input, determine (a) the duty cycle, (b) the peak-to-peak output ripple voltage, (c) the magnitude of the average input current, (d) the magnitude of the average inductor current, and (e) the peak inductor current.

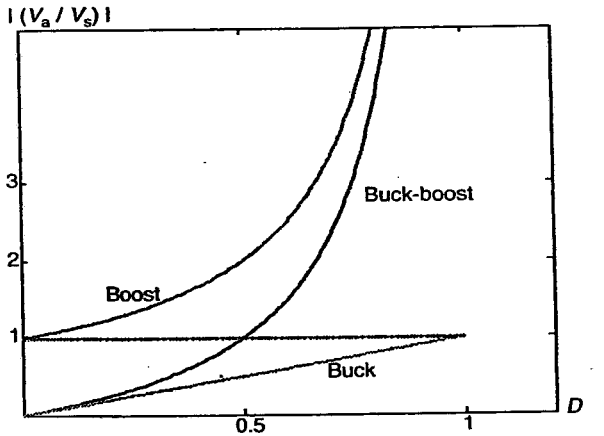

Figure 2.25 Comparisons of the voltage conversion ratios of buck, boost, and buck–boost switching converters.

Solution.

(a) From Equation (2.84), the voltage conversion ratio for the buck–boost converter is

$$\frac{V_a}{V_s} = -\frac{D}{(1-D)} = -2.$$

Therefore, the duty cycle, D, is 2/3 or 66.7%.

(b) From Ohm's law, the average output current is

$$I_a = \frac{V_a}{R} = \frac{24}{24} = 1\,\text{A}.$$

From Equation (2.97), the peak-to-peak output ripple voltage is

$$\Delta V_a = \frac{I_a D}{f_s C} = \frac{1(2/3)}{10000(100 \times 10^{-6})} = 0.667\,\text{V}.$$

(c) From Equation (2.86), the magnitude of the average input current is

$$I_s = \frac{I_a D}{1-D} = \frac{2/3}{1-(2/3)} = 2\text{A}.$$

(d) From Equations (2.86) and (2.100), the magnitude of the average inductor current is

$$I_L = \frac{I_a}{(1-D)} = \frac{1}{1-(2/3)} = 3\text{A}.$$

(e) From Equation (2.89), the peak-to-peak inductor ripple current is

$$\Delta I = \frac{V_s D}{f_s L} = \frac{12(2/3)}{10000(0.001)} = 0.8\text{A}.$$

The peak inductor current is

$$I_{L,\text{peak}} = I_L + \frac{\Delta I}{2} = 3 + \frac{0.8}{2} = 3.4\text{ A}.$$

2.6 CÛK CONVERTER [4]

The Cûk converter can be considered as a series combination of a boost converter followed by a buck converter with the particular feature that the

output boost capacitor is an energy source for the buck section of the system and that both converters share the same switching elements [5] as shown in Figure 2.26. It provides an output voltage which is less than, or greater than, the input voltage with an opposite polarity to its input voltage. It is a derivative of the buck–boost converter in that the energy transfer from the input to the output is achieved by a capacitor rather than by an inductor as in the buck–boost converter. Its switching waveforms are shown in Figure 2.27. Notice that the current flowing through the output capacitor, $i_{Co}(t)$, has been drawn in the negative direction according to the passive sign convention; therefore the waveforms show a change in polarity. The operation of the Cûk converter can be divided into two modes, depending on the switching actions of its switching transistor. The continuous mode of operation of the Cûk converter is discussed below.

Mode 1 ($0 < t \leq t_{on}$)

Mode 1 begins when the switching transistor, Q_s, is switched on at $t = 0$. Its equivalent circuit is shown in Figure 2.28. The current flowing through the input inductor, L_i, rises. At the same time, the voltage across the energy-transfer capacitor, C_t, reverse biases diode D_{fw} and turns it off. C_t discharges its energy to the circuit formed by C_t, C_o, L_o, and the load. If the current of the input inductor L_i rises linearly from $I_{L_{i1}}$ to $I_{L_{i2}}$ in time t_{on}:

$$V_s = L_i \frac{I_{L_{i2}} - I_{L_{i1}}}{t_{on}} = L_i \frac{\Delta I_{L_i}}{t_{on}}. \tag{2.106}$$

The duration of this interval, t_{on}, is

$$t_{on} = \frac{L_i \Delta I_{L_i}}{V_s}. \tag{2.107}$$

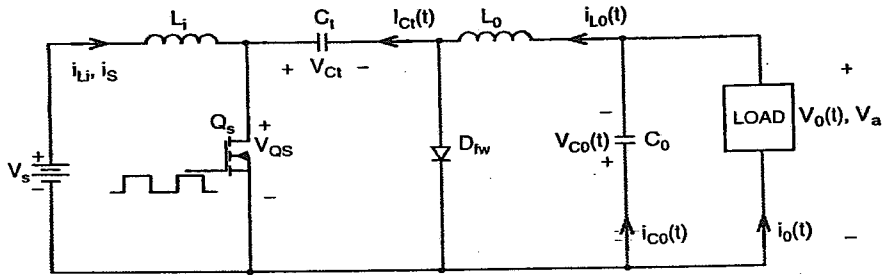

Figure 2.26 Circuit schematic of a Cûk converter.

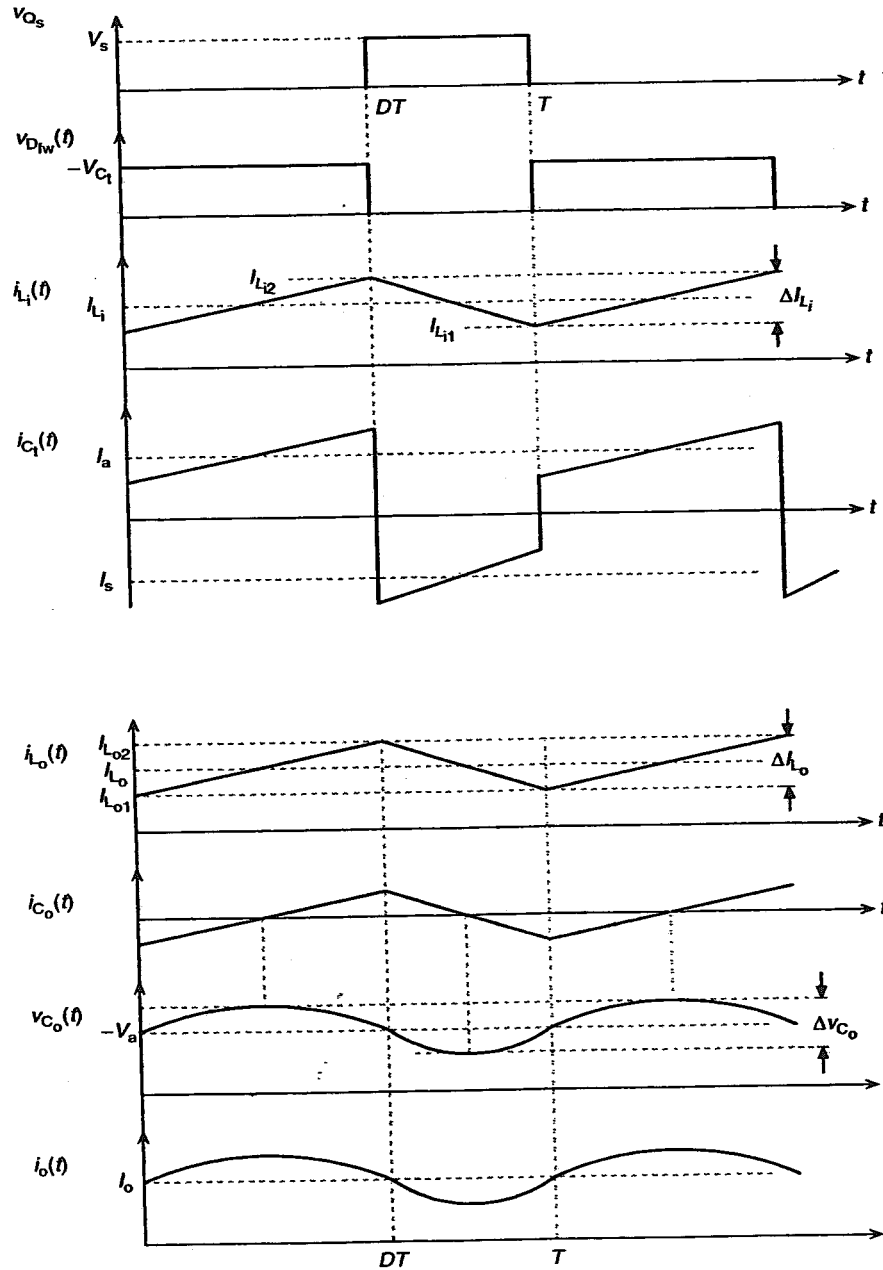

Figure 2.27 Cûk converter switching waveforms.

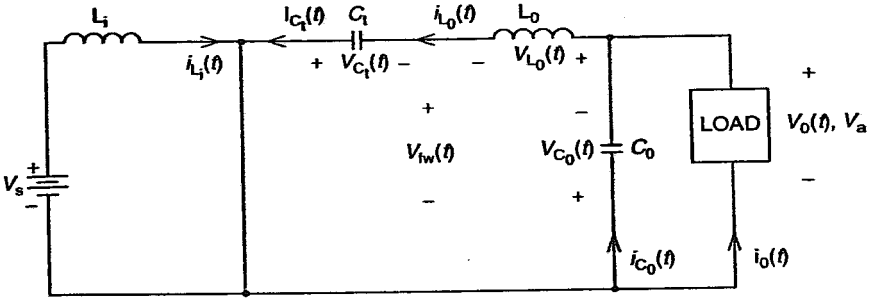

Figure 2.28 Mode 1 equivalent circuit for the Cûk converter.

Due to the discharge of C_t, the current flowing through the output inductor, L_o, rises linearly from $I_{L_{o1}}$ to $I_{L_{o2}}$ in time t_{on},

$$V_{Ct} - V_a = \frac{L_o(I_{L_{o2}} - I_{L_{o1}})}{t_{on}}. \tag{2.108}$$

The duration of t_{on} can, therefore, be expressed as

$$t_{on} = \frac{L_o \Delta I_{L_o}}{V_{Ct} - V_a}. \tag{2.109}$$

Mode 2 ($t_{on} \leq t < T$)

Mode 2 begins when the switching transistor, Q_s, is switched off at $t = t_{on}$. The voltage across the input inductor reverses its polarity in order to maintain its current uninterrupted. The diode D_{fw} is forward-biased since the anode is at a higher potential than its cathode. The converter's equivalent circuit is shown in Figure 2.29. The energy-transfer capacitor, C_t, is charged by the input source V_s and the stored energy in the input inductor L_i. The load current $i_o(t)$ is now supplied by the energy stored in the output inductor, L_o, and the output capacitor, C_o. The current flowing through the input inductor, L_i, falls linearly from $I_{L_{i2}}$ to $I_{L_{i1}}$ in time t_{off}:

$$V_s - V_{C_t} = L_i \frac{\Delta I_{L_i}}{t_{off}}. \tag{2.110}$$

The duration for the t_{off} interval is

$$t_{off} = \frac{L_i \Delta I_{L_i}}{V_s - V_{C_t}}, \tag{2.111}$$

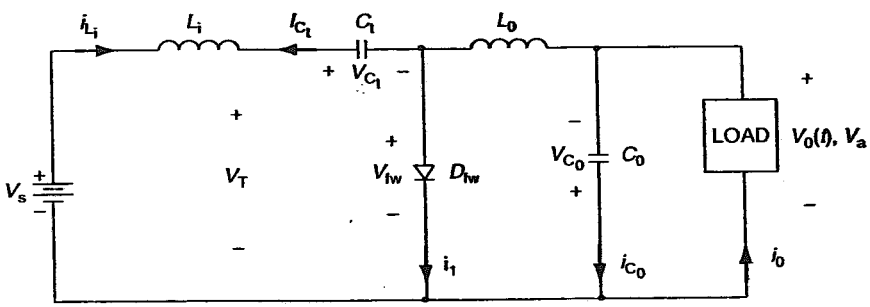

Figure 2.29 Mode 2 equivalent circuit for the Cûk converter.

where V_{Ct} is the average voltage across C_t. At the same time, the current flowing through the output inductor, $i_{Lo}(t)$, falls linearly from $I_{L_{o2}}$ to $I_{L_{o1}}$ in time t_{off}. Therefore,

$$V_a = -\frac{L_o \Delta I_{L_o}}{t_{off}}. \tag{2.112}$$

The duration for the t_{off} interval can also be expressed as

$$t_{off} = -\frac{L_o \Delta I_{L_o}}{V_a}. \tag{2.113}$$

The peak-to-peak ripple current in the input inductor L_i, ΔI_{L_i}, can be found from Equations (2.107) and (2.111):

$$\Delta I_{L_i} = \frac{V_s t_{on}}{L_i} = \frac{-(V_s - V_{C_t}) t_{off}}{L_i}. \tag{2.114}$$

Substituting $t_{on} = DT$ and $t_{off} = (1 - D)T$ into the above equation and solving for V_{Ct} gives

$$V_{C_t} = \frac{V_s}{1 - D}. \tag{2.115}$$

The energy-transfer capacitor stores its energy in the form of an electric field. The electrostatic energy stored in the energy-transfer capacitor is

$$E_c = \frac{1}{2} C_t V_{ct}^2 = \frac{1}{2} C_t \frac{V_c^2}{(1 - D)^2}. \tag{2.116}$$

The peak-to-peak ripple current in the output inductor, ΔI_{L_o}, can be found from Equations (2.108) and (2.112):

$$\Delta I_{L_o} = \frac{(V_{ct} - V_a)t_{on}}{L_o} = -\frac{V_a t_{off}}{L_o}. \tag{2.117}$$

Substituting $t_{on} = DT$ and $t_{off} = (1 - D)T$ into the above equation, we obtain

$$V_{ct} = -\frac{V_a}{D}. \tag{2.118}$$

Equating Equations (2.115) and (2.118)

$$\frac{V_s}{1 - D} = -\frac{V_a}{D}. \tag{2.119}$$

The average output voltage V_a is

$$V_a = \frac{-DV_s}{1 - D}. \tag{2.120}$$

This is similar to the average output voltage of the buck–boost converter. Assuming a lossless Cûk converter, the input power is equal to its output power, and

$$V_s I_s = V_a I_a = \frac{-DV_s}{1 - D} I_a. \tag{2.121}$$

The average input current, I_s, is

$$I_s = \frac{-DI_a}{1 - D}. \tag{2.122}$$

This is, again, similar to the average input current of the buck–boost converter. The switching period, T, is the sum of t_{on} and t_{off} from Equations (2.107) and (2.111):

$$T = \frac{1}{f_s} = t_{on} + t_{off} = \frac{L_i \Delta I_{L_i}}{V_s} + \frac{L_i \Delta I_{L_i}}{V_s - V_{C_t}}. \tag{2.123}$$

Simplifying

$$T = \frac{L_i V_{C_t} \Delta I_{L_i}}{V_s (V_{C_t} - V_s)}. \tag{2.124}$$

The peak-to-peak ripple current in the input inductor, ΔI_{L_i} can be determined from the above equation:

$$\Delta I_{L_i} = \frac{V_s(V_{C_t} - V_s)}{f_s L_i V_{C_t}}. \tag{2.125}$$

Simplifying

$$\Delta I_{L_i} = \frac{V_s D}{f_s L_i}. \tag{2.126}$$

Thus, the peak-to-peak ripple current in the input inductor is inversely proportional to the switching frequency and its inductance value. The switching period, T, can also be found from Equations (2.109) and (2.113):

$$T = \frac{1}{f_s} = t_{on} + t_{off} = \frac{L_o \Delta I_{L_o}}{V_{C_t} + V_a} - \frac{L_o \Delta I_{L_o}}{V_a} = \frac{L_o V_{C_t} \Delta I_{L_o}}{V_a(V_{C_t} + V_a)}. \tag{2.127}$$

The peak-to-peak ripple current in the output inductor is

$$\Delta I_{L_o} = \frac{V_a(V_{C_t} + V_a)}{f_s L_o V_{C_t}} \tag{2.128}$$

or

$$\Delta I_{L_o} = \frac{V_a(1 - D)}{f_s L_o} = \frac{D V_s}{f_s L_o}. \tag{2.129}$$

Thus, the peak-to-peak ripple current in the output inductor, ΔI_{L_o}, is also inversely proportional to its switching frequency and its inductance value, L_o.

When the switching transistor, Q_s, is switched on, the energy-transfer capacitor, C_t, discharges its stored energy to L_o, C_o, and the load circuit. The discharging current increases from $I_{L_{o1}}$ to $I_{L_{o2}}$. The average discharging current, I_{Ct}, in C_t is equal to the average output current, I_a. During the off-time, the energy-transfer capacitor is charged by the energy stored in the input inductor and the input source. The charging current decreases from $I_{L_{i2}}$ to $I_{L_{i1}}$. Therefore, the average charging current, I_{C_t}, is the same as the average input current, I_s. The charging and discharging current–time products for the energy-transfer capacitor, for steady-state operation, must be equal. The peak-to-peak ripple voltage of the energy-transfer capacitor, Δv_{C_t}, is

$$\Delta v_{C_t} = \frac{1}{C_t}\int_0^{t_{off}} I_{C_t}\,dt = \frac{1}{C_t}\int_0^{t_{off}} I_s\,dt = \frac{I_s t_{off}}{C_t}. \tag{2.130}$$

Since $t_{off} = (1 - D)T$ and $T = 1/f_s$, then

$$t_{off} = \frac{(1 - D)}{f_s}. \tag{2.131}$$

The peak-to-peak capacitor ripple voltage is

$$\Delta v_{C_t} = \frac{I_s(1 - D)}{f_s C_t}. \tag{2.132}$$

Thus, the peak-to-peak ripple voltage across the energy-transfer capacitor, Δv_{Ct}, is directly proportional to its average input current, I_s, and inversely proportional to the product of its switching frequency and the capacitance value. Assuming that the peak-to-peak load ripple current, Δi_o, is negligible, then $\Delta i_{L_o} = \Delta i_{Co}$. The average charging current of the output capacitor C_o, which flows for time $T/2$, is $I_{Co} = (\Delta I_{Lo}/4)$. Therefore,

$$\Delta v_{C_o} = \frac{1}{C_o}\int_0^{T/2} I_{Co}\,dt = \frac{1}{C_o}\int_0^{T/2} \frac{\Delta I_{L_o}}{4}\,dt = \frac{T\Delta I_{L_o}}{8C_o} = \frac{\Delta I_{L_o}}{8f_s C_o} \tag{2.133}$$

or

$$\Delta v_{C_o} = -\frac{V_a(1 - D)}{8C_o L_o f^2} = \frac{DV_s}{8C_o L_o f_s^2}. \tag{2.134}$$

The peak-to-peak output ripple voltage, Δv_o, is equal to the peak-to-peak output capacitor ripple voltage, Δv_{Co}, since the output capacitor is connected directly across the load. The most effective way to reduce the output ripple voltage is to increase the switching frequency, since the output ripple voltage is inversely proportional to the square of the switching frequency.

The input and output currents of the Cûk converter are continuous, which reduces EMI problems. The output ripple voltage and ripple current of the Cûk converter are much smaller than those of the buck–boost converter. A substantial weight and size reduction of the Cûk converter over the buck–boost converter is the result of a smaller output filter inductor, L_o, and a smaller energy-transfer capacitor C_t, because the capacitive energy storage in a Cûk converter is more efficient than the inductive energy storage in a

conventional buck–boost converter. The switching transistor and the freewheeling diode in the Cûk converter have to carry the currents flowing through both the input and output inductors. At first sight, it seems that the Cûk converter has higher DC conduction losses when compared to the conventional buck–boost converter. However, both types of switching converters have been shown to have the same DC conduction losses in the ideal case when both the parasitic resistances in the input and output inductors are neglected [6]. In fact, the Cûk converter has been shown to have an overall higher efficiency when compared to the conventional buck–boost converter with the same component values and output requirements. Furthermore, the use of coupled inductors in the Cûk converter has been shown to reduce both the output current ripple as well as the output switching ripple [7].

Example 2.3. The Cûk converter shown in Figure 2.26 has an input voltage of 48 V. The switching frequency is 64 kHz. The magnitude of the average output voltage is 36 V across a 9-Ω load resistor. The maximum ripple voltage across the energy-transfer capacitor is 0.5 V. If $L_i = 10\,\text{mH}$, $L_o = 1\,\text{mH}$, and $C_o = 100\,\mu\text{F}$, determine (a) the duty cycle, (b) the value of the energy-transfer capacitor, C_t, and (c) the peak-to-peak ripple current in L_i.

Solution.

(a) From Equation (2.120), the duty cycle is

$$D = \frac{V_a/V_s}{(1 + (V_a/V_s))} = \frac{(36/48)}{(1 + (36/48))} = 0.429.$$

(b) From Ohm's law, the average output current is

$$I_a = \frac{V_a}{R} = \frac{36}{9} = 4\,\text{A}.$$

From Equation (2.122), the average input current is

$$I_s = \frac{DI_a}{(1 - D)} = \frac{0.429(4)}{(1 - 0.429)} = 3\,\text{A}.$$

The value of the energy-transfer capacitor can be found from Equation (2.132):

$$C_t = \frac{I_s(1 - D)}{f_s \Delta v_{C_t}} = \frac{3(1 - 0.429)}{64000(0.5)} = 53.6\,\mu\text{F}.$$

(c) From Equation (2.114), the peak-to-peak ripple current in L_i is

$$\Delta I_{L_i} = \frac{V_s t_{on}}{L_i} = \frac{48(0.429/64000)}{10 \times 10^{-3}} = 0.032\,\text{A}.$$

2.7 CONVERTER REALIZATION WITH NONIDEAL COMPONENTS

In practical applications, components do not always behave as predicted. Unexpected parasitics and other effects may result in a capacitance that is a tenth of what was expected, or even worse, the capacitor may be acting like an inductor or the inductor acting like a capacitor.

So far, the basic configurations of DC–DC switching converters have been analyzed considering ideal components. This section introduces a nonideal model for capacitors and inductors and analyzes the impact that the nonidealities, including the semiconductor losses, have on the behavior of a switching converter. A buck converter is used as an example.

2.7.1 Inductor Model

Figure 2.30 illustrates the equivalent circuit model for a real inductor with parasitic elements. Most inductors can be represented with an acceptable degree of accuracy by one of the circuits shown in Figure 2.30. Circuit A typically represents an inductor that uses a magnetic core material, such as ferrite or powdered iron. Circuit B represents most nonmagnetic core inductors, commonly referred to as *air cores*.

Most inductors are used well below their self-resonant frequency (SRF) and the basic three-element inductor models will be very accurate under these conditions. The SRF of the inductor occurs when the inductive reactance (XL) is equal to the capacitive reactance (XC) of the inductor. The impedance of the inductor is at its maximum and would be infinite if there were no core losses or if the resistance of the inductor were zero. Above the SRF, the XC exceeds XL and the inductor behaves like a capacitor. As the frequency increases above the SRF, the inductor will go through other resonant phases, caused by secondary parasitic elements. Modeling this behavior requires a more complex equivalent circuit. For this reason, the typical useful range for the three-element inductor models is the SRF of the inductor plus about 25% [8].

The parasitic capacitor is usually very small. In switching applications it charges fast to the voltage applied to the inductor terminals contributing

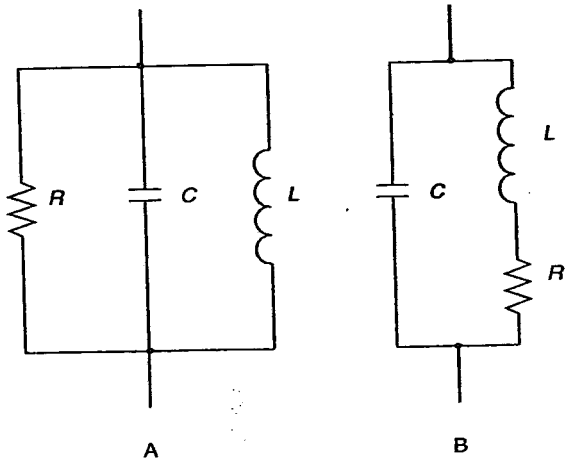

Figure 2.30 Inductor model.

with a current spike; after that no further current circulates through it. Therefore, an RL model is normally used to model power converters.

2.7.2 Semiconductor Losses

The switch, implemented with a BJT or a MOSFET, can be represented in the *on* state by a resistance (R_{on}). A good model for the forward biased diode is a voltage source (V_d) in series with the dynamic resistance of the diode (R_d). Other parasitics like capacitors and inductors are not considered here. Figure 2.31 represents a buck converter that has been modeled

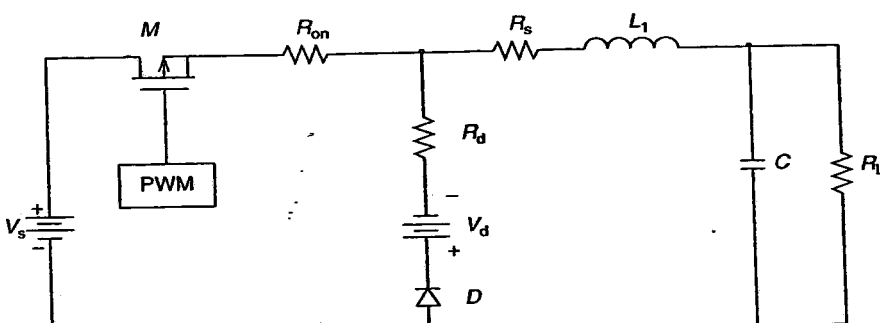

Figure 2.31 Equivalent circuit of a buck converter including losses.

including the losses of the inductor and the semiconductors. During T_{on}, the inductor voltage is

$$v_{L_{on}} = (V_s - V_a) - I_a(R_{on} + R_s). \tag{2.135}$$

During T_{off}, the inductor voltage is

$$v_{L_{off}} = -V_d - V_a - I_a(R_d + R_s). \tag{2.136}$$

For the steady-state operation, the time–voltage product in the inductor must be null; thus

$$Dv_{L_{on}} = (1 - D)v_{L_{off}}. \tag{2.137}$$

Then

$$D\{(V_s - V_a) - I_a(R_{on} + R_s)\} = (1 - D)\{-V_d - V_a - I_a(R_d + R_s)\}. \tag{2.138}$$

Approximating $I_a = V_a/R_L$ and assuming that $R_{on} = R_d$, the expression for the duty cycle can be derived as:

$$D = \frac{V_d + V_a(1 + ((R_{on} + R_s)/R_L))}{V_s + V_d}. \tag{2.139}$$

It is clear that the losses demand a larger than the ideal duty cycle for fixed V_a and V_s. Note that if $V_d = R_{on} = R_s = 0$, then the duty cycle adopts the ideal value.

The expression for the average output voltage yields

$$V_a = \frac{DV_s - (1 - D)V_d}{(1 + ((R_{on} + R_s)/R_L))}. \tag{2.140}$$

Therefore, for a fixed D and V_s, the losses reduce the output voltage.

2.7.3 Capacitor Model

The simple RLC model of Figure 2.32 is often considered a good representation of the capacitor in varying frequency applications. The resistive element is known as the effective series resistance (ESR), while the inductive element is the effective series inductance (ESL). However, things are never as simple as they seem. For example, the resistive element changes with frequency and electrolytic capacitors have a steep capacitance roll-off at higher frequencies [9].

The ceramic capacitor model is distinguished by a frequency-dependent resistive element that seems to result in a minimum ESR at or

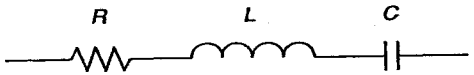

Figure 2.32 Capacitor model.

near the SRF of the capacitor. At the SRF the capacitive reactance and the inductive reactance cancel each other; thus, the capacitor gets reduced to its ESR. Though the capacitance may decay by 1% per decade of frequency, this is insignificant in modeling the performance and is usually disregarded. The tantalum capacitor shows a strong dependency of the capacitance with frequency, which can decay 20% or more per decade. This has been explained by different RC-ladders to define the performance.

Consider now that the ideal capacitor of the output filter of the buck converter of Figure 2.1 is replaced by its RLC model. A capacitor with a large ESL would produce spikes on the capacitor voltage due to the $\partial i_c/\partial t$. Since the ESL is not usually evident when the right capacitor is chosen, only the effect of the ESR will be analyzed. In the steady state, the average current through the capacitor is zero, with the current ripple through the inductor (ΔI) becoming the effective current through the capacitor. The ΔI will produce a voltage drop across the ESR that will add to the output ripple voltage. The magnitude of this extra ripple voltage can be calculated as:

$$\Delta v_{cESR} = \text{ESR}\Delta I. \tag{2.141}$$

PROBLEMS

2.1. A buck converter has an input voltage of 12 V. The switching frequency is 10 kHz. The load is a resistor of 6 Ω. The average load current is 1 A. If the ripple current of the output inductor is limited to 0.1 A and the ripple voltage of the output capacitor is 20 mV. Determine (a) the duty cycle, (b) the filter capacitance, and (c) the output inductance.

2.2. A boost converter has an input voltage of 12 V. The average output voltage is 15 V with a ripple of 100 mV. It has a resistive load of 3 Ω. If the inductor, L, is 1 mH and the output capacitor is 220 μF. Determine (a) the required switching frequency and (b) the peak-to-peak ripple current in the inductor. Sketch the waveforms for the currents flowing through the inductor and capacitor.

2.3. A buck–boost converter has an input voltage of 9 V and an inductor of 10 mH. The magnitude of the average output voltage is 12 V at a switching frequency of 1 kHz. Determine (a) the duty cycle and (b) the magnitude of the ripple inductor current in this converter.

2.4. Derive the critical inductance, L_c, in terms of the load resistance, R, duty cycle, D, and switching frequency, f_s, that will make the inductor current, in a practical buck converter, discontinuous. Assume that the voltage drop across the switching device is V_d and the average inductor current during the on-time is equal to half the peak inductor current.

2.5. A boost converter has a switching frequency of 1 kHz with a duty cycle of 50%. Its maximum ripple current is 4 A and the initial current is 10 A. Determine (a) the average input current, and (b) the average output current. Plot the inductor and output capacitor current waveforms using the passive sign convention. Determine the average charging and discharging currents for the output capacitor. Explain your results.

2.6. The component specifications for a Cûk converter are: $L_o = 150\ \mu H$, $C_o = 220\ \mu F$, and $L_i = 200\ \mu H$ and $C_t = 200\ \mu F$. The input voltage is 12 V. It is operating at a switching frequency of 25 kHz with a duty cycle of 25%. The average load current is 3 A. Determine (a) peak-to-peak ripple current in the inductor L_i, (b) peak-to-peak ripple current in the inductor L_o, and (c) the average input current, I_s. Plot the current flowing through the energy-transfer capacitor, $i_{Ct}(t)$, for a complete switching cycle. Determine the average charging and discharging currents for the energy-transfer capacitor.

2.7. The duty cycle for the two switches, S_1 and S_2, of a switching converter shown in Figure 2.33 is 40% with a switching frequency of 10 kHz. Determine (a) the output voltage, V_a, and its polarity, and (b) the peak-to-peak ripple current in the input inductor, ΔI_{L_i}. Sketch the current waveform flowing through the inductor L_i.

2.8. A buck–boost converter has an input voltage of 9 V, an inductor of 10 mH, an output resistant of 12 Ω, and an output capacitance of 200 μF. The magnitude of the average output voltage is 12 V with a

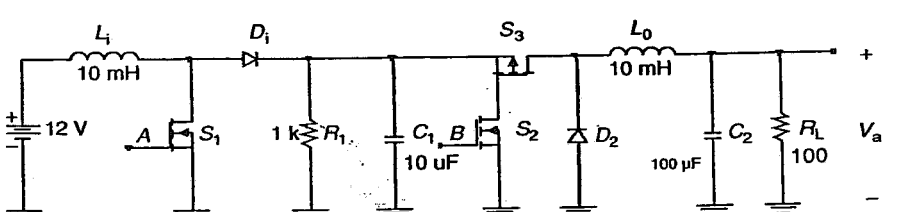

Figure 2.33 Circuit schematic of the switching converter for Problem 2.7.

switching frequency of 1 kHz. Determine (a) the duty cycle, (b) the magnitude of the average input current, (c) the peak input current, (d) the peak inductor current, and (e) the capacitor charging current–time product.

2.9. Calculate the efficiency of the buck converter of Figure 2.31. Find the requirements for high efficiency.

2.10. Find the maximum output voltage that can be obtained with the buck converter of Figure 2.31, when $V_s = 10\,V$, $V_d = 0.7\,V$, $R_{on} = R_d = 0.2\,\Omega$, $R_s = 1.2\,\Omega$, and $R_L = 3\,\Omega$.

2.11. Consider the ideal buck converter of Figure 2.1. Using PSpice, analyze the effect of an output capacitor with ESR $= 10\,m\Omega$, XESL(f_s) $= 0.1$ XC(f_s). Compare your results with the waveforms obtained using ideal components.

2.12. Draw the equivalent circuit for a boost converter including the losses in the transistor, the diode and the inductor; then calculate the duty cycle.

2.13. (a) Calculate the efficiency of a buck converter with $V_s = 5\,V$, $V_a = 1.2\,V$, $V_d = 0.3\,V$, and $R_L = 0.1\,\Omega$. (b) Repeat (a) replacing the diode with a synchronous rectifier with $R_{on} = 3\,m\Omega$.

2.14. (a) Calculate the critical load resistance for the buck converter of Example 2.1. (b) The addition of a synchronous switch, M_2, in parallel with the diode converts the circuit into a synchronous buck converter. Draw the steady-state waveforms for a load resistance 20% larger than the critical resistance.

2.15. Show that the charging and discharging intervals of the output capacitor of a buck converter are both equal to half the switching period.

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3

Resonant Converters

3.1 INTRODUCTION

The major thrusts in switching converter design are to achieve a higher power packing density and higher conversion efficiency. To increase the power packing density, the switching frequency of the switching converter is often increased to reduce the size and weight of its reactive components. However, the conventional or hard-switching switching converter, employing pulse-width modulation to control the dynamic transfer of electrical energy from the input to the output, suffers an excessive switching loss as its switching frequency approaches 1 MHz. The higher switching losses of the power transistor require a larger heat sink capacity that offsets the net magnetic size reduction when operating at a higher switching frequency. At high switching frequencies, capacitive turn-on losses in power MOSFETs become the predominant switching losses. A power MOSFET with a C_{ds} of 100 pF, switching at 500 V, will have a turn-on loss of $0.5C_{ds}f_sV_{ds}^2$, or 12.5 W, when operating at 1 MHz. However, the turn-on loss increases to

62.5 W when this device operates at a switching frequency of 5 MHz. Resonant converters offer an attractive solution to the above dilemma.

There are many topological variations of the resonant converter. Only two of the common resonant converter topologies, the quasi-resonant converter and the load-resonant converter, will be discussed in this chapter. The quasi-resonant converter employs an LC tank circuit to shape the current or voltage waveform of the switching transistor, resulting in a zero-current or zero-voltage condition during device turn-off or turn-on. Zero-current-switching (ZCS) quasi-resonant switches are employed to reduce the turn-off switching losses, while zero-voltage-switching (ZVS) quasi-resonant switches are used to mitigate the turn-on switching losses. In general, ZVS is preferable to ZCS at high switching frequencies. The load-resonant converter can be classified as either a voltage-source series-resonant converter or a current-source parallel-resonant converter. The voltage-source series-resonant converter can be further subdivided into either a series-loaded or parallel-loaded resonant converter. In the series-loaded resonant converter, the load is connected in series with the resonant circuit and the output voltage is obtained from the resonant current. As such, the output voltage is sensitive to load variations. However, the series-loaded resonant converter is inherently overload protected. In the parallel-loaded resonant converter, the load is connected in parallel with the resonant capacitor and the output voltage is obtained from the voltage across this capacitor. Because of this, the output voltage of the parallel-loaded resonant converter is not sensitive to load variations. However, it requires protection against overloading since the output energy is derived directly from the resonant capacitor.

One of the major advantages of resonant converters is the absorption of the switching transistor capacitance and other parasitic components into the converter topologies. However, the switching transistors in the resonant converters generally have to carry a higher peak current or voltage for the same output power than their counterparts in conventional switching converters. Since resonant converters regulate their output by changing their switching frequencies or by frequency modulation, electromagnetic interference may be unpredictable. The choice of using resonant converters over conventional switching converters should be based on the fact that the reduction in switching losses is greater than the increase in semiconductor device conduction losses associated with the higher peak current or voltage in the resonant topologies. A review of the fundamental concept of parallel and series resonant circuits is done to help with the analysis of some of the simple resonant converter topologies.

3.2 PARALLEL RESONANT CIRCUIT — A REVIEW

Consider a current source $\vec{I}_s(j\omega)$ connected in parallel with a resistor R, a capacitor C, and an inductor L, as shown in Figure 3.1. As the frequency of the current source changes, the voltage across terminals a and b is given by

$$\begin{aligned}\vec{V}_o(j\omega) &= \frac{\vec{I}_s}{(1/R) + j\omega C + (1/j\omega L)} \\ &= \frac{I_m \angle 0°}{\sqrt{(1/R^2) + (\omega C - (1/\omega L))^2} \angle \tan^{-1}[R(\omega C - (1/\omega L))]}.\end{aligned} \tag{3.1}$$

The resonant frequency in this circuit is defined as the frequency at which the impedance seen by the current source is purely resistive. This frequency makes the corresponding admittance purely conductive, since $Y = Z^{-1}$. The resonant frequency, ω_n, is then

$$\omega_n C = \frac{1}{\omega_n L} \tag{3.2a}$$

or

$$\omega_n = \frac{1}{\sqrt{LC}}. \tag{3.2b}$$

At the resonant frequency, the voltage across terminals a and b is

$$\vec{V}_o(\omega = \omega_n) = V_{m_{max}} = I_m R. \tag{3.3}$$

The capacitor current, $\vec{I}_c(\omega_o)$, during resonance is

$$\vec{I}_c(\omega = \omega_n) = \frac{V_o}{Z_c} = j\omega_n C I_m R = j I_m R \sqrt{\frac{C}{L}} \tag{3.4}$$

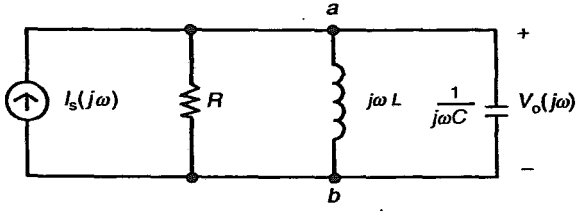


Figure 3.1 A parallel-resonant circuit.

while the inductor current, $\vec{I}_L(\omega_n)$, is

$$\vec{I}_L(\omega = \omega_n) = \frac{V_o}{Z_L} = \frac{I_m R}{j\omega_n L} = -jI_m R\sqrt{\frac{C}{L}}. \tag{3.5}$$

The phasor diagram depicting the currents and voltages at the resonant frequency is shown in Figure 3.2. It can be seen that the capacitive current is of the same magnitude but opposite in sign to the inductive current at resonance. Thus, electrical energy is exchanged between the inductor and the capacitor.

3.3 SERIES RESONANT CIRCUIT — A REVIEW

Consider a voltage source $\vec{V}_s(j\omega)$ connected in series with a resistor R, an inductor L, and a capacitor C, as shown in Figure 3.3. As the frequency of the voltage source changes, the current flowing in the circuit is given by

$$\begin{aligned}\vec{I} &= \frac{\vec{V}_s}{R + j(\omega L - (1/\omega C))} \\ &= \frac{\vec{V}_m \angle 0°}{\sqrt{R^2 + (\omega L - (1/\omega C))^2} \angle \tan^{-1}\left(\dfrac{\omega L - (1/\omega C)}{R}\right)}.\end{aligned} \tag{3.6}$$

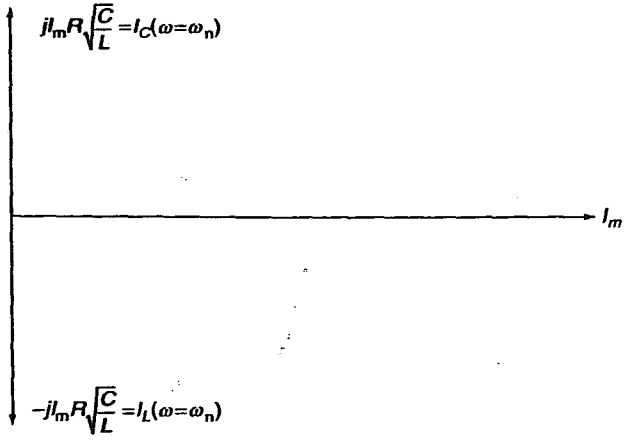


Figure 3.2 Phasor diagram showing the inductor and capacitor currents at the resonant frequency.

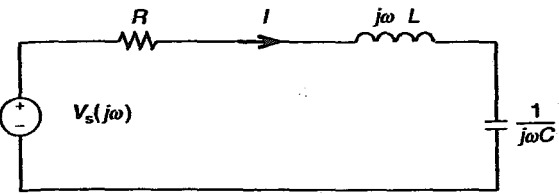


Figure 3.3 A series-resonant circuit.

Again, the resonant frequency in this circuit is defined as the frequency at which the impedance seen by the voltage source is purely resistive. Thus, the resonant frequency, ω_n, is also given by

$$\omega_n = \frac{1}{\sqrt{LC}}. \tag{3.7}$$

At the resonant frequency, the current flowing in the circuit is simply

$$\vec{I}(\omega = \omega_n) = \vec{I}_{\max} = \frac{\vec{V}_m}{R}. \tag{3.8}$$

The voltage across the inductor, $\vec{V}_L(\omega_o)$, is

$$\vec{V}_L(\omega = \omega_n) = (j\omega_n L)\vec{I}_{\max} = \frac{jV_m}{R}\sqrt{\frac{L}{C}} \tag{3.9}$$

and the voltage across the capacitor, $\vec{V}_L(\omega_o)$, is

$$\vec{V}_c(\omega = \omega_n) = \frac{I_{\max}}{j\omega_n C} = -\frac{jV_m}{R}\sqrt{\frac{L}{C}}. \tag{3.10}$$

The phasor diagram depicting the voltages and currents of the series resonant circuit is shown in Figure 3.4. It can be seen that the voltage across the inductor is equal in amplitude, but opposite in phase, to the voltage across the capacitor. Hence, there is a constant exchange of electrical energy between the capacitor and inductor at resonance.

3.4 CLASSIFICATION OF QUASI-RESONANT SWITCHES

The quasi-resonant switch is basically a conventional semiconductor power switching device with an LC tank circuit incorporated into a circuit to shape

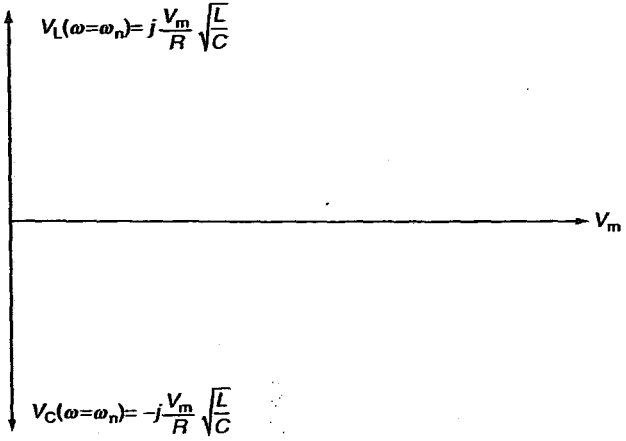


Figure 3.4 Phasor diagram showing the capacitor and inductor voltages at the resonant frequency.

either the voltage across the device or current flowing through it from rectangular pulses into a sinusoidal waveform. The two types of quasi-resonant switches are the current-mode quasi-resonant switch and the voltage-mode quasi-resonant switch. For the current-mode quasi-resonant switch, the inductor of the resonant tank circuit is connected in series with the switching transistor to shape the current flowing through it. There are two current-mode quasi-resonant switch configurations: the L-type and the M-type, as shown in Figure 3.5 [1].

In both cases, the resonant inductor, L_r, is connected in series with the switching transistor, Q_s, while the resonant capacitor, C_r, is connected in parallel with the switching transistor Q_s and the resonant inductor. The resonant inductor and capacitor constitute a series-resonant tank circuit whose resonance occurs during the major portion of the on-time of the switching transistor. The quasi-resonant switch is said to operate in a half-wave mode since the resonant current is not allowed to flow back to the source. If an antiparallel diode, D_1, is connected across the switching transistor, then the quasi-resonant switch is configured to operate in a full-wave mode and the resonant current can flow bi-directionally to both the load and the source.

At turn-on, the switching transistor, Q_s, is first driven into saturation before the current flowing through it gradually rises in a quasi-sinusoidal fashion. The switching transistor is commutated naturally as the current flowing through it tends to oscillate to a negative value. The effect of the resonant switch on the reduction of switching stress and switching loss is

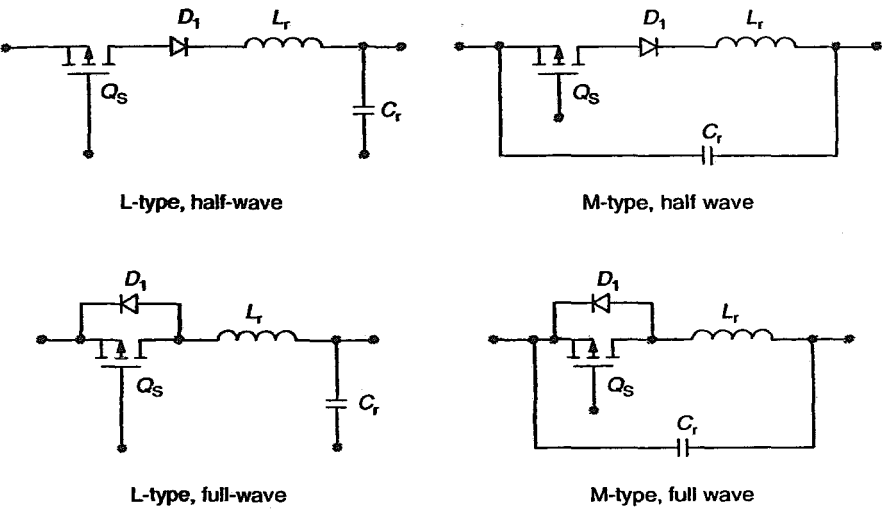


Figure 3.5 Current-mode quasi-resonant switches.

evident from the load-line trajectories shown in Figure 3.6. Path A shows a typical load-line trajectory for inductive switching of a switching transistor with conventional forced turn-off. It traverses through a high-stress region where the switching transistor is subjected to both high voltage and high current simultaneously, whereas the load-line trajectory for inductive switching with a current-mode resonant switch is along either the voltage axis or the current axis, as shown by path B in Figure 3.6. Consequently, the switching stresses and losses in the current-mode quasi-resonant switch are greatly reduced.

The voltage-mode quasi-resonant switch is implemented by connecting a resonant capacitor, C_r, in parallel with the switching transistor, Q_s. The strategy in the voltage-mode quasi-resonant switch is to shape the voltage waveform across the switching transistor during its off-time such that a zero-voltage condition is created before the device is allowed to switch on. Voltage-mode quasi-resonant switches are primarily used to reduce capacitive turn-on loss in power MOSFETs at very high switching frequencies. Nonzero-voltage turn-on in the power MOSFET switching transistor generates substantial noise that interferes with the controller, and reduces its switching speed due to the switching Miller effect. There are also two voltage-mode quasi-resonant switch configurations: the L-type and the M-type as shown in Figure 3.7 [2]. The voltage-mode quasi-resonant switch is said to operate in a half-wave mode when the voltage across the resonant

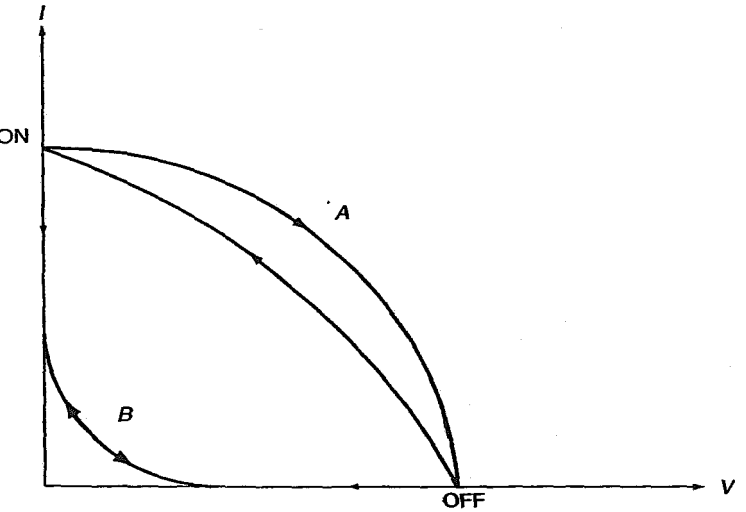


Figure 3.6 Load-line trajectories of a switching transistor: path A, forced switching; path B, resonant switching.

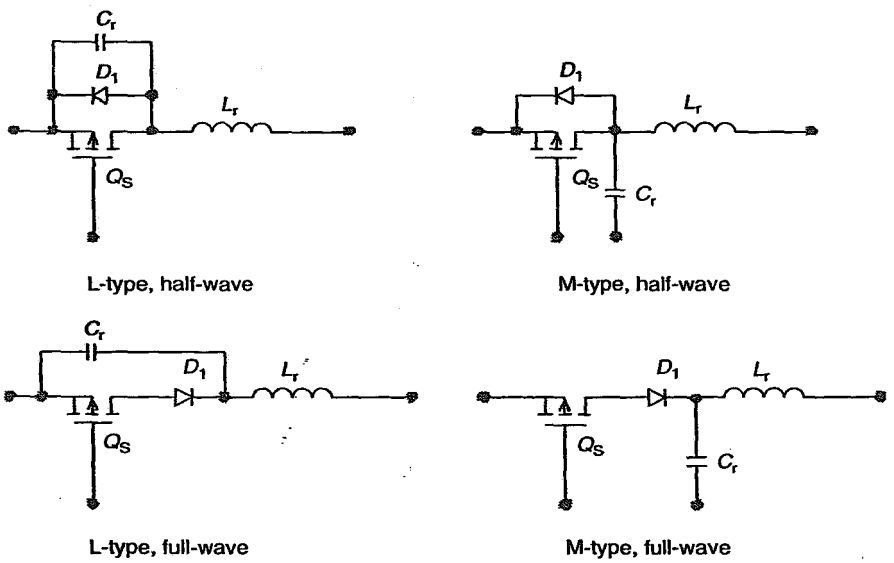


Figure 3.7 Voltage-mode quasi-resonant switches.

capacitor is not allowed to swing to its negative cycle. This is accomplished by a clamping diode, D_1, connected across the resonant capacitor. However, if the diode, D_1, is connected in series with the switching transistor, then the voltage-mode quasi-resonant switch is said to operate in a full-wave mode since the voltage across the resonant capacitor is allowed to swing freely to negative values.

All the basic switching converter topologies can be converted into quasi-resonant converters simply by replacing the switching transistor with either the current-mode or voltage-mode quasi-resonant switch. They are called quasi-resonant converters because there are resonant and nonresonant intervals in the switching waveforms [1,2]. The quasi-resonant switching converter utilizes a voltage-controlled oscillator in its control circuit to change its switching frequency, as shown in Figure 3.8, to maintain a constant output voltage.

3.5 ZERO-CURRENT-SWITCHING QUASI-RESONANT BUCK CONVERTER

A ZCS quasi-resonant converter can be easily implemented by replacing the conventional switching transistor with a current-mode quasi-resonant switch. A half-wave ZCS quasi-resonant buck converter with a L-type switch is shown in Figure 3.9(a) and a full-wave ZCS quasi-resonant buck converter with a L-type switch is shown in Figure 3.9(b). The analysis of this ZCS

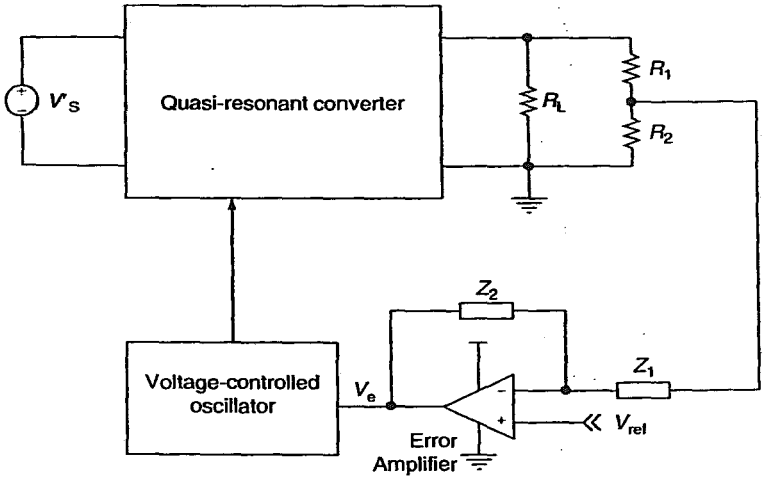


Figure 3.8 Control scheme for a quasi-resonant converter.

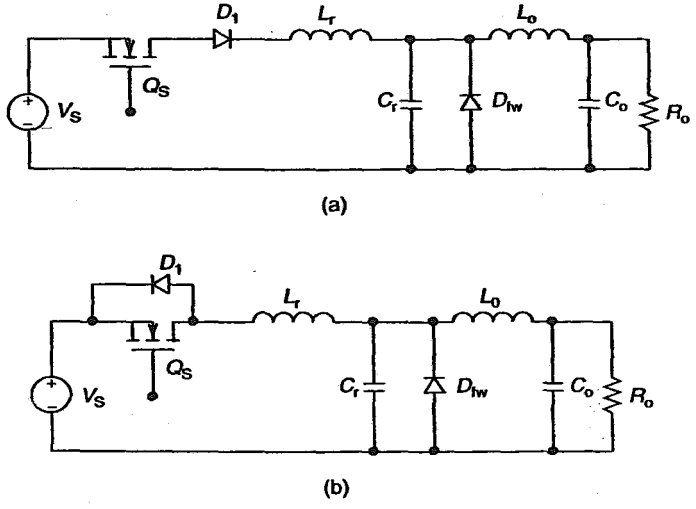


Figure 3.9 Zero-current-switching (ZCS) quasi-resonant buck converter with: (a) a half-wave, L-type switch and (b) a full-wave, L-type switch.

resonant buck converter can be simplified considerably by making the following assumptions [1]. The output inductance, L_o, is assumed to be much larger than the resonant inductance, L_r. The corner frequency of the output filter $L_o - C_o$, f_c, is much lower than the switching frequency. Thus, the output filter $L_o - C_o$ and R_L can be treated as a constant current sink of I_o. The switching devices are ideal semiconductor switches with no forward drops in their on-state and no leakage currents in their off-state. There are also no time delays at both turn-on and turn-off. The resonant inductor and capacitor are ideal circuit elements with no lossy or parasitic elements.

The operation of the ZCS quasi-resonant buck converter can be divided into four modes. Suppose that before the switching transistor is switched on, the freewheeling diode, D_{fw}, carries the steady-state output current of I_o, and the resonant capacitor voltage, $v_{C_r}(t \leq 0)$, is clamped at zero volt by the freewheeling diode. Also, there is no current flowing through the resonant inductor, i.e., $i_{L_r}(0) = 0$.

Mode 1 ($0 < t \leq t_1$)

Mode 1 begins at time $t = 0$ when the switching transistor, Q_s, is switched on. The freewheeling diode, D_{fw}, carries the steady-state output current initially, since the resonant capacitor is clamped at zero volt. Hence, both

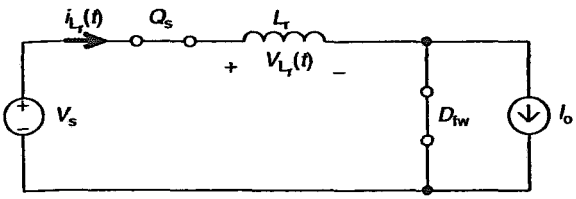


Figure 3.10 Mode 1 equivalent circuit of the ZCS quasi-resonant buck converter.

the switching transistor and the freewheeling diode are switched on during mode 1. The mode 1 equivalent circuit is shown in Figure 3.10. The current flowing through the resonant inductor, $i_{L_r}(t)$, increases linearly from zero to the steady-state output current of I_o. The voltage across the resonant inductor is related to the rate of rise of its current. At the end of mode 1, the voltage across the resonant inductor, $v_{L_r}(t)$, is given by

$$V_s = L_r \frac{I_o}{T_1}. \tag{3.11}$$

The duration of mode 1, T_1, is

$$T_1 = \frac{L_r I_o}{V_s}. \tag{3.12}$$

Thus, mode 1 is characterized by inductor charging and the storage of electrical energy, in magnetic form, in the resonant inductor.

Mode 2 ($t_1 < t \leq t_2$)

Mode 2 begins when the current flowing through the resonant inductor, $i_{L_r}(t)$, reaches the steady-state output current, I_o. The freewheeling diode, D_{fw}, is reverse biased since the resonant capacitor is charged by the difference between the current flowing through the resonant inductor, $i_{L_r}(t)$, and the steady-state output current, I_o (i.e., $i_{L_r}(t) - I_o$). The voltage across the resonant capacitor increases in a quasi-sinusoidal fashion. Figure 3.11 shows the equivalent circuit for mode 2.

The rate of increase of the resonant current is

$$\frac{di_{L_r}}{dt} = \frac{(V_s - v_{C_r}(t))}{L_r}. \tag{3.13}$$

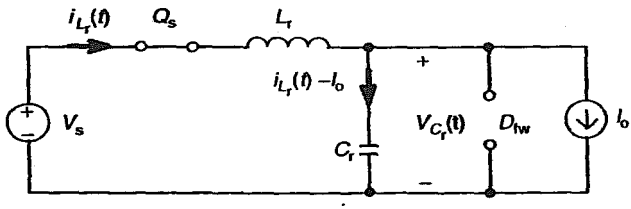


Figure 3.11 Mode 2 equivalent circuit of the ZCS quasi-resonant buck converter.

The rate of increase of the resonant capacitor voltage is

$$\frac{dv_{C_r}}{dt} = \frac{(i_{L_r}(t) - I_o)}{C_r}. \tag{3.14}$$

The initial resonant capacitor voltage is zero (i.e., $v_{C_r}(t_1) = v_{C_r}(0) = 0$), while the initial resonant inductor current, $i_{L_r}(0)$, is I_o. The first-order differential Equations (3.13) and (3.14) can be solved using the two known initial conditions. The expression for the resonant inductor current, $i_{L_r}(t)$, is

$$i_{L_r}(t) = I_o + \frac{V_s}{Z_n} \sin \omega_n t, \tag{3.15}$$

where $Z_n = \sqrt{L_r/C_r}$ is the characteristic impedance and $\omega_n = 1/\sqrt{L_r C_r}$ is the resonant frequency of the resonant tank. The expression for the resonant capacitor voltage, $v_{C_r}(t)$, is

$$v_{C_r}(t) = V_s(1 - \cos \omega_n t). \tag{3.16}$$

The current flowing through the resonant inductor is sinusoidal. However, the voltage across the resonant capacitor increases according to a versine function. Thus, mode 2 is also known as the resonant stage. In the half-wave quasi-resonant buck converter, the switching transistor, Q_s, will be naturally commutated at time t_a when the resonant inductor current, $i_{L_r}(t)$, reduces to zero as shown in Figure 3.12. In a full-wave quasi-resonant buck converter, the resonant inductor current will continue to oscillate and feed energy back to the voltage source, V_s, through the antiparallel diode D_1. The current flowing through diode D_1 oscillates to zero again at time t_b as shown in Figure 3.13.

The duration of this resonant mode, $T_2 = t_2 - t_1$, can be found by setting $i_{L_r}(T_2) = 0$,

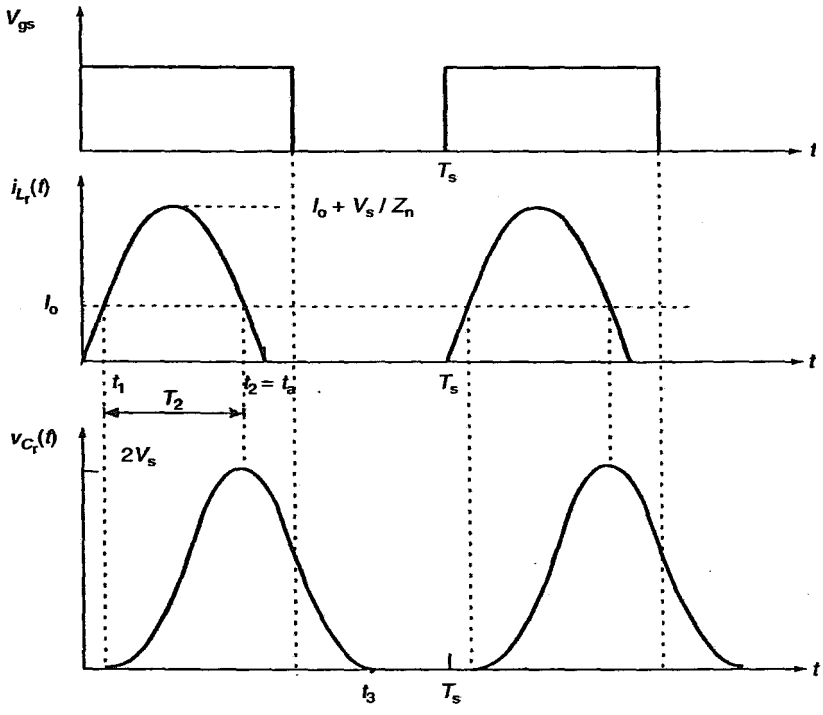


Figure 3.12 Waveforms for the half-wave ZCS quasi-resonant buck converter.

$$i_{L_r}(T_2) = 0 = I_o + \frac{V_s}{Z_n} \sin(\omega_n T_2). \tag{3.17}$$

Rearranging the above equation,

$$\sin(\omega_n T_2) = -\frac{I_o Z_n}{V_s}, \tag{3.18}$$

and the duration of mode 2, T_2, is

$$T_2 = \frac{\sin^{-1}(-I_0 Z_n / V_s)}{\omega_n} = \frac{\alpha}{\omega_n}. \tag{3.19}$$

For the half-wave mode, α takes on values between π and $3\pi/2$. The resonant mode ends at t_a when the resonant inductor current reduces to zero. For the full-wave mode, α adopts values between $3\pi/2$ and 2π.

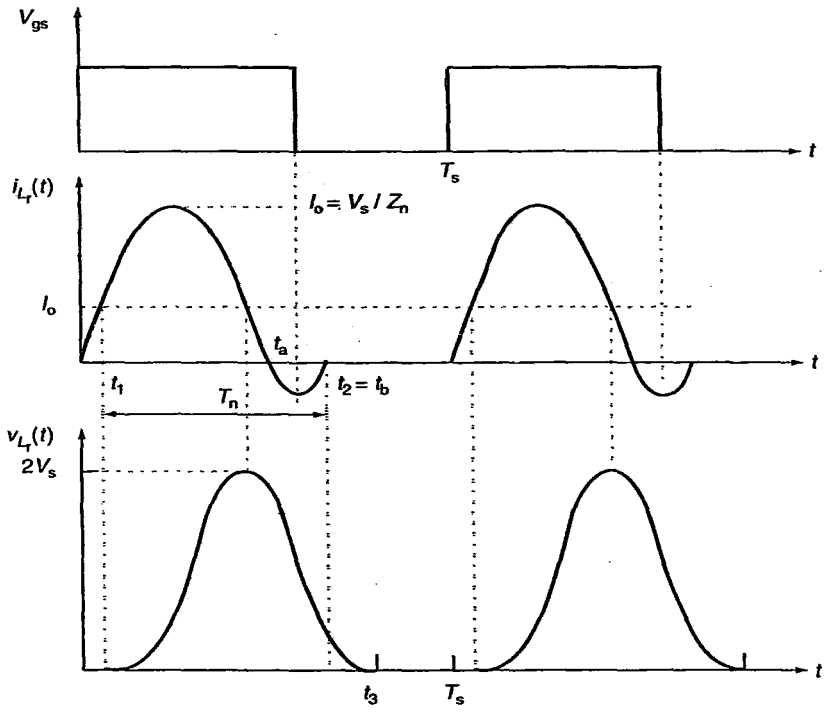


Figure 3.13 Waveforms for the full-wave ZCS quasi-resonant buck converter.

The resonant mode terminates at t_b after the resonant inductor current feeds energy back to the input voltage source. The resonant capacitor still holds some charge even after the current in the resonant inductor is reduced to zero. As such, the freewheeling diode is kept reverse biased at the end of the resonant mode. The resonant capacitor voltage, $v_{C_r}(t)$, at $t = t_2$ is

$$v_{C_r}(t_2) = V_s(1 - \cos\alpha). \tag{3.20}$$

The switching transistor is switched off after t_a for the half-wave mode. For the full-wave mode, the switching transistor is switched off between t_a and t_b. Thus, a zero current condition is created for the switching transistor to switch off in order to reduce turn-off switching losses. The steady-state output current, I_o, must be less than V_s/Z_n for the switching transistor to switch off during zero current.

Mode 3 ($t_2 < t \leq t_3$)

Mode 3 begins after the switching transistor switches off at t_2. The equivalent circuit is shown in Figure 3.14.

The resonant capacitor, C_r, begins to discharge through the output loop and $v_{C_r}(t)$ decreases linearly to zero at time t_3. Thus,

$$C_r \frac{dv_{C_r}}{dt} = -I_0. \tag{3.21}$$

The initial resonant capacitor voltage is given by Equation (3.20). At the end of this mode, the voltage across the resonant capacitor, $v_{C_r}(t_3)$, is zero. Using the boundary conditions, Equation (3.21) can be solved for the duration of mode 3, T_3,

$$T_3 = t_3 - t_2 = C_r \frac{v_{C_r}(t_3) - v_{C_r}(t_2)}{-I_0} = C_r \frac{V_s(1 - \cos\alpha)}{I_0}. \tag{3.22}$$

The drain-to-source voltage of the switching transistor increases during mode 3. At the end of mode 3 (i.e., at t_3), the drain-to-source voltage of the switching transistor is equal to the input voltage, V_s, as the switching transistor is completely switched off.

Mode 4 ($t_3 < t \leq T_s$)

Mode 4 begins when the voltage across the resonant capacitor reduces to zero at time $t = t_3$. The freewheeling diode, D_{fw}, switches on and the output current now flows through D_{fw}. The equivalent circuit is shown in Figure 3.15.

The duration of mode 4, T_4, is

$$T_4 = T_s - T_3 - T_2 - T_1, \tag{3.23}$$

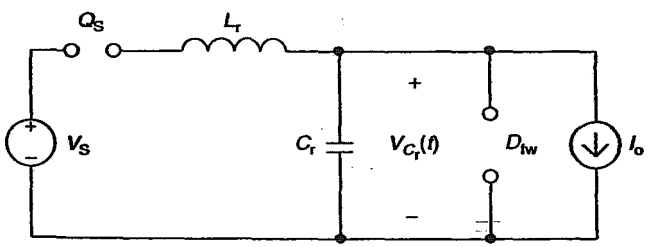


Figure 3.14 Mode 3 equivalent circuit of the ZCS quasi-resonant buck converter.

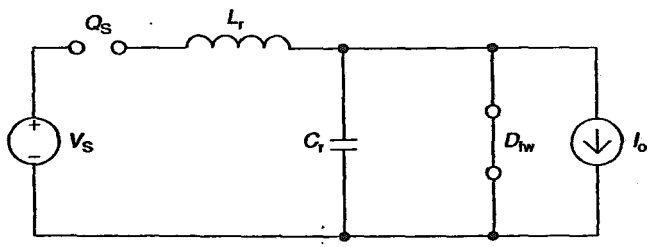


Figure 3.15 Mode 4 equivalent circuit of the ZCS quasi-resonant buck converter.

where T_s is the switching period. By controlling the freewheeling time interval, T_4, the output voltage, V_a, can be regulated.

The voltage conversion ratio of the full-wave ZCS quasi-resonant buck converter can be found by imposing the constant volt-second relationship on the output inductor, L_o, since the average voltage across the output inductor is zero under steady-state conditions. Since the resonant capacitor voltage waveform is approximately $V_s(1 - \cos \omega_n t)$ during the interval between t_3 and t_1, its average value is approximately equal to the input voltage, V_s. The resonant period is approximately $T_n = t_3 - t_1$. During this time interval, the average voltage across the output inductor is $(V_s - V_a)$. The voltage across the output inductor during the remaining switching period, i.e., $T_s - T_n$, is $-V_a$. From the constant volt-second relationship,

$$(V_s - V_a)T_n - V_a(T_s - T_n) = 0. \tag{3.24}$$

Rearranging this equation, the voltage conversion ratio, V_a/V_s, for a full-wave ZCS quasi-resonant buck converter is

$$\frac{V_a}{V_s} = \frac{T_n}{T_s} = \frac{f_s}{f_n}. \tag{3.25}$$

Thus, the output voltage of a ZCS quasi-resonant buck converter is regulated by changing the switching frequency. It is obvious that the switching frequency, f_s, must be less than the resonant frequency, f_n.

In a half-wave ZCS quasi-resonant buck converter, the output voltage is very sensitive to load variations as shown in Figure 3.16 [1]. This is because the only means for the half-wave quasi-resonant buck converter to regulate the output voltage is by varying the switching frequency since it takes a longer time to discharge the tank energy to the load in a light load situation. The voltage conversion ratio of the full-wave ZCS quasi-resonant buck converter is insensitive to load variations. This is because the excess tank

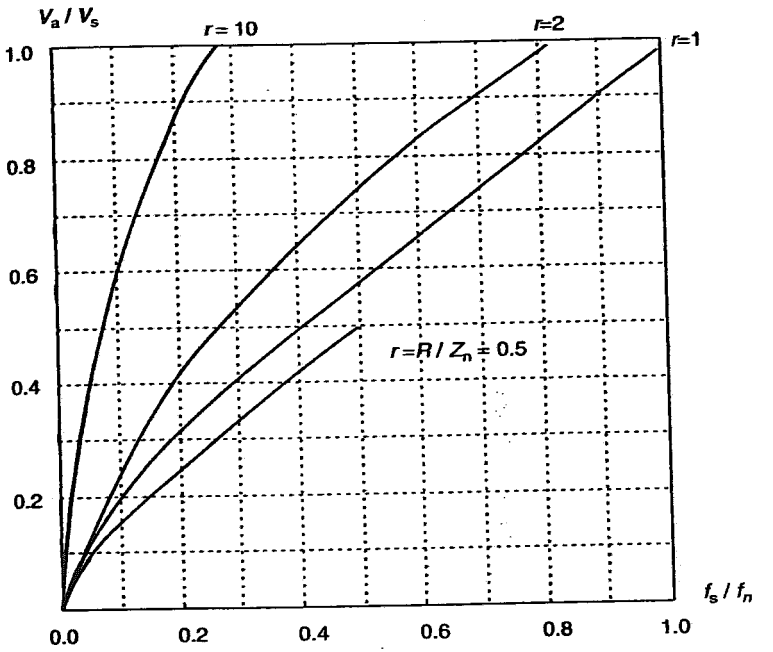


Figure 3.16 Voltage conversion ratio for the half-wave ZCS quasi-resonant buck converter. (From K.H. Liu, R. Oruganti, and F.C. Lee. Resonant Switches—Topologies and Characteristics, IEEE Power Electronics Specialists Conference 1985, Record: 106, 1985. With permission.)

energy in the full-wave ZCS quasi-resonant buck converter is allowed to feed back to the input source during a small output load current requirement. When the required output current is large, the time interval to charge the resonant inductor is longer, and consequently, the resonant inductor is charged to a higher value according to the requirement of the load as shown in Figure 3.17.

Since most of the stored magnetic energy in the resonant inductor is used to satisfy the output current requirement, very little excess tank energy is fed back to the input source. Consequently, the magnitude of the resonant inductor current is higher in the first half-cycle during the resonant mode, and is lower during the second half-cycle when the excess energy is fed back to the input source as shown in Figure 3.17(a). Conversely, when the required output current is small, the magnitude of the current flowing through the resonant inductor is small during the resonant mode and is larger during the second half-cycle as shown in Figure 3.17(b). This is because a larger amount

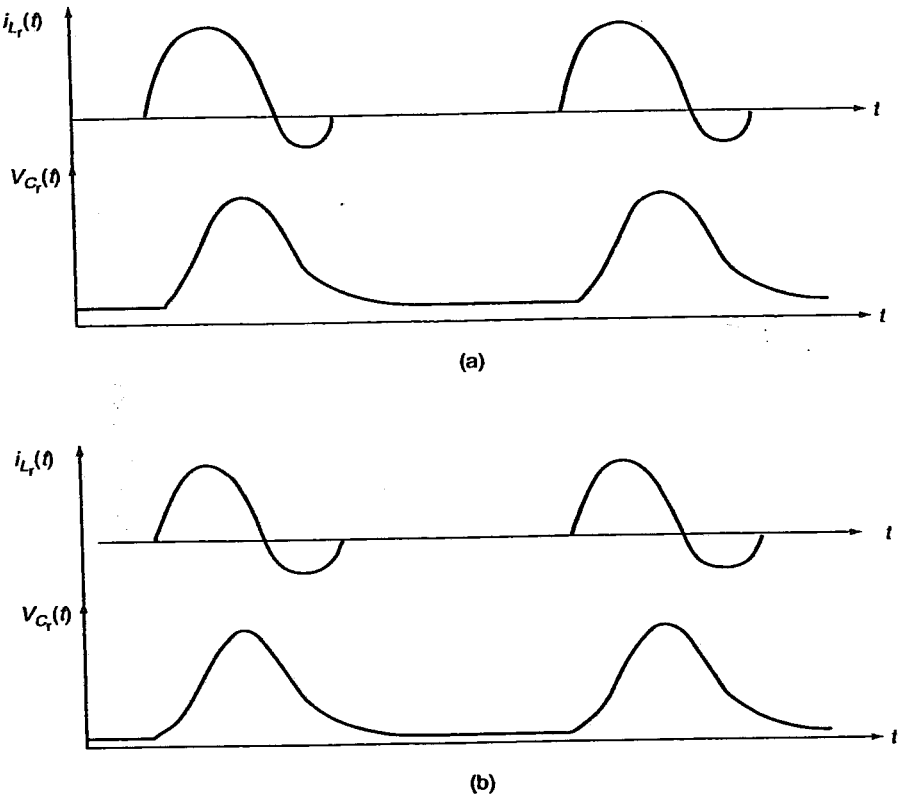


Figure 3.17 Resonant inductor current and resonant capacitor voltage for (a) heavy load and (b) light load. (From K.H. Liu, R. Oruganti, and F.C. Lee. Resonant Switches — Topologies and Characteristics, IEEE Power Electronics Specialists Conference 1985, Record: 106, 1985. With permission.)

of stored energy is fed back to the input source. Thus, the full-wave ZCS quasi-resonant buck converter is able to regulate its output voltage against load variations without a large change in the switching frequency.

Example 3.1. The zero-current-switching quasi-resonant buck converter shown in Figure 3.9(b) has an input voltage of 12 V. The values of the resonant inductor, L_r, and resonant capacitor, C_r, are 2 μH and 79 nF, respectively. The average output voltage is 9 V across a 9-Ω resistor. The output inductor and output capacitor are 10 mH and 100 μF, respectively. Determine (a) the switching frequency, f_s, (b) the duration that the resonant

inductor is charged, (c) the peak current in the resonant inductor, and (d) the peak voltage across the resonant capacitor.

Solution.

(a) The resonant frequency is

$$f_n = \frac{1}{2\pi}\frac{1}{\sqrt{LC}} = \frac{1}{2\pi}\frac{1}{\sqrt{2\times 10^{-6}(79\times 10^{-9})}} = 400\,\text{kHz}.$$

From Equation (3.25), the switching frequency, f_s, is

$$f_s = \frac{V_a}{V_s}f_n = \frac{9}{12}400\,\text{kHz} = 300\,\text{kHz}.$$

(b) The average output current is

$$I_o = \frac{V_a}{R} = \frac{9}{9} = 1\ \text{A}.$$

From Equation (3.12), the resonant inductor is charged for

$$T_1 = \frac{L_r I_o}{V_s} = \frac{2\times 10^{-6}(1)}{12} = 0.167\ \mu\text{s}.$$

(c) From Equation (3.15), the peak current in the resonant inductor is

$$I_{L_r,\max} = I_o + \frac{V_s}{Z_n} = 1 + \frac{12}{\sqrt{(L_r/C_r)}} = 3.385\ \text{A}.$$

(d) From Equation (3.16), the expression for the voltage across the resonant capacitor is

$$V_{C_r} = V_s\left[1 - \cos\frac{t}{\sqrt{L_r C_r}}\right] = 12[1 - \cos(2.516\times 10^6 t)]$$

The peak voltage across the resonant capacitor is

$$V_{C_r,\max} = 12(1+1) = 24\,\text{V}.$$

3.6 ZERO-CURRENT-SWITCHING QUASI-RESONANT BOOST CONVERTER

The circuit schematic of a full-wave, ZCS quasi-resonant boost converter is shown in Figure 3.18. The analysis of this converter can be simplified by

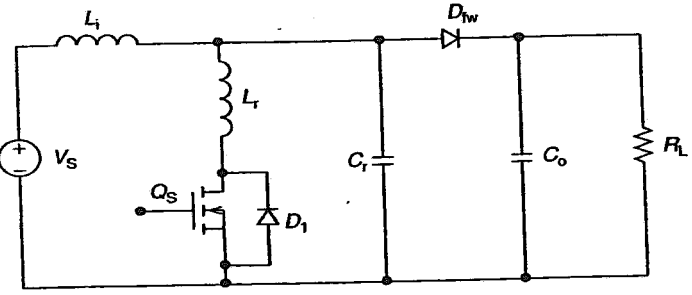


Figure 3.18 Circuit schematic of a full-wave ZCS quasi-resonant boost converter.

adopting the same assumptions made in Section 3.5. Furthermore, the input of the boost converter is treated as a constant-current source, I_s, supplying power to a constant-voltage load, V_a.

The operation of the ZCS quasi-resonant boost converter can also be divided into four modes. Suppose before the switching transistor, Q_s, is switched on, the freewheeling diode is conducting, and consequently, the resonant capacitor is charged to the output voltage, V_a.

Mode 1 ($0 < t \leq t_1$)

Mode 1 begins when the switching transistor, Q_s, is switched on at $t=0$. The equivalent circuit is shown in Figure 3.19. The current flowing through the resonant inductor, $i_{L_r}(t)$, increases linearly from zero to the steady-state input current I_s. The voltage across the resonant inductor is related to the rate of rise of its current. At the end of mode 1, the voltage across the resonant inductor, $v_{L_r}(t)$, is given by

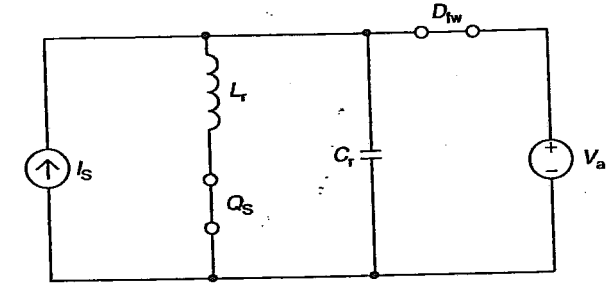


Figure 3.19 Mode 1 equivalent circuit of the ZCS quasi-resonant boost converter.

$$V_a = L_r \frac{I_s}{T_1}. \tag{3.26}$$

The duration of mode 1, T_1, is

$$T_1 = \frac{L_r I_s}{V_a}. \tag{3.27}$$

Thus, mode 1 is characterized by the storage of electrical energy in the resonant inductor in magnetic form.

Mode 2 ($t_1 < t \leq t_2$)

Mode 2 begins when the current flowing through the resonant inductor reaches the input current, I_s. The freewheeling diode is reverse biased as the resonant capacitor discharges its stored energy into the resonant inductor. The equivalent circuit is shown in Figure 3.20. The voltage across the resonant capacitor, $v_{C_r}(t)$, decreases sinusoidally according to

$$C_r \frac{dv_{C_r}(t)}{dt} = I_s - i_{L_r}(t). \tag{3.28}$$

The rate of increase of the resonant inductor current, $(di_{L_r}(t)/dt)$, is

$$\frac{di_{L_r}(t)}{dt} = \frac{v_{C_r}(t)}{L_r}. \tag{3.29}$$

The above first-order differential equations can be solved using the two known initial conditions: $i_{L_r}(t_1) = i_{L_r}(0) = I_s$ and $v_{C_r}(t_1) = v_{C_r}(0) = V_a$. The expression for the resonant inductor current, $i_{L_r}(t)$, is

$$i_{L_r}(t) = I_s + \frac{V_a}{Z_n} \sin(\omega_n t) \tag{3.30}$$

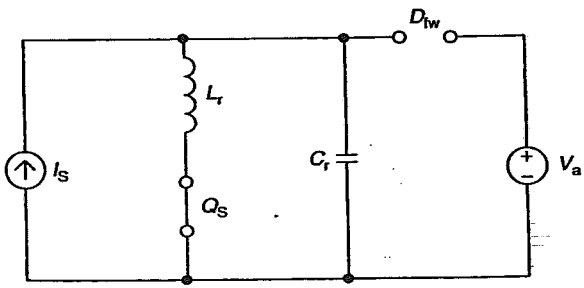


Figure 3.20 Mode 2 equivalent circuit of the ZCS quasi-resonant boost converter.

where $Z_n = \sqrt{L_r/C_r}$ is the circuit characteristic impedance and $\omega_n = 1/\sqrt{L_r C_r}$ is the resonant frequency. The expression for the resonant capacitor voltage, $v_{C_r}(t)$, is

$$v_{C_r}(t) = V_a \cos(\omega_n t). \tag{3.31}$$

Thus, both the current flowing through the resonant inductor and the voltage across the resonant capacitor are sinusoidal. Hence, electrical energy is exchanged between the resonant inductor and capacitor. Mode 2 is also known as the resonant mode. The resonant inductor current continues to swing to its negative cycle when it feeds energy back to the input source as shown in Figure 3.21. At the beginning of this mode, the resonant capacitor discharges its energy to the resonant inductor. However, as the resonant inductor current decreases below the steady-state input current, I_s, the resonant capacitor voltage increases toward the output voltage, V_a. The duration of this resonant mode, $T_2 = t_2 - t_1$, can be found by setting $iL_r(T_2) = 0$:

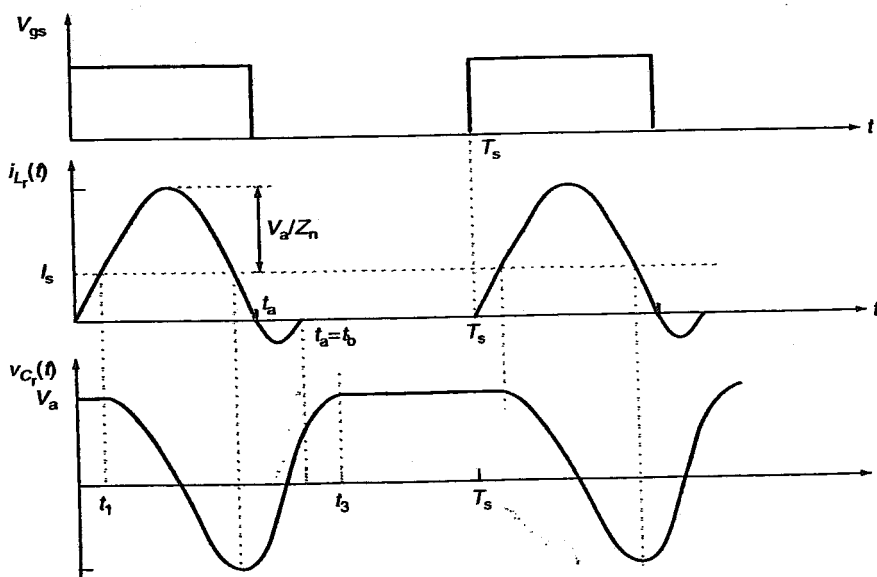


Figure 3.21 Waveforms for the full-wave ZCS quasi-resonant boost converter.

$$i_{L_r}(T_2) = 0 = I_s + \frac{V_a}{Z_n} \sin(\omega_n T_2). \tag{3.32}$$

The duration for mode 2, T_2, is

$$T_2 = \frac{\sin^{-1}(-(Z_n I_s / V_a))}{\omega_n} = \frac{\alpha}{\omega_n} \tag{3.33}$$

where α takes on values between 1.5π and 2π. The resonant mode terminates at $t_2 = t_b$ after the resonant inductor has completely fed its stored energy back to the input source. After t_a, the switching transistor, Q_s, can now be switched off. Thus, a zero-current condition is created for the switching transistor to switch off. The input current, I_s, should be smaller than V_a/Z_n for the switching transistor to switch off during zero current.

Mode 3 ($t_2 < t \leq t_3$)

Mode 3 begins after the resonant inductor current decreases to zero from its negative peak at time t_2. The switching transistor, Q_s, switches off and its drain-to-source voltage continues to rise during this interval. The equivalent circuit is shown in Figure 3.22.

The resonant capacitor continues to charge towards the output voltage, V_a, by the input current, I_s. The rate of increase of the capacitor voltage is

$$\mathrm{d}\frac{v_{C_r}(t)}{\mathrm{d}t} = \frac{I_s}{C_r}. \tag{3.34}$$

The initial resonant capacitor voltage is

$$v_{C_r}(t_2) = V_a \cos(\alpha). \tag{3.35}$$

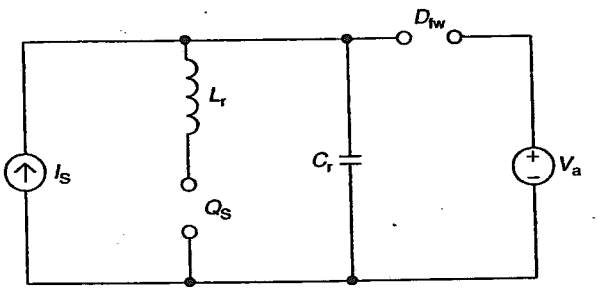


Figure 3.22 Mode 3 equivalent circuit of the ZCS quasi-resonant boost converter.

The duration of mode 3, T_3, is

$$T_3 = \frac{C_r V_a (1 - \cos \alpha)}{I_s}. \tag{3.36}$$

Mode 4 ($t_3 < t \leq T_s$)

Mode 4 begins when the resonant capacitor voltage reaches V_a at t_3. The freewheeling diode, D_{fw}, is forward biased and switched on. The equivalent circuit is shown in Figure 3.23. The duration of mode 4 is

$$T_4 = T_s - T_1 - T_2 - T_3, \tag{3.37}$$

where T_s is the switching period.

The voltage conversion ratio of the full-wave ZCS quasi-resonant boost converter can be found by imposing the constant volt-second relationship on the input inductor, L_i, since the average voltage across it is zero for steady-state operation. The average voltage across the input inductor during the time interval between t_1 and t_3 (i.e., the resonant period T_n) is V_s since the average V_{C_r} is zero. During the remaining time interval (i.e., $T_s - T_n$), the average voltage across the input inductor is $(V_s - V_a)$. Thus,

$$V_s T_n + (T_s - T_n)(V_s - V_a) = 0. \tag{3.38}$$

The voltage conversion ratio for the full-wave ZCS quasi-resonant boost converter is

$$\frac{V_a}{V_s} = \frac{1}{(1 - (f_s/f_n))}. \tag{3.39}$$

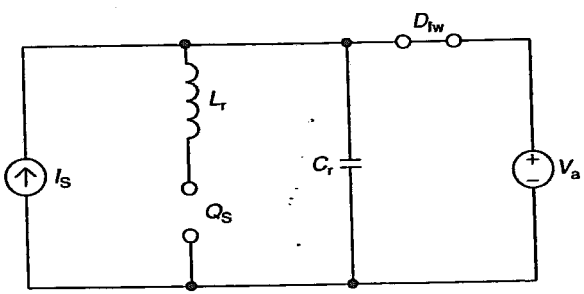


Figure 3.23 Mode 4 equivalent circuit of the ZCS quasi-resonant boost con verter.

Note that this voltage conversion ratio is similar to that of the conventional boost switching converter if the ratio of the switching frequency to the resonant frequency is replaced by its duty cycle, D. The voltage conversion ratio versus f_s/f_n relationship for a full-wave ZCS quasi-resonant boost converter is shown in Figure 3.24. It should be noted that the switching frequency, f_s, must be smaller than the resonant frequency. In a half-wave ZCS quasi-resonant boost converter, the output voltage is very sensitive to load variations. Thus, the only means to regulate its output voltage is to change the switching frequency. On the other hand, the full-wave ZCS quasi-resonant boost converter is able to regulate its output voltage against load variation without a large change in switching frequency.

Example 3.2. The zero-current-switching quasi-resonant boost converter shown in Figure 3.18 has an input voltage of 12 V. The values of the resonant inductor, L_r, and resonant capacitor, C_r, are 2 μH and 79 nF, respectively. The output voltage is 15 V across a 10-Ω resistor. The output inductor and output capacitor are 10 mH and 100 μF, respectively. Determine (a) the switching frequency, f_s, (b) the duration that the resonant inductor is charged, (c) the peak current in the resonant inductor, and (d) the peak voltage across the resonant capacitor.

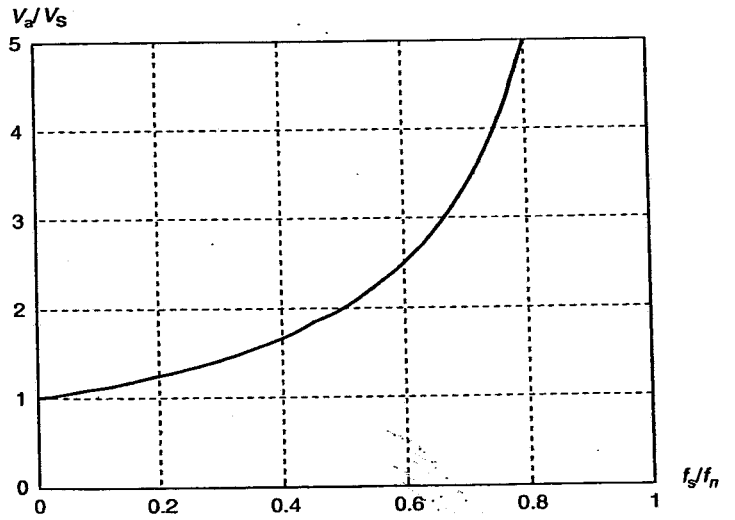


Figure 3.24 Voltage conversion ratio versus f_s/f_n for a full-wave ZCS quasi-resonant boost converter.

Solution.

(a) From Equation (3.39), the switching frequency, f_s, is

$$f_s = \left(1 - \frac{V_s}{V_a}\right) f_n = \left(1 - \frac{12}{15}\right) 400\,\text{kHz} = 80\,\text{kHz}.$$

(b) The average output current is

$$I_o = \frac{V_a}{R} = \frac{15}{10} = 1.5\,\text{A}.$$

Assuming a lossless converter, the input current, I_s, is

$$I_s = \frac{V_a I_o}{V_s} = \frac{15(1.5)}{12} = 1.875\,\text{A}.$$

From Equation (3.27), the duration that the resonant inductor is charged is

$$T_1 = \frac{L_r I_s}{V_a} = \frac{2 \times 10^{-6}(1.875)}{15} = 0.25\,\mu\text{s}.$$

(c) From Equation (3.30), the peak current in the resonant inductor is

$$I_{L_r,\max} = I_s + \frac{V_a}{Z_n} = 1.875 + \frac{15}{\sqrt{(2 \times 10^{-6}/79 \times 10^{-9})}} = 4.86\,\text{A}.$$

(d) From Equation (3.31), the peak voltage across the resonant capacitor is

$$V_{C_r,\max} = V_a = 15\,\text{V}.$$

3.7 ZERO-VOLTAGE-SWITCHING QUASI-RESONANT BUCK CONVERTER

The circuit schematic of a full-wave ZVS quasi-resonant buck converter is shown in Figure 3.25. The analysis of this converter can be simplified by using the same assumptions made for the ZCS quasi-resonant buck converter. The operation of the ZVS quasi-resonant buck converter can be divided into four modes. Suppose that before the switching transistor, Q_s, is switched off, the resonant inductor, L_r, carries the load current, I_o. The resonant capacitor, C_r, is clamped at zero volt and the freewheeling diode, D_{fw}, is switched off.

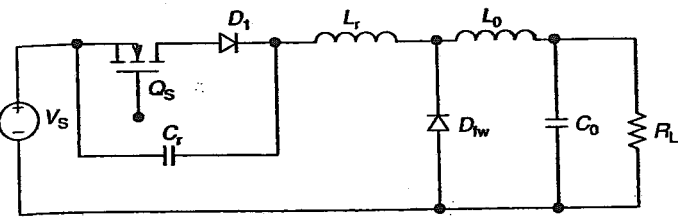


Figure 3.25 Circuit schematic of a full-wave ZVS quasi-resonant buck converter.

Mode 1 ($0 < t \leq t_1$)

Mode 1 begins when the switching transistor is switched off at time $t = 0$. The equivalent circuit is shown in Figure 3.26. The resonant capacitor begins its charging process as soon as the switching transistor is switched off. At the end of mode 1, the current flowing through the resonant capacitor is

$$I_o = C_r \frac{V_s}{T_1}. \tag{3.40}$$

The duration of mode 1, T_1, is

$$T_1 = \frac{C_r V_s}{I_o}. \tag{3.41}$$

Thus, mode 1 is characterized by the capacitor charging and the storage of electrical energy in electrostatic form in the resonant capacitor. It should be noted that both the switching transistor and the freewheeling diode remain off during mode 1.

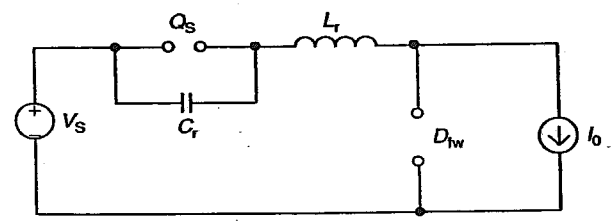


Figure 3.26 Mode 1 equivalent circuit of the full-wave ZVS quasi-resonant buck converter.

Mode 2 ($t_1 < t \leq t_2$)

Mode 2 begins when the voltage across the resonant capacitor reaches the input supply voltage, V_s, at time t_1. The freewheeling diode, D_{fw}, is switched on and the current flowing in the resonant inductor decreases in a sinusoidal fashion. Figure 3.27 shows the equivalent circuit for mode 2. The rate of decrease of the resonant inductor current is

$$\frac{di_{L_r}}{dt} = V_s - \frac{v_{C_r}(t)}{C_r}. \tag{3.42}$$

The rate of increase of the resonant capacitor voltage is

$$\frac{dv_{C_r}}{dt} = \frac{i_{L_r}(t)}{C_r}. \tag{3.43}$$

The initial resonant inductor current, $i_{L_r}(t_1)$, is I_o, while the initial resonant capacitor voltage, $v_{C_r}(t_1)$, is V_s. The above first-order differential equations can be solved using the two known initial conditions. The expression for the resonant inductor current, $i_{L_r}(t)$, is

$$i_{L_r}(t) = I_o \cos \omega_n t \tag{3.44}$$

and the resonant capacitor voltage, $v_{C_r}(t)$, is

$$v_{C_r}(t) = V_s + Z_n I_o \sin \omega_n t, \tag{3.45}$$

where $Z_n = \sqrt{L_r/C_r}$ is the circuit characteristic impedance and $\omega_n = 1/\sqrt{L_r C_r}$ is the resonant frequency. Mode 2 is also known as the resonant mode. The voltage across the resonant capacitor continues to swing to its negative cycle as it feeds energy back to the input source as shown in Figure 3.28. The current flowing through the resonant inductor decreases to its minimum value as the voltage across the resonant capacitor

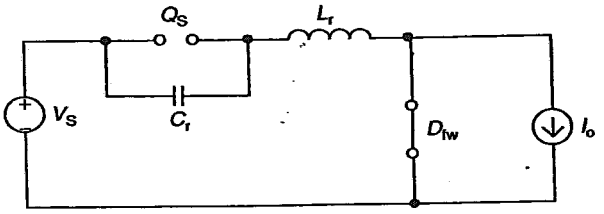


Figure 3.27 Mode 2 equivalent circuit of the full-wave ZVS quasi-resonant buck converter.

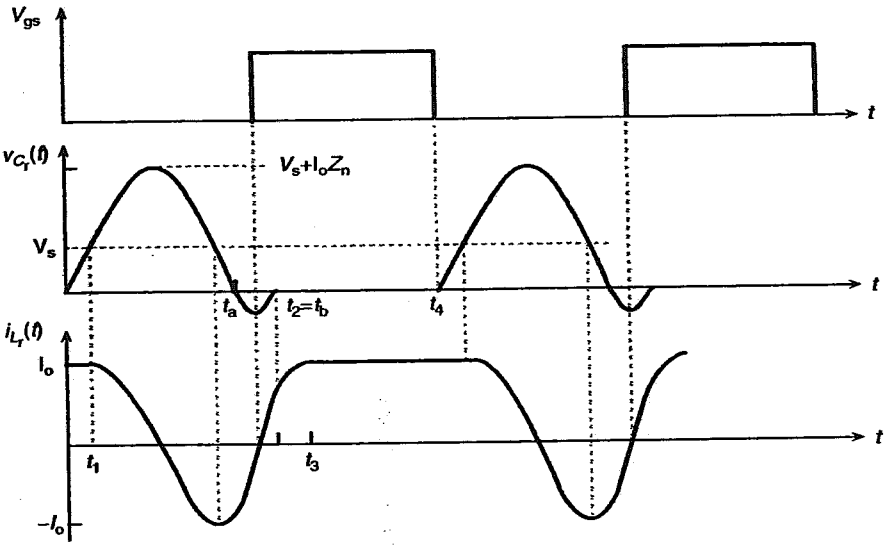


Figure 3.28 Waveforms of the full-wave ZVS quasi-resonant buck converter.

is again at V_s. After this, the current in the resonant inductor increases toward I_o. The duration of this resonant mode, $T_2 = t_2 - t_1$, can be found by setting $v_{C_r}(T_2) = 0$:

$$v_{C_r}(T_2) = V_s + Z_n I_o \sin(\omega_n T_2) = 0. \tag{3.46}$$

Thus, the duration of mode 2, T_2, is

$$T_2 = \frac{\sin^{-1}(-(V_s/Z_n I_o))}{\omega_n} = \frac{\alpha}{\omega_n} \tag{3.47}$$

where α takes on values between 1.5π and 2π. The resonant mode terminates at t_2, after the resonant capacitor has completely fed its stored energy back to the input source. The switching transistor should be switched on during the negative part of the resonant capacitor voltage. Otherwise, the resonant capacitor will begin to recharge and the switching transistor will lose the opportunity to switch on under zero-voltage condition. It should be noted that the steady-state load current, I_o, must be greater than (V_s/Z_o) for the switching transistor to switch on at zero voltage.

Mode 3 ($t_2 < t \leq t_3$)

Mode 3 begins after the resonant capacitor voltage decreases to zero from its negative peak at time t_2. The equivalent circuit is shown in Figure 3.29. The resonant inductor current continues to increase toward the steady-state output current, I_o. The rate of increase of the resonant inductor current is

$$\mathrm{d}\frac{i_{L_r}}{\mathrm{d}t} = \frac{V_s}{L_r}. \tag{3.48}$$

The current flowing through the resonant inductor at the beginning of this mode is

$$i_{L_r}(t_3) = I_o \cos(\alpha). \tag{3.49}$$

The duration of mode 3, T_3, is

$$T_3 = \frac{L_r I_o}{V_s}(1 - \cos\alpha). \tag{3.50}$$

Mode 4 ($t_3 < t \leq T_s$)

Mode 4 begins when the current in the resonant inductor reaches the steady-state output current, I_o, at time t_3. The freewheeling diode is switched off at time t_3. The equivalent circuit is shown in Figure 3.30. The duration of this mode is

$$T_4 = T_s - T_1 - T_2 - T_3, \tag{3.51}$$

where T_s is the switching period.

The voltage conversion ratio of the full-wave ZVS quasi-resonant buck converter can be solved by imposing the constant volt-second relationship on the output inductor, L_o. The average voltage across the output inductor

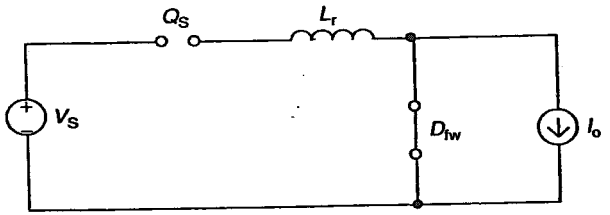


Figure 3.29 Mode 3 equivalent circuit of the full-wave ZVS quasi-resonant buck converter.

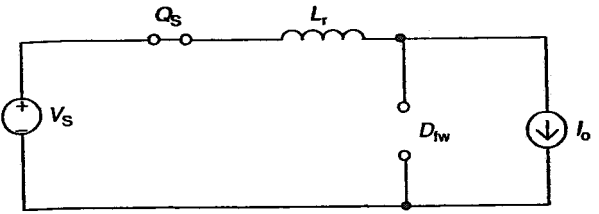


Figure 3.30 Mode 4 equivalent circuit of the full-wave ZVS quasi-resonant buck converter.

during the time interval between t_1 and t_3, or $T_n = t_3 - t_1$ is $-V_a$. During the remaining time interval (i.e., $T_s - T_n$), the average voltage across the output inductor is approximately $(V_s - V_a)$. Thus

$$-V_a T_n + (V_s - V_a)(T_s - T_n) = 0. \tag{3.52}$$

The voltage conversion ratio of the full-wave ZVS quasi-resonant buck converter is

$$\frac{V_a}{V_s} = \left(1 - \frac{f_s}{f_n}\right). \tag{3.53}$$

A plot of the voltage conversion ratio versus f_s/f_n is shown in Figure 3.31. As can be seen, it is very insensitive to any load variations. Note that the voltage conversion ratio of the ZVS resonant buck converter is quite different from that of the ZCS quasi-resonant buck converter and the conventional buck converter. Since the resonant mode occurs during the off-time of the switching transistor, it is expected that the voltage conversion ratio is related to this period. As in the previous two ZCS quasi-resonant converters, the switching frequency of the ZVS quasi-resonant converter must be less than its resonant frequency. The voltage conversion ratio of the half-wave ZVS quasi-resonant buck converter is also very sensitive to load variations. Thus, the half-wave ZVS quasi-resonant buck converter requires a larger change in switching frequency to regulate its output voltage compared to the full-wave, ZVS, quasi-resonant buck converter.

Example 3.3. The ZVS quasi-resonant buck converter shown in Figure 3.25 has an input voltage of 12 V and a resistive load of 2Ω. The values of the resonant inductor, L_r, and resonant capacitor, C_r, are 2 μH and 79 nF, respectively. The switching frequency is 200 kHz. The output inductor and output capacitor are 10 mH and 100 μF, respectively. Determine (a) the average output voltage, V_a, (b) the duration that the resonant capacitor is

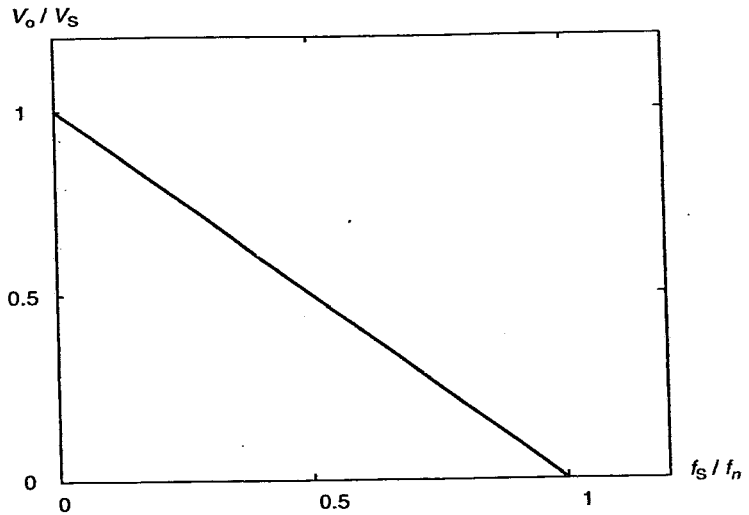


Figure 3.31 Voltage conversion ratio versus f_s/f_n for the full-wave ZVS quasi-resonant buck converter.

charged, (c) the peak voltage across the resonant capacitor, and (d) the expression for the resonant inductor current.

Solution.

(a) From Equation (3.53), the average output voltage is

$$V_a = \left(1 - \frac{f_s}{f_n}\right) V_s = \left(1 - \frac{200\text{k}}{400\text{k}}\right) 12 = 6\,\text{V}.$$

(b) The average output current is

$$I_o = \frac{V_a}{R} = \frac{6}{2} = 3\,\text{A}.$$

From Equation (3.41), the duration that the resonant capacitor is charged is

$$T_1 = \frac{C_r V_s}{I_o} = \frac{79 \times 10^{-9}(12)}{3} = 0.316\,\mu\text{s}.$$

(c) From Equation (3.45), the peak voltage across the resonant capacitor is

$$V_{Cr,\max} = V_s + Z_n I_o = V_s + \frac{V_a}{R}\sqrt{\frac{L_r}{C_r}} = 12 + \frac{6}{2}\sqrt{\frac{2 \times 10^{-6}}{79 \times 10^{-9}}} = 27.1\,\text{V}$$

(d) From Equation (3.44), the expression for the resonant inductor current is

$$i_{L_r} = I_o \cos(\omega_n t) = 3\cos\left(\frac{t}{\sqrt{L_r C_r}}\right) = 3\cos(2.516 \times 10^6)t \text{ A}.$$

3.8 ZERO-VOLTAGE-SWITCHING QUASI-RESONANT BOOST CONVERTER

The circuit schematic of a full-wave ZVS quasi-resonant boost converter is shown in Figure 3.32. The same assumptions made for the ZCS quasi-resonant boost converter are valid here. Suppose that before the switching transistor, Q_s, is switched off, it carries the input current, I_s. Also, the freewheeling diode, D_{fw}, is switched off.

Mode 1 ($0 < t \leq t_1$)

Mode 1 begins when the switching transistor, Q_s, is switched off at $t = 0$. The resonant capacitor, C_r, is charged up and its voltage increases according to

$$C_r \frac{dv_{C_r}}{dt} = I_s. \tag{3.54}$$

The duration of mode 1, T_1, is

$$T_1 = C_r \frac{V_a}{I_s}. \tag{3.55}$$

Thus, mode 1 is characterized by the charging of the resonant capacitor and the storage of energy in electrostatic form. Both the switching transistor and the freewheeling diode are switched off during mode 1 as shown by the equivalent circuit shown in Figure 3.33.

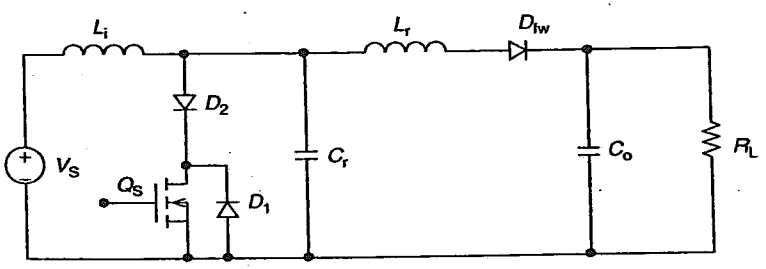


Figure 3.32 Circuit schematic of a full-wave ZVS quasi-resonant boost converter.

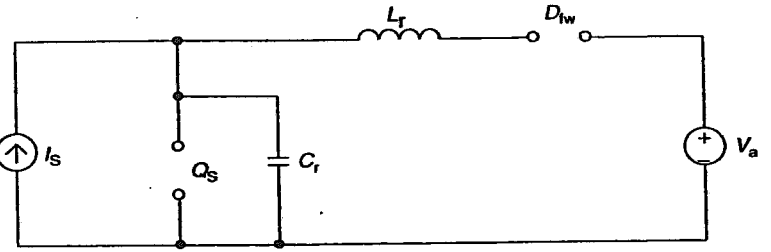


Figure 3.33 Mode 1 equivalent circuit of the full-wave ZVS quasi-resonant boost converter.

Mode 2 ($t_1 < t \leq t_2$)

Mode 2 commences when the voltage across the resonant capacitor reaches the steady-state output voltage, V_a. The freewheeling diode, D_{fw}, is forward-biased and switched on. Current starts to flow through the resonant inductor. The equivalent circuit is shown in Figure 3.34.

The rate of increase of the resonant inductor current, $i_{L_r}(t)$, is

$$\frac{\mathrm{d}i_{L_r}}{\mathrm{d}t} = \frac{v_{C_r}(t) - V_a}{L_r}. \tag{3.56}$$

The voltage across the resonant capacitor continues to increase beyond the steady-state output voltage, V_a, according to

$$C_r \frac{\mathrm{d}v_{C_r}}{\mathrm{d}t} = I_s - i_{L_r}(t). \tag{3.57}$$

The expressions for the resonant inductor current, $i_{L_r}(t)$, and resonant capacitor voltage, $v_{C_r}(t)$, can be found by using the initial conditions $i_{L_r}(t_1) = 0$

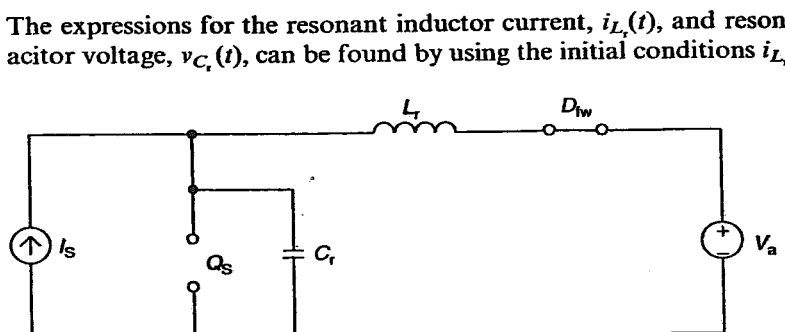


Figure 3.34 Mode 2 equivalent circuit of the full-wave ZVS quasi-resonant boost converter.

and $v_{C_r}(t_1) = V_a$. The resonant inductor current, $i_{L_r}(t)$, is

$$i_{L_r}(t) = I_s(1 - \cos \omega_n t), \tag{3.58}$$

while the resonant capacitor voltage, $v_{C_r}(t)$, is

$$v_{C_r}(t) = V_a + I_s Z_n \sin \omega_n t, \tag{3.59}$$

where Z_n and ω_n are the circuit characteristic impedance and resonant frequency, respectively, as defined previously. Mode 2 is also known as the resonant mode. The resonant capacitor voltage continues to swing to the negative cycle as it feeds energy back to the input source as shown in Figure 3.35.

The duration of the resonant mode, $T_2 = t_2 - t_1$, can be found by setting $v_{C_r}(T_2) = 0$:

$$v_{C_r}(T_2) = V_a + I_s Z_n \sin(\omega_n T_2) = 0. \tag{3.60}$$

The duration of mode 2, T_2, is

$$T_2 = \frac{\sin^{-1}(-(V_a/I_s Z_n))}{\omega_n} = \frac{\alpha}{\omega_n}, \tag{3.61}$$

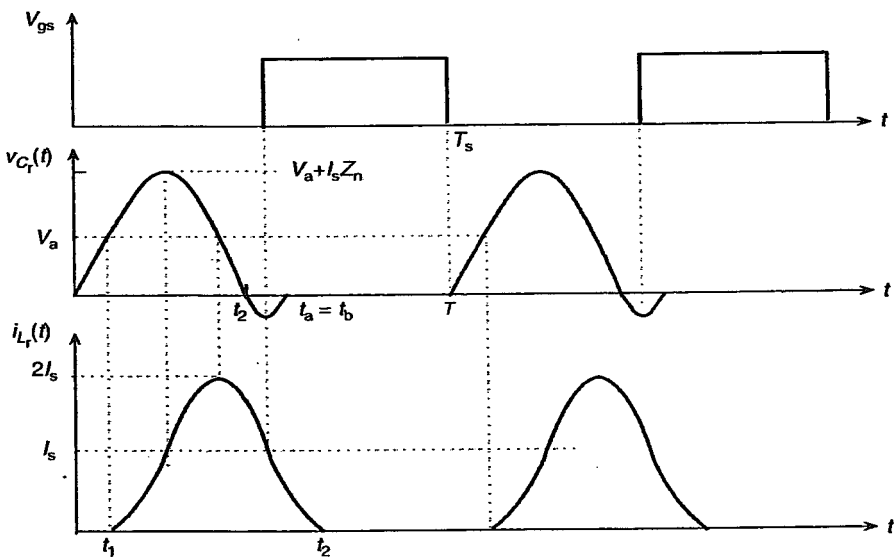


Figure 3.35 Waveforms of the full-wave ZCS quasi-resonant boost converter.

where α takes on values of 1.5π and 2π. The resonant mode terminates after all the stored energy in the resonant capacitor has been fed back to the input source. The switching transistor, Q_s, should be switched on during the negative resonant capacitor voltage cycle. Otherwise, the resonant capacitor will begin to recharge and the switching transistor will miss the opportunity to switch on at the zero-voltage condition. It should be noted that the input current, I_s, must be greater than V_a/Z_n for the switching transistor to switch on at zero voltage.

Mode 3 ($t_2 < t \leq t_3$)

Mode 3 begins after the resonant capacitor voltage decreases to zero from its negative peak at time t_2. The equivalent circuit is shown in Figure 3.36. Both the switching transistor, Q_s and the freewheeling diode, D_{fw}, are switched on during this mode. The resonant inductor current continues to decrease according to

$$L_r \mathrm{d}\frac{i_{L_r}}{\mathrm{d}t} = -V_a. \tag{3.62}$$

The initial resonant inductor current is

$$i_{L_r}(t_2) = I_s[1 - \cos\alpha]. \tag{3.63}$$

The duration of mode 3, $T_3 = t_3 - t_2$, is

$$T_3 = \frac{L_r I_s[1 - \cos\alpha]}{V_a}. \tag{3.64}$$

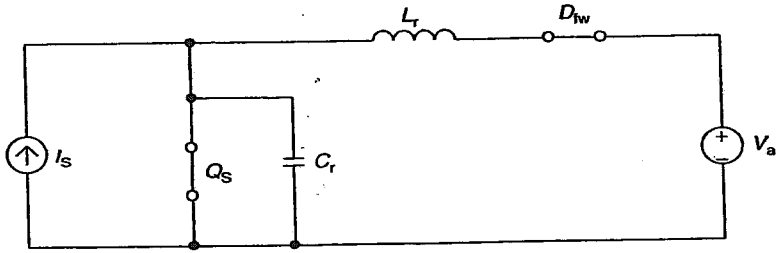


Figure 3.36 Mode 3 equivalent circuit of the full-wave ZVS quasi-resonant boost converter.

Mode 4 ($t_3 < t \leq T_s$)

Mode 4 begins when the resonant inductor current decreases to zero at time t_3. The freewheeling diode, D_{fw}, is now reverse biased and switched off at time t_3. The equivalent circuit is shown in Figure 3.37. The duration of this mode is

$$T_4 = T_s - T_1 - T_2 - T_3, \tag{3.65}$$

where T_s is the switching period.

The voltage conversion ratio of the full-wave ZVS quasi-resonant boost converter can be found by imposing the constant volt-second relationship on the input inductor, L_i. The average voltage across the input inductor during the time interval between t_1 and t_3 (i.e., $T_n = t_3 - t_1$) is $(V_s - V_a)$. During the remaining time interval (i.e., $T_s - T_n$), the average voltage across the input inductor is V_s. Thus,

$$(V_s - V_a)T_n + V_s(T_s - T_n) = 0. \tag{3.66}$$

The voltage conversion ratio of the full-wave ZVS quasi-resonant boost converter is

$$\frac{V_a}{V_s} = \frac{f_n}{f_s}. \tag{3.67}$$

A plot of the voltage conversion ratio versus f_s/f_n of a full-wave ZVS quasi-resonant boost converter is shown in Figure 3.38. As shown, the voltage conversion ratio is inversely proportional to the f_s/f_n ratio. A lower switching frequency in the ZVS quasi-resonant boost converter yields a higher average output voltage. Note that the voltage conversion ratio of the ZVS quasi-resonant boost converter is quite different from that of the ZCS

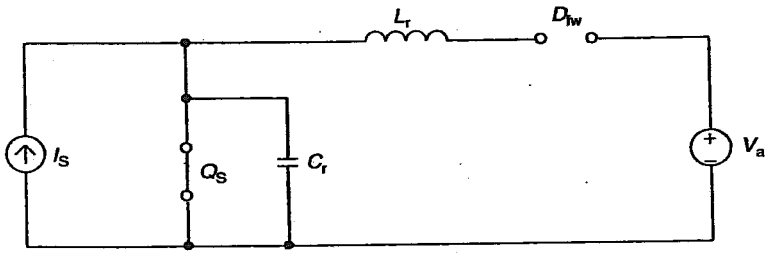


Figure 3.37 Mode 4 equivalent circuit of the full-wave ZVS quasi-resonant boost converter.

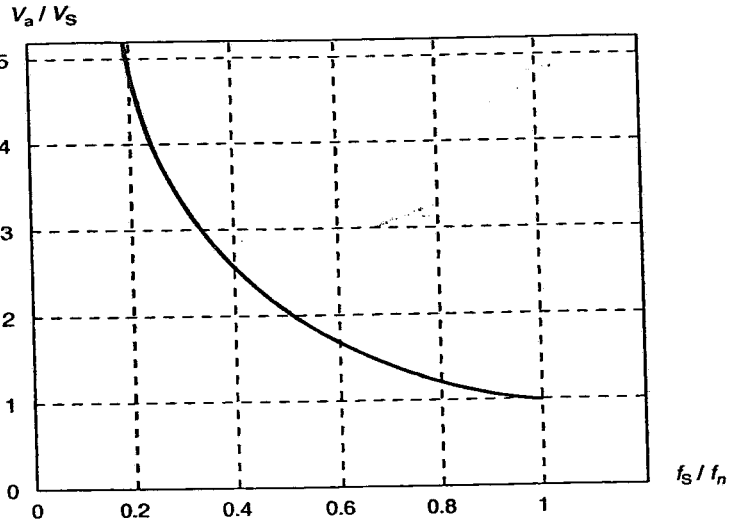


Figure 3.38 Voltage conversion ratio versus f_s/f_n for the full-wave ZVS quasi-resonant boost converter.

quasi-resonant boost converter, as well as the conventional boost converter. As in all other quasi-resonant converters, the switching frequency of the ZVS quasi-resonant boost converter must be less than its resonant frequency, f_n. The voltage conversion ratio of the half-wave ZVS quasi-resonant boost converter is very sensitive to load variations for the same reasons previously mentioned.

Example 3.4. The ZVS quasi-resonant boost converter shown in Figure 3.32 has an input voltage of 12 V. The output voltage is 24 V across a resistive load of 6 Ω. The values of the resonant inductor, L_r, and resonant capacitor, C_r, are 2 μH and 79 nF, respectively. Determine (a) the switching frequency, f_s, (b) the duration that the resonant capacitor is charged, (c) the peak resonant inductor current, and (d) the peak voltage across the resonant capacitor.

Solution.

(a) The resonant frequency, f_n, is 400 kHz.
From Equation (3.67), the switching frequency, f_s, is

$$f_s = \frac{V_s}{V_a} f_n = \frac{12}{24}\ 400\ \text{kHz} = 200\ \text{kHz}.$$

(b) From Ohm's law, the average output current is

$$I_o = \frac{V_a}{R} = \frac{24}{6} = 4\text{A}.$$

Assuming a lossless converter, the average input current is

$$I_s = \frac{V_a I_o}{V_s} = \frac{24(4)}{12} = 8\text{A}.$$

From Equation (3.55), the resonant capacitor is charged for

$$T_1 = C_r \frac{V_a}{I_s} = (79 \times 10^{-9})\frac{24}{8} = 237\,\text{ns}.$$

(c) From Equation (3.58), the peak current in the resonant inductor is

$$I_{L_r,\max} = I_s[1 - (-1)] = 8(2) = 16\text{A}.$$

(d) From Equation (3.59), the peak voltage across the resonant capacitor is

$$V_{C_r,\max} = V_a + I_s Z_n = 24 + 8\sqrt{\frac{L_r}{C_r}} = 64.25\,\text{V}.$$

3.9 SERIES-LOADED RESONANT CONVERTER [3]

The circuit schematic of a half-bridge series-loaded resonant converter is shown in Figure 3.39. As the name implies, both, the resonant inductor, L_r, and the resonant capacitor, C_r, are connected in series with the output load via a full-wave rectification circuit. The series-loaded resonant converter topology has an important advantage over the parallel-loaded resonant converter in high-voltage applications since it does not require an output

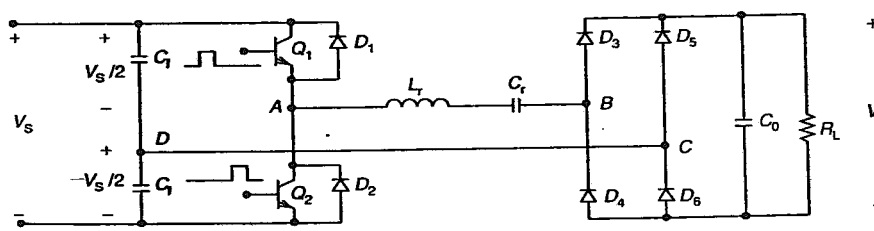


Figure 3.39 Circuit schematic of a half-bridge series-loaded resonant converter.

inductor. For a very large output filter capacitor, the rectification circuit and the load can be represented as a constant output voltage source of V_o. In the steady-state symmetrical operation, the switching transistors, Q_1 and Q_2, conduct for less than each half cycle of a switching period. Similarly, the two antiparallel diodes, D_1 and D_2, conduct during a portion of each half cycle of a switching period. Thus, it is sufficient to analyze only one-half cycle of the operation in this resonant converter. The input voltage, V_s, is divided equally between the two symmetrical input capacitors that serve as the input sources during each half of the switching cycle. As such, the one-half equivalent circuit, neglecting all parasitic resistances, can be represented as shown in Figure 3.40.

This is essentially an undamped series-resonant circuit. In the steady-state, the operation of the half-bridge series-loaded resonant converter can be classified as either the discontinuous mode or the continuous mode. There are two continuous modes of operation, depending on the switching frequency.

3.9.1 Discontinuous Mode ($0 < f < 0.5f_n$)

In the discontinuous mode of operation, the energy in the resonant inductor is consumed before the second switching transistor is switched on in the second-half of a switching cycle. There are six stages of operation in one switching cycle. Suppose before the beginning of a switching cycle, the voltage across the resonant capacitor, $v_{C_r}(0)$, is charged to $(V_o - 0.5\,V_s)$ and the current flowing through the resonant inductor, $i_{L_r}(0)$, is zero. Stage 1 $(0 < t \leq t_1)$ begins when the switching transistor Q_1 is switched on at time $t = 0$. The current in the resonant inductor begins to increase sinusoidally as the resonant capacitor voltage increases from its initial value of $(V_o - 0.5\,V_s)$ toward a positive value. It should be noted that $V_o \leq 0.5\,V_s$. The equivalent circuit for stage 1 is shown in Figure 3.41(a).

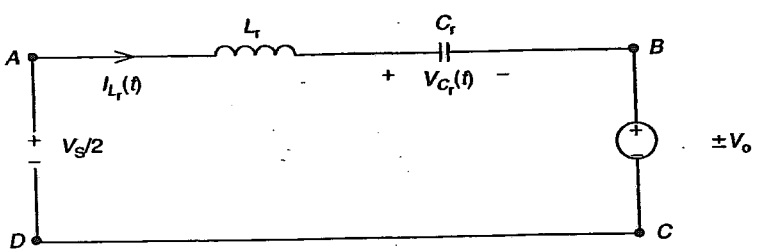


Figure 3.40 Equivalent circuit for the half-bridge series-loaded resonant converter.

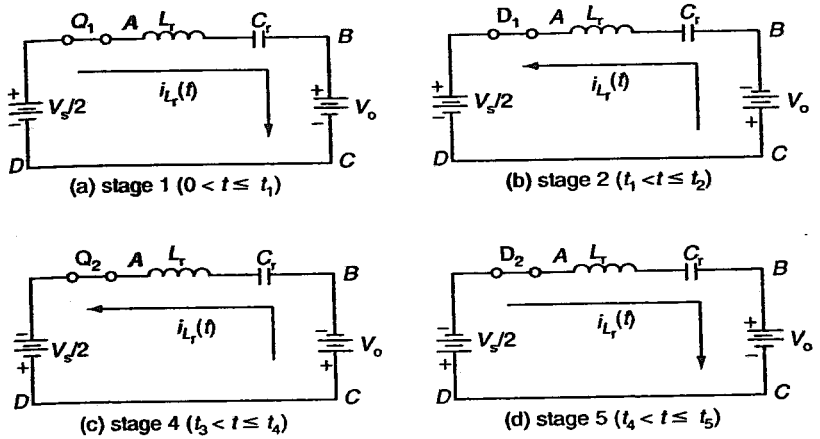


Figure 3.41 Discontinuous-mode equivalent circuits for the half-bridge series-loaded resonant converter.

The rate of rise of the resonant inductor current is related to the voltage across its terminals according to

$$\frac{di_{L_r}(t)}{dt} = \frac{((V_s/2) - V_o - v_{C_r}(t))}{L_r}, \tag{3.68}$$

while the rate of rise of the resonant capacitor voltage is

$$d\frac{v_{C_r}(t)}{dt} = \frac{i_{L_r}(t)}{C_r}. \tag{3.69}$$

Thus, the series-loaded resonant converter acts as a step-down converter without an output transformer. The current flowing through the resonant inductor, $i_{L_r}(t)$, is

$$i_{L_r}(t) = \frac{V_s - 2V_o}{Z_o} \sin(\omega_n t), \tag{3.70}$$

and the voltage across the resonant capacitor, $v_{C_r}(t)$, is

$$v_{C_r}(t) = \frac{V_s}{2} - V_o - (V_s - 2V_o)\cos(\omega_n t), \tag{3.71}$$

where $\omega_n = 1/\sqrt{L_r C_r}$ is the resonant frequency and $Z_o = \sqrt{L_r/C_r}$ is the characteristic impedance. Stage 1 ends at time t_1 when the current flowing

through the resonant inductor decreases to zero and the voltage across the resonant capacitor reaches its peak value of $(3V_s/2) - 3V_o$. Hence, the switching transistor commutates naturally and switches off at both zero current and zero voltage.

Stage 2 ($t_1 < t \leq t_2$) begins when the antiparallel diode, D_1, is forward-biased at t_1 as the direction of the resonant inductor current reverses. The voltage across the resonant capacitor decreases as it discharges its stored energy to the upper input source via the antiparallel diode, D_1. The equivalent circuit is shown in Figure 3.41(b). The polarity of the voltage across terminals B and C (i.e., v_{BC}) is reversed since the current now flows through the rectifiers D_4 and D_5. Stage 2 ends when the current in the resonant inductor decreases to zero again and the voltage across the resonant capacitor reaches a value of $0.5\,V_s - V_o$. Thus, the antiparallel diode, D_1, switches on and off at zero current. During stage 3 ($t_2 < t \leq t_3$), all the switching devices remain off. The resonant capacitor voltage remains at $0.5\,V_s - V_o$ since there is no discharge path. This completes the first half-cycle of operation. Stage 4 ($t_3 < t \leq t_4$) begins when the lower switching transistor, Q_2, switches on at time t_3. The polarity of the source voltage reverses since it is connected through the lower switching transistor, Q_2. Both the resonant inductor current and the resonant capacitor voltage begin to decrease toward their negative peaks. The equivalent circuit during stage 4 is shown in Figure 3.41(c). Stage 4 ends when the current in the resonant inductor reaches zero from its negative value. The switching transistor, Q_2, commutates naturally. At the same time, the antiparallel diode, D_2, switches on as it is forward-biased, thus feeding the stored energy in the resonant tank back to the lower input source during stage 5 ($t_4 < t \leq t_5$). v_{BC} reverses its polarity as the output current flows through the rectifiers D_3 and D_6. Stage 6 ($t_5 < t \leq T$) is characterized by zero current in the resonant inductor and a constant voltage of $V_o - 0.5\,V_s$ across the resonant capacitor. This completes the switching cycle. The switching waveforms for the half-bridge series-loaded resonant converter are shown in Figure 3.42. Since the switching transistors switch off at both zero current and zero voltage in the discontinuous mode of operation, it is feasible to use conventional silicon-controlled rectifiers without the need for commutation circuits in high-power, low-frequency applications.

3.9.2 Continuous Mode ($f_s > f_n$ or Above-Resonant Mode)

There are six stages of operation in the above-resonant continuous mode of operation. Figure 3.43 shows the first three stages during the first-half cycle of operation. Suppose before the beginning of a switching cycle, the voltage across the resonant capacitor is at some negative value, while the resonant

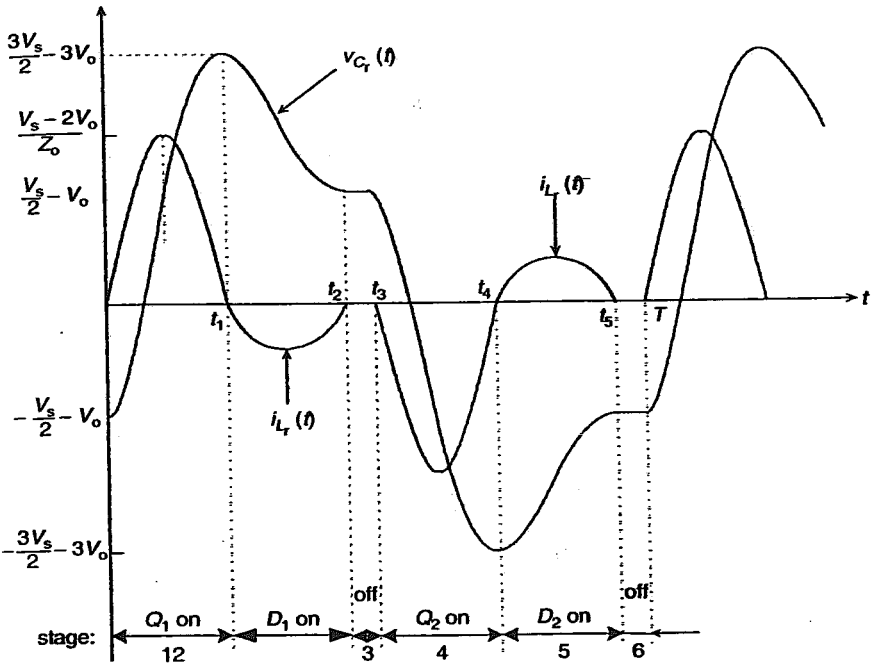


Figure 3.42 Switching waveforms for the discontinuous-mode half-bridge series-loaded resonant converter.

inductor current is at some positive value. Stage 1 ($0 < t \leq t_1$) begins when the switching transistor, Q_1, switches on at $t = 0$. The rate of rise of the resonant inductor current is related to the voltage across its terminals according to

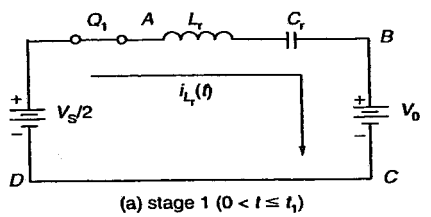
$$\frac{di_{L_r}(t)}{dt} = \frac{((V_s/2) - V_o - v_{C_r}(t))}{L_r}, \tag{3.72}$$

while the rate of rise of the resonant capacitor voltage is

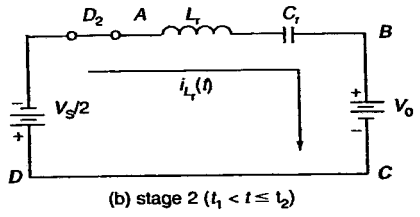
$$\frac{dv_{C_r}(t)}{dt} = \frac{i_{L_r}(t)}{C_r}. \tag{3.73}$$

The above two equations can be solved using the initial conditions $i_{L_r}(0)$ (for $i_{L_r}(0) > 0$) and $v_{C_r}(0)$ (for $v_{C_r}(0) < 0$). The resonant inductor current, $i_{L_r}(t)$, is

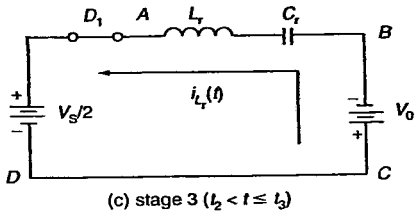
$$i_{L_r}(t) = \frac{((V_s/2) - V_o - v_{C_r}(0))}{Z_n} \sin(\omega_n t) + i_{L_r}(0) \cos(\omega_n t), \tag{3.74}$$



(a) stage 1 ($0 < t \leq t_1$)



(b) stage 2 ($t_1 < t \leq t_2$)



(c) stage 3 ($t_2 < t \leq t_3$)

Figure 3.43 Continuous-mode ($f_s > f_n$) equivalent circuits for the half-bridge series-loaded resonant converter.

and the voltage across the resonant capacitor, $v_{C_r}(t)$, is

$$v_{C_r}(t) = \left(\frac{V_s}{2} - V_o\right) - \left(\frac{V_s}{2} - V_o - v_{C_r}(0)\right)\cos(\omega_n t) + i_{L_r}(0) Z_n \sin(\omega_n t). \tag{3.75}$$

It is noted that the peak of the resonant inductor current occurs when the resonant capacitor voltage is equal to $(0.5\ V_s - V_o)$. Stage 2 ($t_1 < t \leq t_2$) begins when the switching transistor Q_1 is forced to switch off at time t_1. Since the resonant inductor current cannot be interrupted, the antiparallel diode, D_2, starts to conduct as it is forward-biased and the resonant inductor current continues to flow through the path along D_3, the output V_o, D_6, the bottom input source $0.5\ V_2$, and D_2. The resonant capacitor voltage continues to increase according to

$$v_{C_r}(t) = -\left(\frac{V_s}{2} + V_o\right) + \left(\frac{V_s}{2} + V_o + v_{C_r}(t_1)\right)\cos(\omega_n t) + i_{L_r}(t_1) Z_n \sin(\omega_n t), \tag{3.76}$$

and the resonant inductor current decreases according to

$$i_{L_r}(t) = -\frac{((V_s/2) + V_o + v_{C_r}(t_1))}{Z_n}\sin(\omega_n t) + i_{L_r}(t_1)\cos(\omega_n t). \tag{3.77}$$

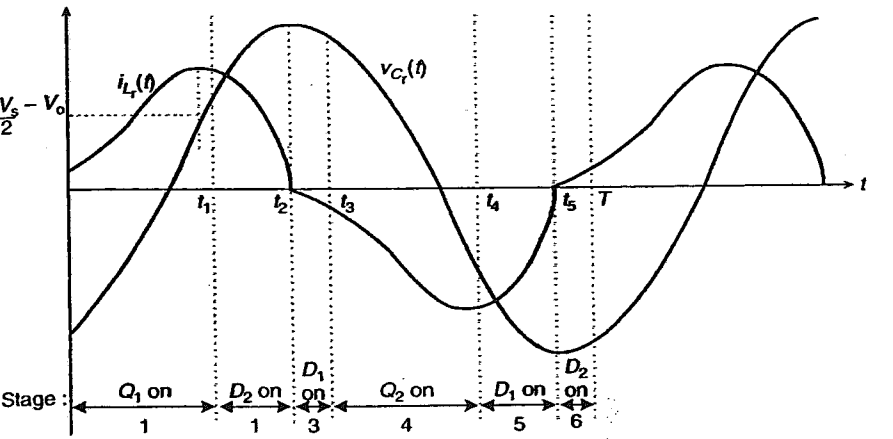


Figure 3.44 Switching waveforms for the above-resonant continuous-mode half-bridge series-loaded resonant converter.

Stage 2 ends when the resonant inductor current decreases to zero at time t_2. The resonant capacitor voltage is now at its positive peak value. Stage 3 ($t_2 < t \leq t_3$) begins when the resonant inductor current decreases to zero at time t_2. The antiparallel diode, D_1, is forward-biased and feeds energy back to the upper voltage source. Stage 3 ends when the switching transistor, Q_2, switches on at time t_3. This completes the first half-cycle of operation. The switching waveforms of this continuous mode of operation are shown in Figure 3.44. The combined conduction interval for the positive resonant inductor current is less than 180° of the resonant frequency, thus resulting in $f_s > f_n$ or $T_s < T_n$.

3.9.3 Continuous Mode ($0.5f_n < f < f_n$ or Below-Resonant Mode)

The below-resonant continuous mode has four stages of operation in one switching cycle. Suppose before the start of a switching cycle, the inductor current is positive while the voltage across the resonant capacitor is negative. The switching waveforms and equivalent circuits are shown in Figure 3.45 and Figure 3.46, respectively. Stage 1 ($0 < t \leq t_1$) begins when the switching transistor, Q_1, switches on at $t = 0$. The resonant inductor current increases and reaches its peak amplitude when the resonant capacitor voltage reaches ($0.5\,V_s - V_o$). The switching transistor remains conducting until it is naturally commutated when the resonant inductor current reduces to zero. Stage 2 ($t_1 < t \leq t_2$) begins as the antiparallel diode, D_1, conducts. The resonant

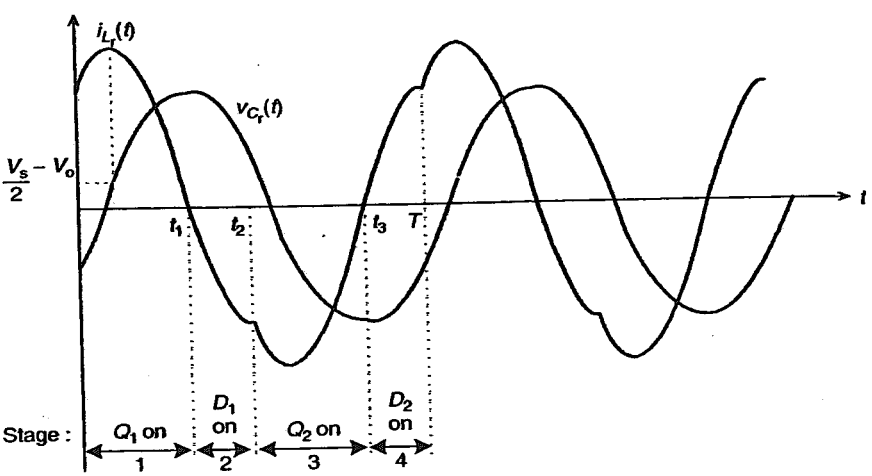


Figure 3.45 Switching waveforms for the below-resonant continuous-mode half-bridge series-loaded resonant converter.

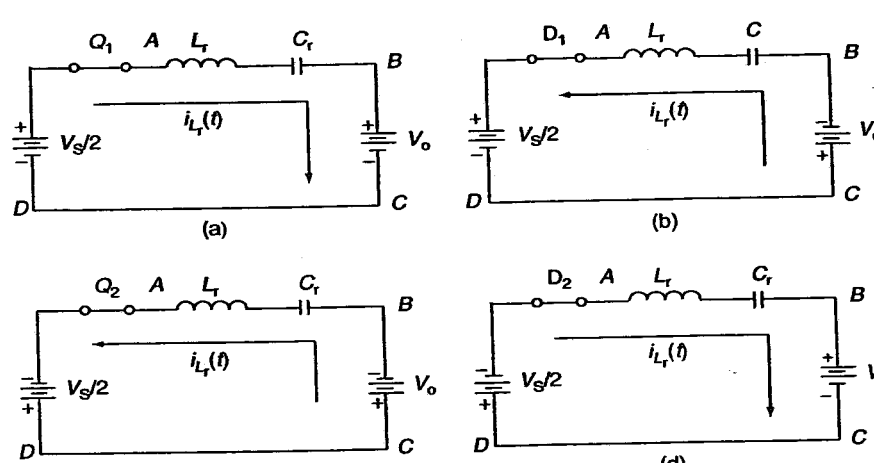


Figure 3.46 Equivalent circuits for the below-resonant continuous-mode half-bridge series-loaded resonant converter.

inductor current reverses its direction as it feeds energy back to the upper input source. At the same time, v_{BC} reverses its polarity as the output current flows through D_4 and D_5. Stage 3 ($t_2 < t \leq t_3$) commences as the switching transistor, Q_2, switches on at time t_2 and remains conducting until it is

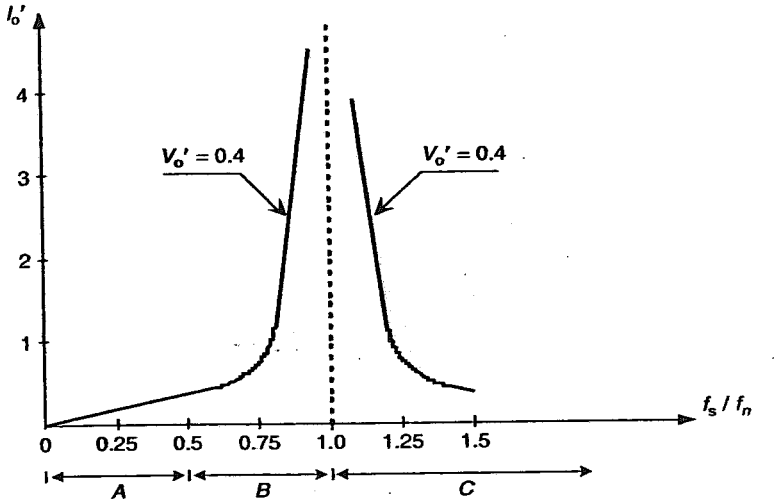


Figure 3.47 Steady-state output characteristics of a half-bridge series-loaded resonant converter: (A) discontinuous mode, (B) below-resonant continuous mode, and (C) above-resonant continuous mode.

naturally commutated at time t_3. Stage 4 ($t_3 < t \leq T$) begins as the resonant inductor current continues to flow through D_2. The next cycle starts when the switching transistor, Q_1, switches on again.

Figure 3.47 shows the steady-state normalized output current I_o' versus f_s/f_n characteristics of the series-loaded resonant converter. As shown, the discontinuous mode requires a larger change in switching frequency to maintain a constant output voltage, V_o', as the load current changes. As such, the discontinuous mode of operation is to be avoided for a large load swing. The output voltage remains fairly constant in the two continuous modes of operation. In the above-resonant mode, the switching frequency must decrease to increase the output voltage or current, while the switching frequency in the below-resonant mode must be increased to increase the output voltage or current. However, the continuous mode is the preferred mode of operation since it requires a smaller frequency range to regulate the output voltage.

Example 3.5. The series-loaded resonant converter shown in Figure 3.39 has the following parameters for its components: $C_r = 0.1\,\mu F$, $L_r = 100\,\mu H$, $C_f = 1000\,\mu F$, and $C_o = 2000\,\mu F$. The input source, V_s, is 24 V and the output voltage, V_o, is 5 V. The switching frequency is 20 kHz. Identify the mode of operation for this series-loaded resonant converter. Determine

(a) the peak amplitude of the resonant inductor current and (b) the peak value of the resonant capacitor voltage.

Solution. The resonant frequency, f_n, is

$$f_n = \frac{1}{2\pi\sqrt{L_r C_r}} = 50.3\,\text{kHz}.$$

Since $f_s = 20\,\text{kHz}$ is less than $f_n/2 = 25.15\,\text{kHz}$, the series-loaded resonant converter is operating in the discontinuous mode of operation.

(a) From Equation (3.70), the peak amplitude of the resonant inductor current is

$$I_{L_{r(\text{peak})}} = \frac{V_s - 2V_o}{Z_o} = \frac{24 - 10}{\sqrt{(100/0.1)}} = 0.443\,\text{A}.$$

(b) From Equation (3.71), the peak amplitude of the resonant capacitor voltage is

$$v_{C_{r(\text{peak})}} = \frac{V_s}{2} - V_o - (V_s - 2V_o)(-1) = \frac{3V_s}{2} - 3V_o = 21\,\text{V}.$$

3.10 PARALLEL-LOADED RESONANT CONVERTER [4]

In the parallel-loaded resonant converter, the load is connected directly across the resonant capacitor, C_r, via a full-wave rectification circuit as shown in Figure 3.48. This converter is capable of providing an output voltage that is higher or lower in amplitude than its input voltage without the use of a transformer. Parallel-loaded resonant converters are mainly used for low-voltage, high-current applications since the output inductor reduces

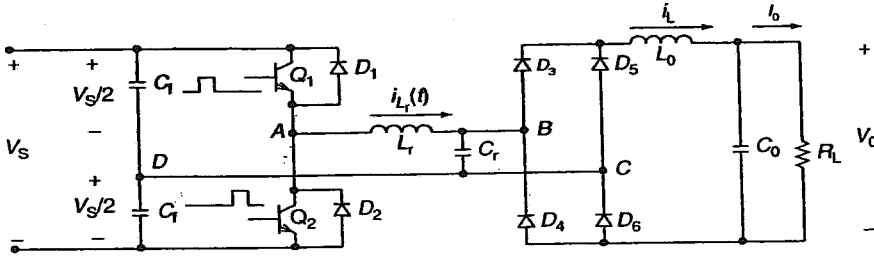


Figure 3.48 Circuit schematic of a half-bridge parallel-loaded resonant converter.

the ripple current in the output capacitor. For a sufficiently large output inductor, the output of the parallel-loaded resonant converter can be represented as a constant current sink of magnitude I_o. The equivalent circuit of the parallel-loaded resonant converter is shown in Figure 3.49. In the steady-state, these converters can operate in either the discontinuous or continuous modes of operation.

3.10.1 Discontinuous Mode ($0 < f < 0.5f_n$)

Suppose before the beginning of a switching cycle, the resonant inductor current is zero and the output current, I_o, is freewheeling through the four rectifiers. The resonant capacitor is clamped at zero volt by the freewheeling action. The switching waveforms for the below-resonant discontinuous mode of operation are shown in Figure 3.50.

Stage 1 ($0 < t \leq t_1$) begins when the switching transistor, Q_1, switches on at time $t = 0$. The equivalent circuit is shown in Figure 3.51(a).

The rate of increase of the resonant inductor current is

$$\frac{di_{L_r}(t)}{dt} = \frac{V_s}{2L_r}. \tag{3.78}$$

The resonant inductor current increases linearly according to

$$i_{L_r}(t) = \frac{V_s t}{2L_r}. \tag{3.79}$$

The duration of stage 1 is

$$t_1 = \frac{2L_r I_o}{V_s}. \tag{3.80}$$

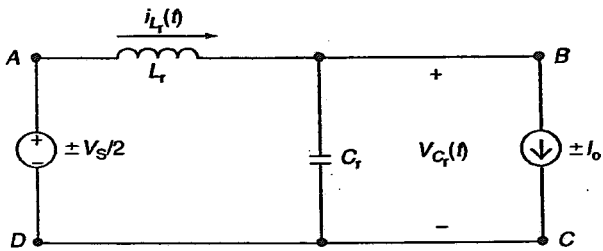


Figure 3.49 Equivalent circuit for the half-bridge parallel-loaded resonant converter.

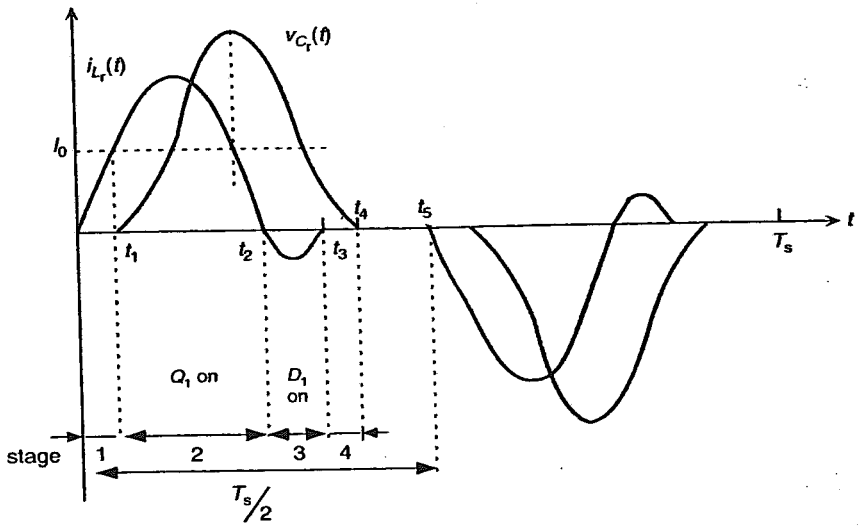


Figure 3.50 Switching waveforms for the discontinuous-mode half-bridge parallel-loaded resonant converter.

Stage 2 ($t_1 < t \leq t_2$) begins when the resonant inductor current reaches the magnitude of the output current, I_o, at time t_1. The output current, I_o, is now supplied entirely by the input source. The resonant capacitor is charged by the difference between the resonant inductor current and the output current (i.e., $i_{L_r}(t) - I_o$). As the resonant capacitor voltage increases, rectifiers D_4 and D_5 are reverse-biased. Rectifier D_3 and D_6 remain conducting and the equivalent circuit is shown in Figure 3.51(b). The rate of rise of the voltage across the resonant capacitor is

$$\frac{dv_{C_r}(t)}{dt} = \frac{i_{L_r}(t) - I_o}{C_r}. \tag{3.81}$$

The resonant inductor current begins to increase in a sinusoidal fashion. The rate of increase of the resonant inductor current, $i_{L_r}(t)$, is

$$\frac{di_{L_r}(t)}{dt} = \frac{((V_s/2) - v_{C_r}(t))}{L_r}. \tag{3.82}$$

The resonant capacitor voltage, $v_{C_r}(t)$, and the resonant inductor current, $i_{L_r}(t)$, can be found using the initial conditions of $i_{L_r}(0) = I_o$ and $v_{C_r}(0) = 0$ to yield

$$i_{L_r}(t) = I_o + \frac{V_s}{2Z_o} \sin[\omega_n(t - t_1)], \tag{3.83}$$

and

$$v_{C_r}(t) = \frac{V_s}{2}[1 - \cos \omega_n(t - t_1)], \tag{3.84}$$

where $Z_o = \sqrt{(L_r/C_r)}$.

It can be seen from the above equation that the resonant capacitor voltage approximates a haversine function with a peak value of V_s. The resonant inductor current reaches its peak value when the resonant capacitor voltage reaches 0.5 V_s. On the other hand, the resonant capacitor voltage attains its peak as the resonant inductor current decreases to I_o from its peak. The switching transistor, Q_1, remains conducting until its current decreases to zero at a time t_2, given by

$$t_2 = t_1 + \frac{[\pi + \sin^{-1}(2I_oZ_o/V_s)]}{\omega_n}. \tag{3.85}$$

Thus, the switching transistors switch off naturally in the discontinuous mode of operation.

Stage 3 ($t_2 < t \leq t_3$) begins when the anti-parallel diode, D_1, switches on at time t_2 as the current in the resonant inductor decreases to zero. The equivalent circuit is shown in Figure 3.51(c). The tank energy is fed back to the source through the antiparallel diode, D_1. Stage 3 ends when the resonant inductor current decreases to zero from its negative peak at a time t_3, given by

$$t_3 = t_1 + \frac{[2\pi - \sin^{-1}(2I_oZ_o/V_s)]}{\omega_n}. \tag{3.86}$$

Stage 4 ($t_3 < t \leq t_4$) commences at time t_3. The resonant capacitor voltage during this time interval is

$$v_{C_r}(t) = \frac{1}{C_r}\int_{t_3}^{t} [-I_o]dt = v_{C_r}(t_3) - \frac{I_o(t - t_3)}{C_r}, \tag{3.87}$$

where

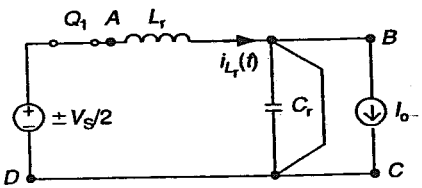
$$v_{C_r}(t_3) = \frac{V_s}{2}\left[1 - \cos\left(2\pi - \sin^{-1}\frac{2I_oZ_o}{V_s}\right)\right]. \tag{3.88}$$

The resonant capacitor continues to discharge its stored energy to the output as shown by the equivalent circuit in Figure 3.51(d) until time t_4, given by

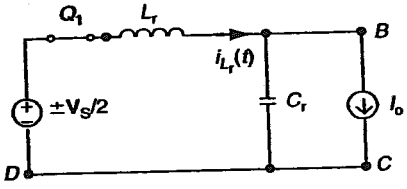
$$t_4 = t_3 + \frac{C_r v_{C_r}(t_3)}{I_o}. \tag{3.89}$$

Stage 5 ($t_4 < t \leq t_5$) commences when the voltage across the resonant capacitor decreases to zero. The output circuit is now freewheeling through the rectifiers to maintain a constant output current, I_o. This completes the first half-cycle of operation. The above half-cycle operation is repeated as the switching transistor, Q_2, switches on at time t_5, except that the direction of the resonant inductor current and the polarity of the resonant capacitor voltage are reversed. The average output voltage is determined by rectifying and averaging the resonant capacitor voltage:

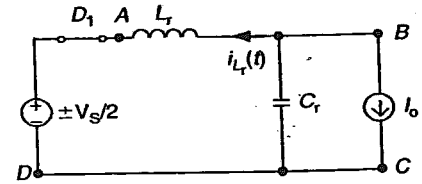
$$\begin{aligned} V_o &= \frac{2}{T}\left[\int_{t_1}^{t_3} \frac{V_s}{2}[1 - \cos\omega_n(t - t_1)]\,dt + \int_{t_3}^{t_4}\left[v_{C_r}(t_3) - \frac{I_o(t - t_3)}{C_r}\right]dt\right] \\ &= \frac{2}{T}\left[\frac{(V_s/2)(\omega_n T_3 - \sin(\omega_n T_3))}{\omega_n} + v_{C_r}(t_3)T_4 - \frac{I_o T_4^2}{2C_r}\right] \end{aligned} \tag{3.90}$$



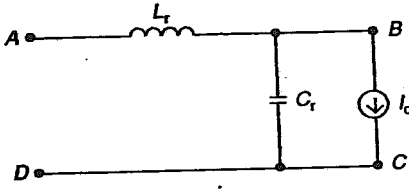
(a) stage 1($0 < t \leq t_1$)



(b) stage 2 ($t_1 < t \leq t_2$)



(c) stage 3 ($t_2 < t \leq t_3$)



(d) stage 4 ($t_3 < t \leq t_4$)

Figure 3.51 Discontinuous-mode equivalent circuits for the half-bridge parallel-loaded resonant converter.

where

$$T_3 = t_3 - t_1 = \frac{[2\pi - \sin^{-1}(2I_oZ_o/V_s)]}{\omega_n} \tag{3.91}$$

and

$$T_4 = t_4 - t_3 = \frac{C_r v_{C_r}(t_3)}{I_o}. \tag{3.92}$$

Thus, the output voltage in the discontinuous mode of operation can be regulated by controlling the off-time of the switching transistor while keeping its on-time fixed.

3.10.2 Continuous Mode ($f_s > f_2$ or Above-Resonant Mode)

There are six stages of operation in a switching cycle for the above-resonant continuous mode. In this mode of operation, the turn-on losses in the switching transistors are mitigated since they are switched on at zero resonant inductor current. The switching waveforms and equivalent circuits are shown in Figure 3.52 and Figure 3.53, respectively.

Suppose before the switching transistor is switched on, there is no current flowing through the resonant inductor, while the resonant capacitor voltage is at some negative value. Stage 1 ($0 < t \leq t_1$) commences when the switching transistor, Q_1, switches on at $t = 0$. Since the resonant capacitor voltage is negative, both the resonant inductor current and the steady-state output current, I_o, flow into the resonant capacitor. The voltage across the resonant capacitor increases from its negative value. Stage 2 ($t_1 < t \leq t_2$) begins when the resonant capacitor voltage reaches zero. However, the resonant inductor current continues to increase. The output current now flows through rectifiers D_3 and D_6 as the resonant capacitor voltage becomes positive. The resonant capacitor is now charged by the difference in the resonant inductor current and the steady-state output current (i.e., $i_{L_r}(t) - I_o$). Stage 3 ($t_2 < t \leq t_3$) begins when the switching transistor is forced to switch off at time t_2. Since the resonant inductor current cannot be interrupted, the antiparallel diode, D_2, starts to conduct. The resonant inductor current decreases from its peak value. However, the resonant capacitor voltage continues to increase as it is charged by the difference in the resonant inductor current and the output current (i.e., $i_{L_r}(t) - I_o$). The resonant capacitor voltage is at its peak value when the resonant inductor current is equal to the steady-state output current. The resonant capacitor then begins to discharge in order to maintain a constant output current, I_o. Stage 3 ends

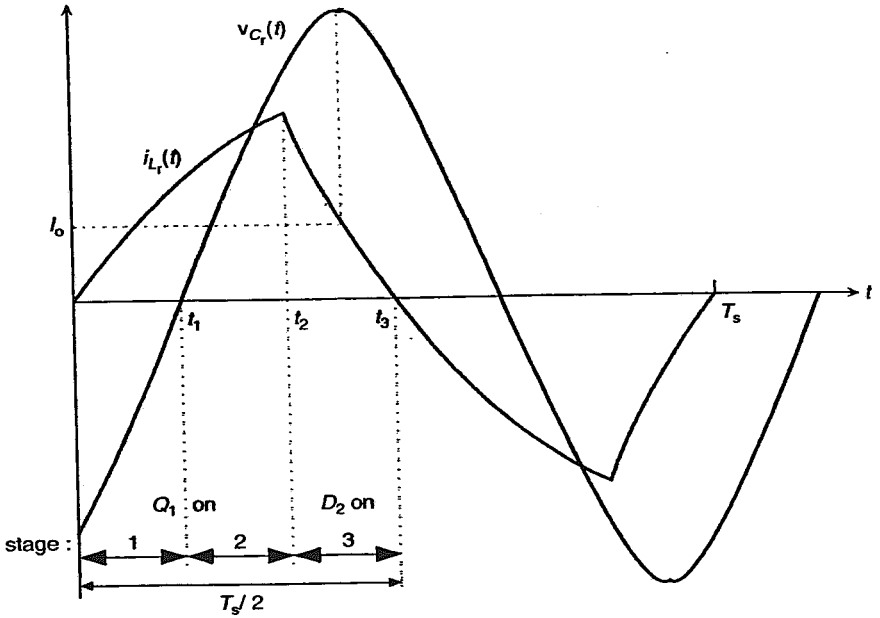
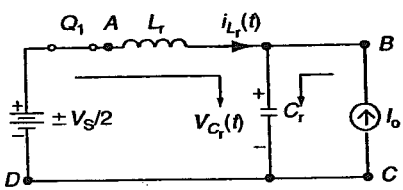
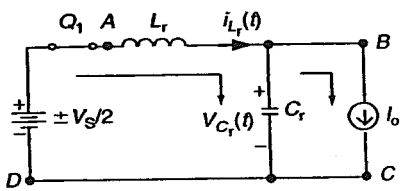


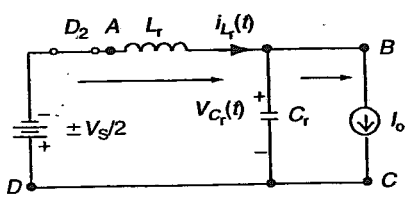
Figure 3.52 Switching waveforms for the above-resonant continuous-mode half-bridge parallel-loaded resonant converter.



(a) stage 1 ($0 < t \leq t_1$)



(b) stage 2 ($t_1 < t \leq t_2$)



(c) stage 3 ($t_2 < t \leq t_3$)

Figure 3.53 Equivalent circuits for the above-resonant continuous-mode half-bridge parallel-loaded resonant converter.

when the resonant inductor current decreases to zero at time t_3. This completes the first half-cycle of operation. The next half-cycle repeats the same way as the first half-cycle except that the direction of the resonant inductor current and the polarity of the resonant capacitor voltage are reversed.

3.10.3 Continuous Mode ($0.5f_n < f_s < f_n$ or Below-Resonant Mode)

There are six stages of operation in one switching cycle, as shown in Figure 3.54. The equivalent circuits for the first three stages are shown in Figure 3.55.

Suppose before the start of a switching cycle, the resonant inductor current attains a positive value while the resonant capacitor voltage is negative. Stage 1 ($0 < t \leq t_1$) begins when the switching transistor, Q_1, switches on at time $t = 0$. The resonant capacitor voltage increases from its negative value as it is charged by both the resonant inductor current and the output current, I_o, until it reaches zero at time t_1. Stage 2 ($t_1 < t \leq t_2$) begins when the resonant capacitor voltage reaches zero at time t_1. The steady-state output current now flows through rectifiers D_3 and D_6, as the voltage across the resonant capacitor becomes positive. The resonant capacitor is charged by the difference in the resonant inductor current and the

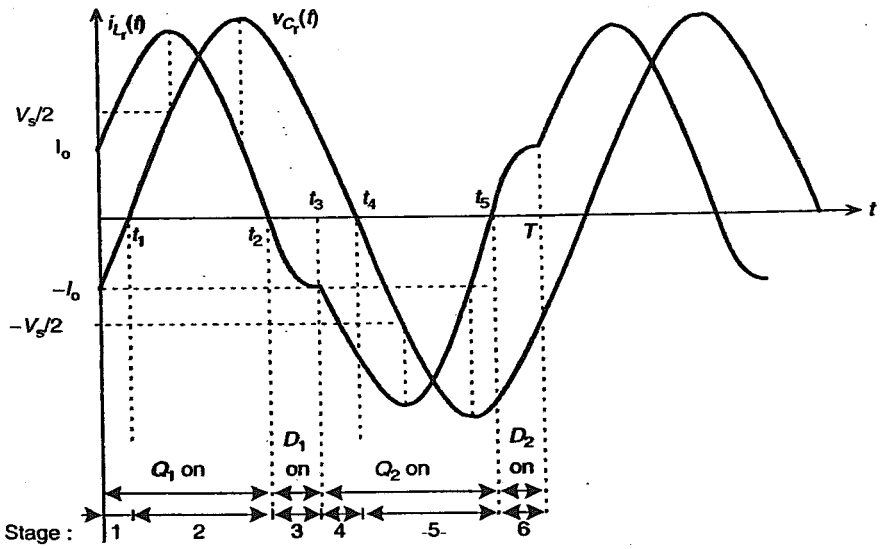


Figure 3.54 Switching waveforms for the below-resonant continuous-mode half-bridge parallel-loaded resonant converter.

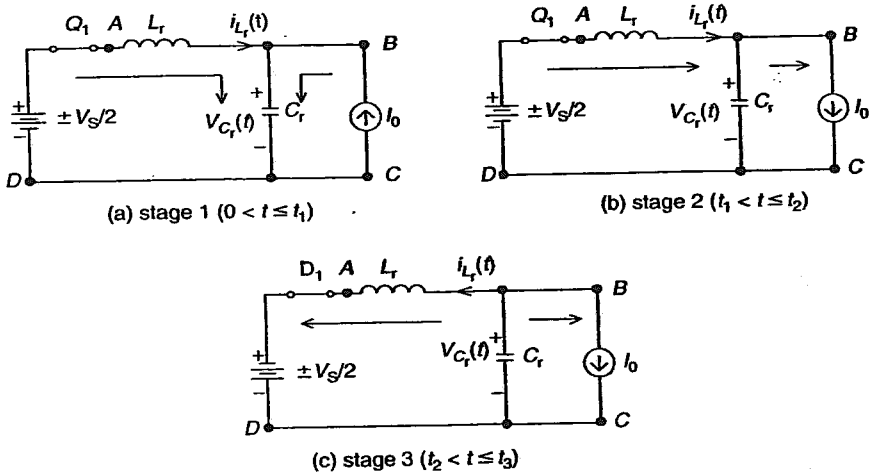


Figure 3.55 Equivalent circuits for the below-resonant continuous-mode half-bridge parallel-loaded resonant converter.

steady-state output current. The switching transistor, Q_1, remains conducting until it is switched off naturally when the resonant inductor current reaches zero at time t_2. Stage 3 ($t_2 < t \leq t_3$) begins when the antiparallel diode, D_1, starts to conduct and feeds the stored energy in the resonant tank back to the input source. Stage 3 ends when the switching transistor, Q_2, is switched on at t_3. This completes the first half-cycle of operation. The next half-cycle repeats the same way as the first half-cycle except that the direction of the resonant inductor current and the polarity of the resonant capacitor voltage are reversed.

Figure 3.56 shows the voltage conversion ratio, $V_a/0.5\,V_s$ versus f_s/f_n characteristics of a half-bridge parallel-loaded resonant converter. The output voltage of the parallel-loaded resonant converter operating in the below-resonant discontinuous mode is always less than the input voltage of $0.5\,V_s$. On the other hand, the output voltage can be higher than the input voltage of $0.5\,V_s$ for both the above-resonant and below-resonant continuous mode of operation. However, the above-resonant continuous mode is preferred since it can maintain a constant output current as the output voltage changes with a smaller change in frequency as compared to the other two modes of operation.

Example 3.6. The parallel-loaded resonant converter shown in Figure 3.48 has the following parameters for its components: $L_r = 50\,\mu\text{H}$, $C_r = 1\,\mu\text{F}$, $C_o = 500\,\mu\text{F}$, $L_o = 1\,\text{mH}$, and $C_f = 1000\,\mu\text{F}$. The input source, V_s, is a

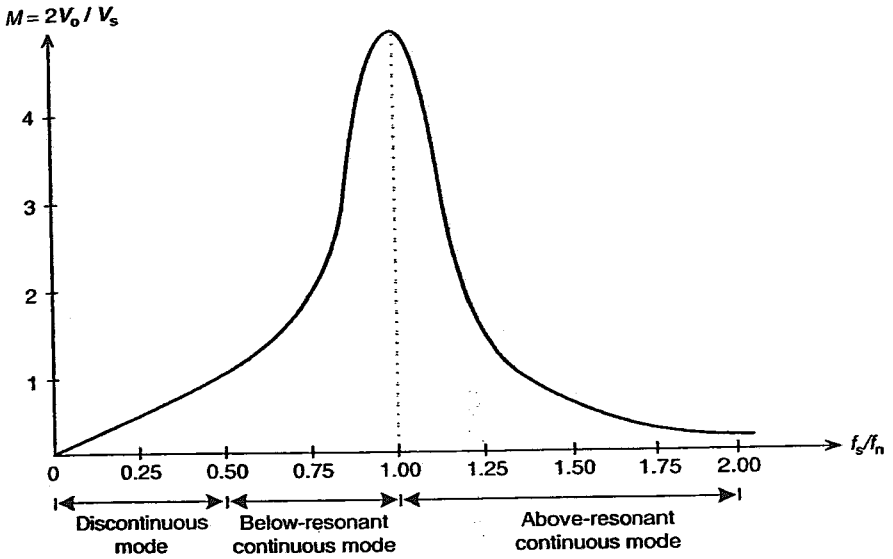


Figure 3.56 Voltage conversion ratio ($2V_o/V_s$) versus f_s/f_n of a typical half-bridge parallel-loaded resonant converter.

12-V automotive battery and the steady-state output current, I_o, is 1 A. The switching frequency is 10 kHz and the resonant capacitor voltage is clamped at zero volt before the beginning of a switching cycle. Identify the mode of operation for this converter. Determine (a) the peak value of the resonant inductor current and (b) the duration that the switching transistor is switched on.

Solution. The resonant frequency, f_n, is given by

$$f_n = \frac{1}{2\pi\sqrt{L_r C_r}} = 22.5\,\text{kHz}.$$

Since f_s is less than $0.5f_n$, the parallel-loaded resonant converter is operating in the discontinuous mode of operation.

(a) The peak value of the resonant inductor current can be found from Equation (3.83). The resonant inductor current reaches its peak value when

$$t = \frac{(\pi/2)}{2\pi f_n} = 11.1\,\mu\text{s}.$$

(b) From Equation (3.85), the duration that the switching transistor is switched on is

$$t_2 = \frac{2L_r}{V_s I_o} + \frac{[\pi + \sin^{-1}(2I_o Z_o / V_S)]}{\omega_n} = 43.43\ \mu S.$$

PROBLEMS

3.1. The ZCS quasi-resonant buck converter shown in Figure 3.9 has an input voltage of 48 V and a resistive load of 12 Ω. The values of the resonant inductor and resonant capacitor are 4 μH and 147 nF, respectively. The switching frequency is 100 kHz. The output inductor and output capacitor are 10 mH and 100 μF, respectively. Determine (a) the average output voltage, V_a, (b) the duration of the resonant mode, and (c) the minimum load resistance for this quasi-resonant converter.

3.2. Draw a circuit schematic of a full-wave ZCS quasi-resonant buck converter with an M-type switch. Sketch the waveforms for the current flowing through the resonant inductor and voltage across the resonant capacitor over two switching periods given the following parameters: $L_r = 2\,\mu H$, $C_r = 79\,nF$, $f_s = 200\,kHz$, $L_o = 10\,mH$, and $C_o = 100\,\mu F$.

3.3. The ZCS quasi-resonant boost converter shown in Figure 3.18 has an input voltage of 24 V and a resistive load of 40 Ω. The values of the resonant inductor and resonant capacitor are 10 μH and 470 nF, respectively. The switching frequency is 25 kHz. The output inductor and output capacitor are 10 mH and 100 μF, respectively. Determine (a) the average output voltage, V_a, (b) the duration of the resonant mode, (c) the time when the resonant inductor current is at its negative peak, and (d) the minimum load resistance for this quasi-resonant converter.

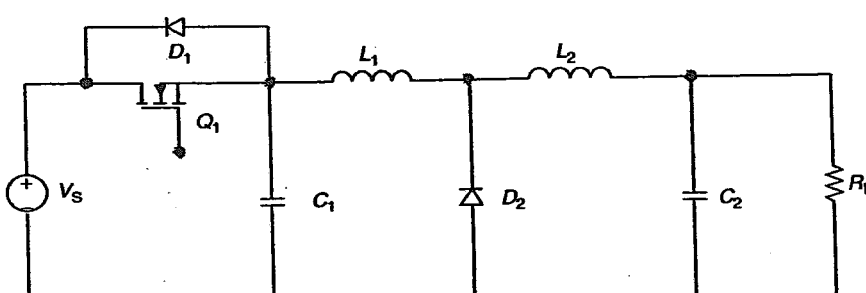


Figure 3.57 Circuit schematic for Problem 3.4.

3.4. Identify the topology of the quasi-resonant converter shown in Figure 3.57. Sketch the equivalent circuits for the four modes of operation in one switching period.

3.5. The ZVS quasi-resonant buck converter shown in Figure 3.25 has an input voltage of 24 V and a load resistance of 3 Ω. The values of the resonant inductor and resonant capacitor are 2 μH and 47 nF, respectively. The average output voltage, V_a, is 12 V. The output inductor and output capacitor are 10 mH and 100 μF, respectively. Determine (a) the switching frequency, (b) the duration of the resonant mode, (c) the time that the current flowing through the resonant inductor crosses zero during the resonant mode, and (d) the maximum load resistance for this quasi-resonant converter.

3.6. Draw a circuit schematic for a full-wave ZVS quasi-resonant boost converter with a L-type switch with the following parameters: $L_r = 10\ \mu H$, $C_r = 470\ nF$, $f_s = 25\ kHz$, $L_o = 10\ mH$, and $C_o = 100\ \mu F$. Sketch the waveforms for the current flowing through the resonant inductor and voltage across the resonant capacitor over two switching periods.

3.7. Identify the topology of the resonant converter shown in Figure 3.58. State whether it is a full-wave or half-wave and L- or M-type switch.

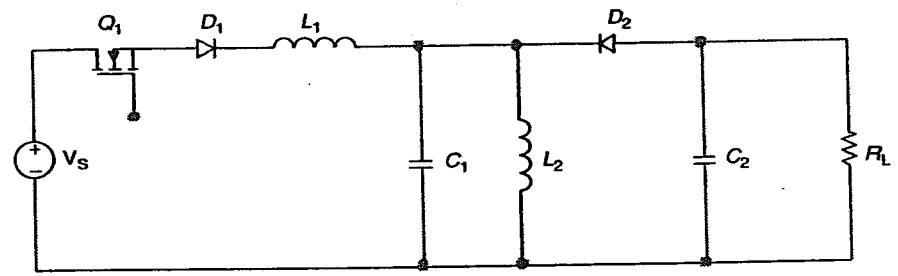


Figure 3.58 Circuit schematic for Problem 3.7.

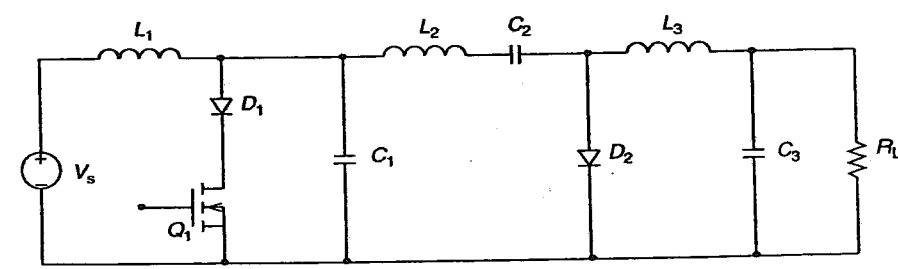


Figure 3.59 Circuit schematic for Problem 3.8.

3.8. Identify the topology of the resonant converter shown in Figure 3.59. State whether it is a full-wave or half-wave and L- or M-type switch.

3.9. The series-loaded resonant converter shown in Figure 3.39 has the following parameters for its components: $C_r = 0.1\ \mu F$, $L_r = 100\ \mu H$, $C_f = 2000\ \mu F$, and $C_o = 200\ \mu F$. The input source, V_s, is 36 V and the output voltage is 12 V. The switching frequency is 20 kHz. Identify the mode of operation for this series-loaded resonant converter. Determine (a) the peak amplitude of the resonant inductor current, (b) the duration of the negative resonant inductor current (i.e., $t_2 - t_1$), and (c) the duration of the positive-cycle of operation, t_3.

3.10. The parallel-loaded resonant converter shown in Figure 3.48 has the following parameters for its components: $L_r = 100\ \mu H$, $C_r = 0.1\ \mu F$, $C_f = 2500\ \mu F$, $L_o = 1\ mH$, and $C_o = 470\ \mu F$. The input source, V_s, is 24 V. The switching frequency is 20 kHz. Identify the mode of operation for this converter. Determine (a) the maximum steady-state load current, I_o, (b) expressions for the resonant inductor current when the upper switching transistor is switched on, and (c) the duration of the upper switching transistor switched on.

3.11. In the quasi-resonant ZCS buck converter, the output steady-state current, I_o, must be less than V_a/Z_n for the switching transistor to switch off during zero current. Explain its physical significance.

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4

Transformerized Switching Converters

4.1 INTRODUCTION

One of the most important drawbacks of the switching converter topologies, discussed in Chapters 2 and 3, is that their inputs and outputs are not isolated from each other. Isolation between the common or ground of the input supply and the output load is often desired to isolate the common returns from different parts of the electronic system to eliminate ground loops between circuitries. In switching power supplies, there is always a need to have multiple outputs with the same or different voltages for different load requirements. The switching converter topologies discussed so far can only provide a single regulated output.

Transformers are commonly used to provide isolation between the inputs and outputs of alternating-current systems. In switching converters, transformers can also be used to isolate the output load from the input power supply. Transformers also provide the necessary voltage scaling, thus enabling a higher output voltage in all the topologies considered. The use of transformers thus offers the advantage of having multiple outputs at

different voltage levels. The transformerized switching converters to be discussed in this chapter are the forward converter, push–pull switching converter, half-bridge switching converter, full-bridge switching converter, flyback converter, and resonant switching converter. Forward converters are used for medium power applications from 100 to 500 W. Push–pull-switching converters are mainly used for high-power applications to a few thousand watts. Half-bridge and full bridge switching converters are mainly used for off-line applications. Flyback converters are often used for high-voltage applications for output power from about 5 to 200 W. The choice of a switching converter for a specific application often requires many other considerations such as economic feasibility, electromagnetic interference generation, and size and weight of the switching converter.

4.2 FORWARD CONVERTER

The forward converter is the most commonly used switching converter for medium power applications below 500 W. A circuit schematic of the forward converter with a slave output is shown in Figure 4.1. The forward converter resembles the buck converter in that the switching transistor in the basic buck-switching converter is replaced by the transformer, the switching transistor, and the rectifier combination. As shown, the center-tapped transformer consists of two primary and two secondary windings. It should be noted that the dotted ends represent the transformer windings that are in phase with each other. This implies that the terminal voltages at the dotted ends increase or decrease simultaneously. The output with a negative feed-

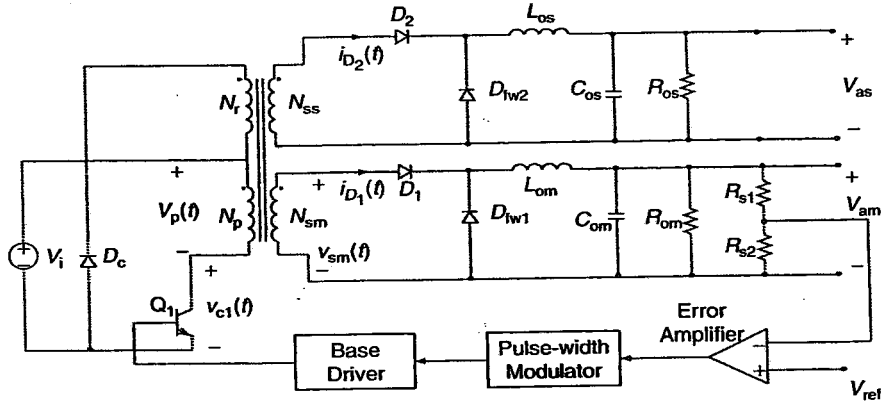

Figure 4.1 Circuit schematic of the forward converter.

back loop is called the master output while the nonfeedback output is called the slave output. In general, the dynamic behavior of the slave output depends on the load and closed-loop characteristic of the master output circuitry. However, the regulation of the slave output voltage can be improved significantly with the use of a magnetic amplifier postregulator in the slave output circuitry. By using a magnetic core as a switch, it is possible to regulate the slave output efficiently with very few parts, over a wide power range, at a reasonable cost [1]. The operation of the forward converter in the continuous mode can be divided into two modes.

Mode 1 ($0 < t \leq t_1$)

Mode 1 begins when the switching transistor, Q_1, is switched on at $t \leq 0$. Since the dotted end of the primary winding, N_p, is connected to the positive input supply voltage, V_i, all the dotted ends of the transformer windings are positive with respect to the undotted ends. The current in the primary winding rises linearly from I_1 to I_2 in time t_{on} according to:

$$V_i = L_p \frac{I_2 - I_1}{t_{on}} \tag{4.1}$$

neglecting the saturated collector–emitter voltage of the switching transistor. The duration of mode 1 is

$$t_{on} = L_p \frac{(I_2 - I_1)}{V_i}. \tag{4.2}$$

The currents in the secondary windings rise synchronously with the main primary winding, their magnitude being scaled by the inverse turns-ratio of the transformer (i.e., N_p/N_s). The current in the secondary master winding increases from $I_1(N_p/N_{sm})$ to $I_2(N_p/N_{sm})$ in time t_{on}. The voltage at the dotted end of the secondary master winding is

$$V_{sm} = V_i \frac{N_{sm}}{N_p}, \tag{4.3}$$

where N_{sm} is the number of turns in the secondary master winding. Similarly, the voltage at the dotted end of the slave secondary winding is

$$V_{ss} = V_i \frac{N_{ss}}{N_p}. \tag{4.4}$$

Thus, different output voltages can be accomplished using different number of turns for the master and slave windings. In principle, the forward

converter can accommodate multiple secondary slaves according to load requirements. Since the polarity of the dotted end of the secondaries is positive with respect to the undotted ends, the rectifiers, D_1 and D_2, are forward-biased. The freewheeling diodes, D_{fw1} and D_{fw2}, are reverse-biased. Thus, the input energy is "forward-transferred" to the output inductors during the on-time of the switching transistor and, hence, this switching converter topology is called the forward converter.

Mode 2 ($t_{on} < t \leq T_s$)

Mode 2 begins when the switching transistor, Q_1, switches off at t_{on}. Since the current flowing through the main primary winding is now interrupted, the voltage across the primary winding reverses its polarity to oppose this change. As such, the voltages at all the dotted ends of the transformer windings are now negative with respect to their undotted ends. The clamp diode, D_c, connected between the dotted end of the reset winding, N_r, and the input common, prevents this voltage from falling below its turn-on voltage of about 1 V. Hence, the rectifiers, D_1 and D_2, are reverse-biased. At the same time, the freewheeling diodes, D_{fw1} and D_{fw2}, are forward-biased and allow the output inductors to discharge their stored energies to satisfy the load requirements. Neglecting the leakage inductance of the transformer, the voltage across the primary winding is

$$v_p(t) = -V_i \frac{N_p}{N_r}. \tag{4.5}$$

Neglecting the voltage drop across the clamp diode, the voltage across the reset winding is simply the input supply voltage, V_i. The off-state collector voltage of the switching transistor is then

$$V_c = V_{N_r} + V_i \frac{N_p}{N_r} = V_i \left(1 + \frac{N_p}{N_r}\right). \tag{4.6}$$

If the number of turns in the reset winding, N_r, is equal to the number of the primary winding, N_p, then the voltages across the primary and reset windings are equal to the input supply voltage, V_i. The voltage at the collector of the switching transistor is then twice the input supply voltage, i.e., $2V_i$. The off-state collector voltage is smaller if the number of turns in the reset winding is larger than the primary winding as shown in Equation (4.6). However, the peak primary current for a given output power is greater than the case when N_r is equal to N_p. The voltage spike observed at the collector of the switching transistor shown in Figure 4.2, immediately after it

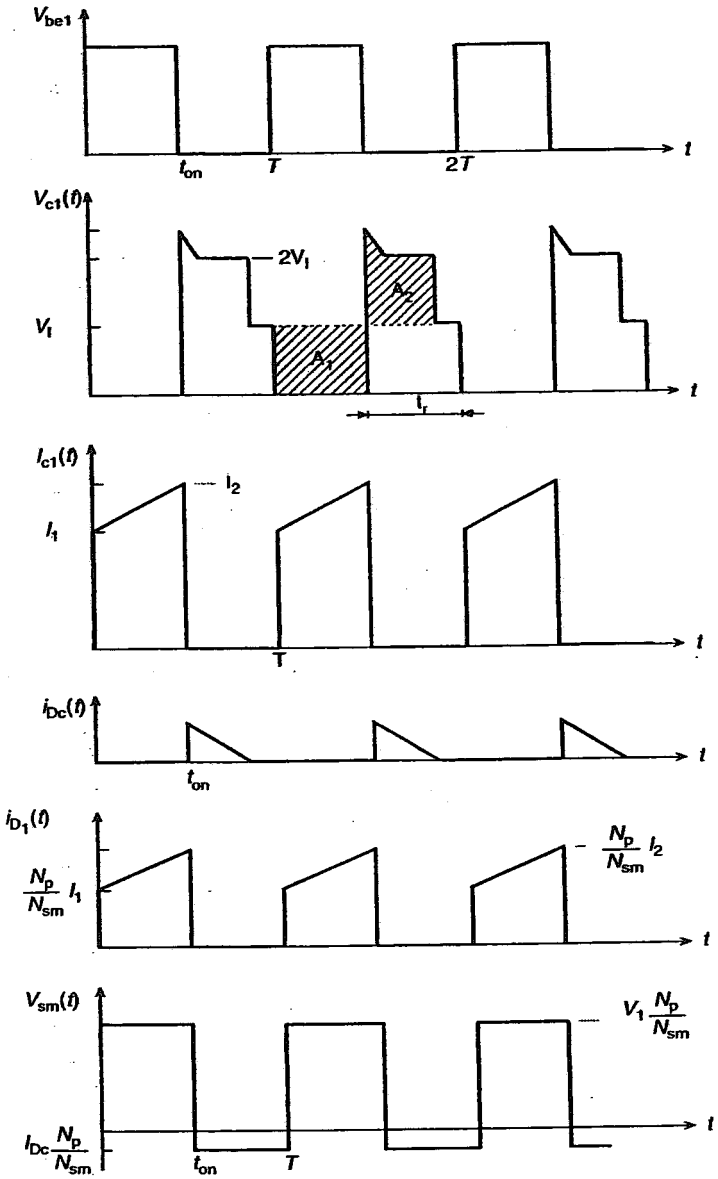

Figure 4.2 Switching waveforms of the forward converter for N_r/N_p.

is switched off, is due to the stray inductance in the collector circuit and leakage inductance in the transformer.

This is because the falling current of the switching transistor induces a positive-going spike at the collector according to

$$V_{lk} = L_{lk}\frac{di_c}{dt}, \tag{4.7}$$

where L_{lk} is the sum of the stray and leakage inductances in the collector circuit.

The clamp diode, D_c, conducts immediately after the switching transistor is switched off at t_{on}. Thus, the trapped energy in the primary winding is fed back to the input source. It remains conducting for a time t_r to satisfy the volt-second product given by

$$t_r\left(\frac{N_p}{N_r}V_i\right) = t_{on}V_i \tag{4.8a}$$

or

$$t_r = t_{on}\frac{N_r}{N_p}. \tag{4.8b}$$

This is because the magnetic core in the transformer must be completely reset before the beginning of the next switching cycle. In magnetic terms, the core must be restored to its original position on the hysteresis loop or the core will be saturated. Thus, the on-state volt-second products must be equal to the off-state volt-second products, as shown in the cross-hatched areas of A_1 and A_2, respectively, of Figure 4.2. The clamp diode, D_c, switches off after satisfying the volt-second requirement of the magnetic core. The collector voltage of the switching transistor is now equal to the input supply voltage, V_i, for N_r equals N_p. It is essential to choose a switching period greater than the sum of t_{on} and t_r to ensure that the magnetic core is reset before the start of the next switching cycle. If the transformer is completely reset before the next switching cycle, the maximum value of (t_r/T) is $(1 - D)$. Therefore, the maximum duty cycle, D_{max}, with a given turns ratio, N_r/N_p, is

$$(t_r/T)_{max} = (1 - D)_{max} = D_{max}(N_r/N_p) \tag{4.9a}$$

or

$$D_{max} = \frac{1}{1 + (N_r/N_p)}. \tag{4.9b}$$

The maximum duty cycle is 50% if the number of turns of the reset winding, N_r, is equal to the number of turns of the primary winding, N_p. The maximum duty cycle will be larger than 50% if the number of turns of the reset winding is smaller than the number of turns of the primary winding.

The voltage conversion ratio of the forward converter can be derived by imposing the constant volt-second relationship on the output inductor, L_{om}, of the master secondary output. The average voltages across the output inductor are $(V_i(N_{sm}/N_p) - V_{am})$ and $-V_{am}$ during the on-time and off-time, respectively. V_{am} is the average output voltage of the secondary master output. Thus,

$$\left(V_i\frac{N_{sm}}{N_p} - V_{am}\right)t_{on} + (-V_{am})t_{off} = 0. \tag{4.10}$$

The voltage conversion ratio is

$$V_{am} = V_i\left(\frac{N_{sm}}{N_p}\right)D. \tag{4.11}$$

It can be seen that the voltage conversion ratio of the forward converter is similar to that of the conventional buck converter. The turns ratio, N_{sm}/N_p, is to account for the voltage scaling of the transformer in the forward converter.

Following a similar analysis as in the buck converter, the peak-to-peak ripple current in the output inductor is

$$\Delta I_{om} = \frac{DV_i(N_{sm}/N_p)(1-D)}{f_sL_{om}}. \tag{4.12}$$

The output ripple voltage of the forward converter is

$$\Delta v_{om} = \frac{V_i\frac{N_{sm}}{N_p}D(1-D)}{8f_s^2L_{om}C_{om}}. \tag{4.13}$$

As can be seen, both the peak-to-peak inductor ripple current and output ripple voltage of the forward converter are similar to those of the conventional buck converter, except that they are scaled by the transformer turns ratio, (N_{sm}/N_p).

The forward converter has a low output ripple voltage. However, it has a poor transient response and its efficiency is low due to poor transformer utilization. Thus, the size and weight of the transformer is a major factor in choosing the forward converter for a specific application.

Example 4.1. The forward converter shown in Figure 4.1 has an input supply voltage of 60 V and an average output voltage of 5 V at the secondary master output. The switching frequency is 1 kHz with a maximum output inductor ripple current of 0.1 A. The number of turns in the primary winding is 60 and the turns ratio, N_r/N_p, is equal to one. Determine (a) the smallest number of turns in the secondary master winding N_{sm}, and (b) the output filter inductance L_{om}.

Solution.

(a) From Equation (4.9b), the maximum duty cycle D_{max} is

$$D_{max} = \frac{1}{1 + (N_r/N_p)} = \frac{1}{1+1} = 0.5.$$

From Equation (4.11),

$$\left(\frac{N_{sm}}{N_p}\right)_{min} D_{max} = \frac{V_a}{V_s} = \frac{5}{60}.$$

Therefore, the smallest number of turns in the secondary winding is

$$(N_{sm})_{min} = N_p\left(\frac{5}{60}\right)\frac{1}{D_{max}} = 60\left(\frac{5}{60}\right)\frac{1}{0.5} = 10 \text{ turns}.$$

(b) From Equation (4.12),

$$L_{om} = \frac{DV_i(N_{sm}/N_p)(1-D)}{f_s \Delta I_{om}} = \frac{0.5(60)(10/60)(1-0.5)}{1000(0.1)} \leq 0.025\text{H} \leq 25\text{mH}.$$

4.3 PUSH–PULL CONVERTER

The push–pull converter is derived from two forward converters working in antiphase. As such, the push–pull converter topology has the advantage over the forward converter in that the voltage across the transformer and, hence, the peak collector voltage of the switching transistor is limited to twice the input voltage. This is due to the symmetrical center-tapped transformer with equal number of turns in the primary windings. Since the power supplied to the load is never stored in the transformer, more power can be handled at a greater efficiency and with a better regulation than the forward converter. The basic circuit schematic of a push–pull converter is shown in Figure 4.3. The switching transistors, Q_1 and Q_2, alternately conduct each half cycle at a

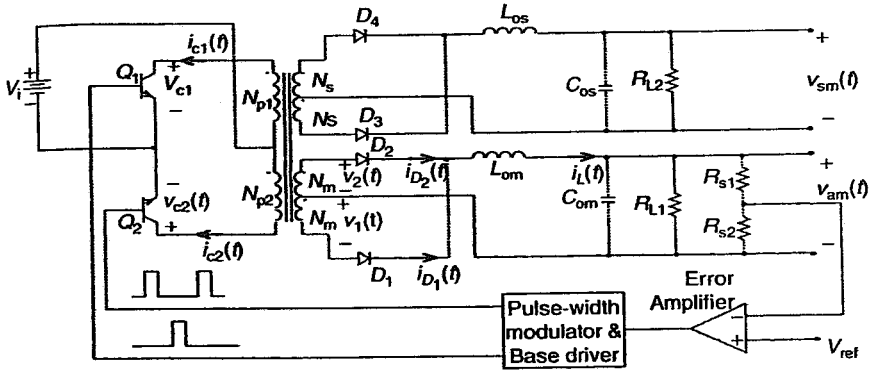

Figure 4.3 Circuit schematic of the push–pull converter.

duty cycle determined by the input supply voltage, V_i, transformer turn ratio, and the desired output voltage. Thus, the maximum duty cycle attainable is slightly less than 50% to account for the turn-off times of the switching transistors. Otherwise, "shoot through" will occur in the two switching transistors, resulting in irreversible damage to them. This "shoot through" phenomenon can be avoided by defining a dead time, t_d, between the turn-on of Q_2 and the turn-off of Q_1 switching transistors. The dead time t_d should, at least, be equal to turn-off times of the switching transistors.

When the switching transistor, Q_1, is switched on during the first half of the switching period, all the undotted ends of the transformer windings are now positive as the input supply voltage is applied across the primary winding, N_{p1}. Its collector current, $i_{c1}(t)$, increases linearly from I_1 to I_2 in time t_{on} as shown in Figure 4.4. The collector of the switching transistor, Q_2, is now at twice the input supply voltage since both the primary windings have the same number of turns.

The voltage at the anode of the rectifier D_1 is a rectangular waveform of the input supply voltage, V_i, except it is scaled by the turns-ratio of the transformer:

$$v_1 = V_i \frac{N_m}{N_p}, \tag{4.14}$$

where $N_p \leq N_{p1} \leq N_{p2}$. The rectifier D_1 is now forward-biased. Thus, the output inductor, L_{om}, is charged during this time interval. The current flowing through the rectifier D_1, $i_{D_1}(t)$, is a scaled version of the collector current, $i_{c1}(t)$:

$$i_{D_1}(t) = i_{c1}(t) \frac{N_p}{N_m}. \tag{4.15}$$

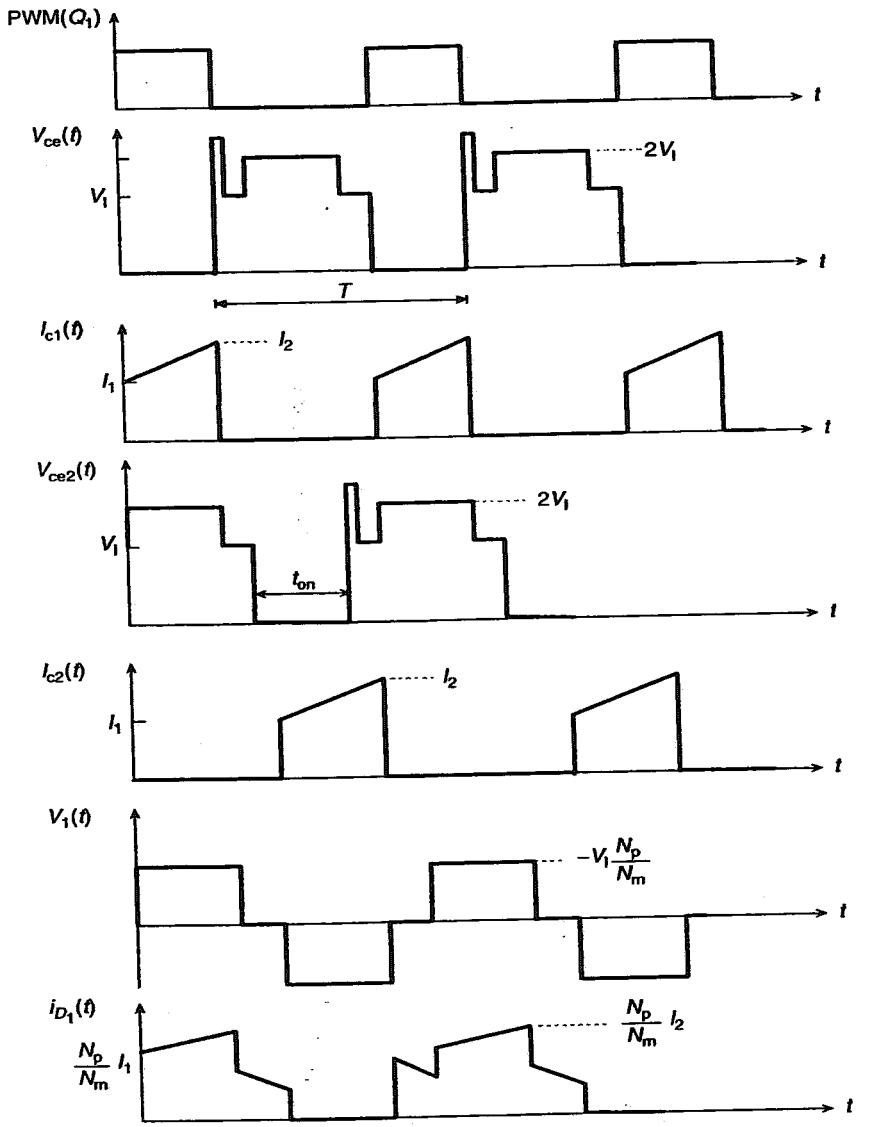

Figure 4.4 Waveforms of the push–pull converter.

The switching transistor, Q_1, is switched off at $t \leq t_{on}$. It should be noted that t_{on} must be less than half the switching period to accommodate the turn-off time of the switching transistor. As the switching transistor, Q_1, is switched off, a voltage spike appears at its collector due to the induced voltage caused by the falling collector current and the stray and leakage inductances in the collector circuit. The collector voltage momentarily drops to the input supply voltage after the trapped energy is dissipated. The collector voltages of the two switching transistors are now at the input supply voltage since both are switched off. As the collector current in Q_1 drops abruptly to zero at t_{on}, a ledge current continues to flow through the rectifiers before the other switching transistor, Q_2, is switched on as shown in Figure 4.5. This ledge current is due to the voltage reversal of the output inductor, L_{om}, as the switching transistor, Q_1, is switched off.

The negative voltage at the cathodes of both rectifiers causes them to be forward-biased. Each rectifier is now carrying half the total current in the inductor. Hence, the rectifiers in the push–pull converter perform the function of freewheeling as in a conventional buck converter.

The voltage conversion ratio of the push–pull switching converter can be derived by imposing the constant volt-second relationship on the output

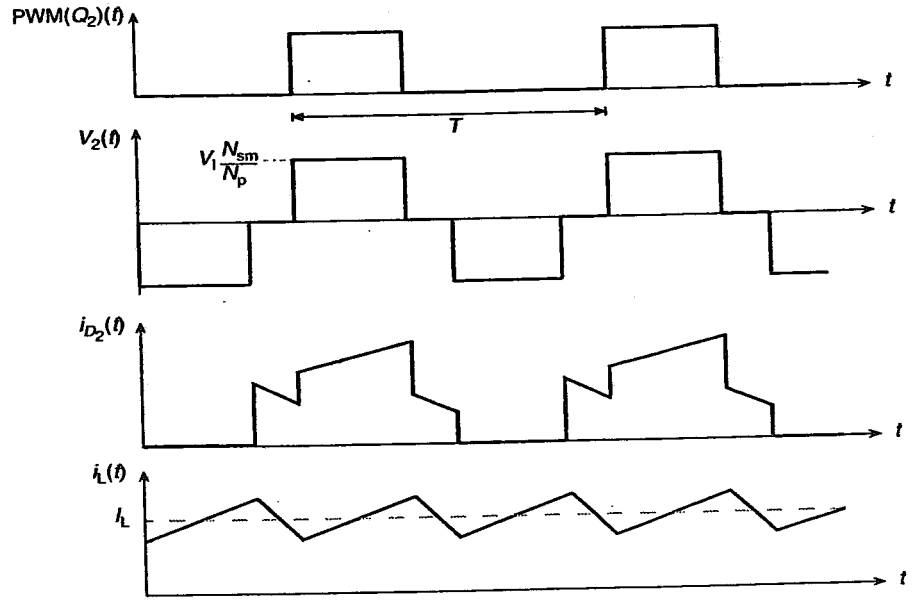

Figure 4.5 Output waveforms of the push–pull converter.

inductor, L_{om}. Neglecting the on-state voltages of the switching transistor and the rectifier, the average voltage across the output inductor, when either one of the switching transistors is switched on, is $(V_i(N_m/N_p) - V_{am})$. During the freewheeling of the rectifiers, the average voltage across the output inductor is $-V_{am}$. Thus

$$\left(V_i\frac{N_m}{N_p} - V_{am}\right)2t_{on} - V_{am}(T - 2t_{on}) = 0. \tag{4.16}$$

The factor of 2 for t_{on} is to account for the fact that the output inductor is charged twice in one switching cycle. The voltage conversion ratio is

$$V_{am} = V_i\left(\frac{N_m}{N_p}\right)\left(\frac{2t_{on}}{T}\right) \tag{4.17}$$

or

$$V_{am} = [(V_i - V_{cesat})\frac{N_m}{N_p} - V_d]\frac{2t_{on}}{T} \tag{4.18}$$

when the on-state voltages of the switching transistors and rectifiers are taken into consideration. The most common failure mode in the push–pull converter with bipolar switching transistors is caused by a flux imbalance in the transformer. This occurs when the volt-second products across the two primary windings are not equal to each other. When this occurs, the magnetic core will not return to its original starting point in its hysteresis loop after a switching cycle. After a number of switching cycles, the magnetic core will saturate. Once in saturation, the magnetic core will not be able to support the applied input voltage. Thus, the bipolar switching transistors are subjected to high current and high voltage situations and may eventually be destroyed due to thermal run-away. This failure mode is less severe in the push–pull converter with power MOSFET switching transistors. This is due to the negative temperature coefficient of the drain current in power MOSFETs. As the device temperature increases in a power MOSFET due to a flux imbalance problem, its drain current tends to decrease. Thus, thermal runaway caused by flux imbalance in the transformer is mitigated in the push–pull converter with the use of power MOSFETs.

4.4 HALF-BRIDGE SWITCHING CONVERTER

The half-bridge topology is primarily used in off-line switching converters since their switching transistors are not subjected to twice the input supply

voltage as in the forward and push–pull switching converters. Figure 4.6 shows the circuit schematic of a half-bridge switching converter. As shown, the undotted end of the transformer is connected to the common terminal of the two identical filter capacitors, C_{f1} and C_{f2}, via a DC blocking capacitor, C_b. The DC blocking capacitor can be omitted in some applications. A drop in primary voltage will result due to the charging of this capacitor by the current flowing in the transformer. The input supply voltage, V_i, is divided between the two filter capacitors. Thus, the common terminal of the filter capacitors has an average voltage of $V_i/2$. The purpose of the DC blocking capacitor, C_b, is to avoid the flux imbalance problem caused when the voltage at the common terminal is not exactly half the input supply voltage. The dotted end of the transformer is connected to the common terminal of the switching transistors configured in a totem-pole configuration. The switching transistors, Q_1 and Q_2, alternately conduct each half cycle of a switching cycle. Thus, the two switching transistors alternately connect the dotted end of the transformer to V_i or ground, while the undotted end of the transformer is maintained at $V_i/2$. When the switching transistor, Q_1, is switched on, the voltage at the dotted end of the primary winding is now V_i. The voltage across the primary winding is $V_i/2$, since the undotted end is maintained at $V_i/2$. Thus, the polarity of the voltages at all the dotted ends of the secondary windings is positive. The collector of Q_2 is at V_i as long as Q_1 remains conducting. The rectifier, D_2, conducts and the output inductor, L_o, is charged during this time interval. When Q_1 is switched off at $t \leq t_{on}$, the dotted end of the transformer is now grounded by the switching transistor, Q_2. The undotted ends of the transformer windings are now

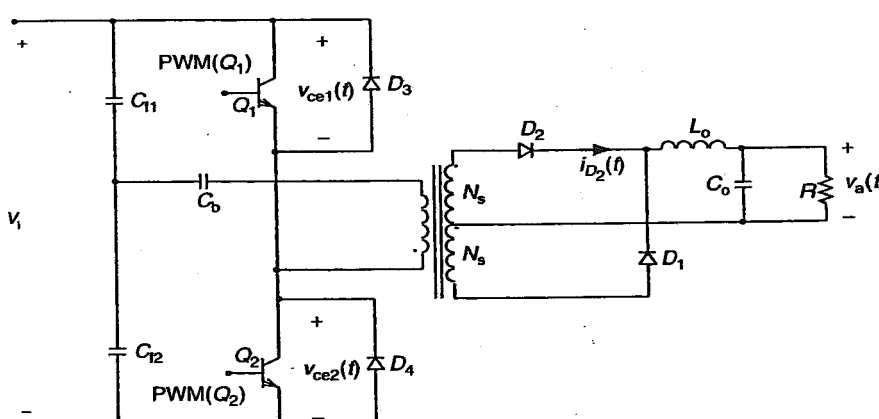

Figure 4.6 Circuit schematic of a half-bridge converter.

positive with respect to the dotted ends. Rectifier D_1 is now forward-biased and the output inductor is charged. It is obvious that the voltage across the primary winding is always maintained at half the input supply voltage. During the interval between the on-time of the two switching transistors, the two rectifiers, D_1 and D_2, are freewheeling as the energy stored in the output inductor, L_o, is transferred to the output capacitor and the load as the ledge current. Figure 4.7 shows the switching waveforms of the half-bridge switching converter.

The voltage conversion ratio of the half-bridge switching converter can be derived by imposing the constant volt-second relationship on the output inductor. The average voltages across the output inductor are $[(V_i/2)\,(N_s/N_p) - V_a]$ and $-V_a$ during t_{on} and t_{off}, respectively. Thus

$$\left(\frac{V_i}{2}\frac{N_s}{N_p} - V_a\right)\frac{2t_{on}}{T} - V_a\frac{t_{off}}{T} = 0. \tag{4.19}$$

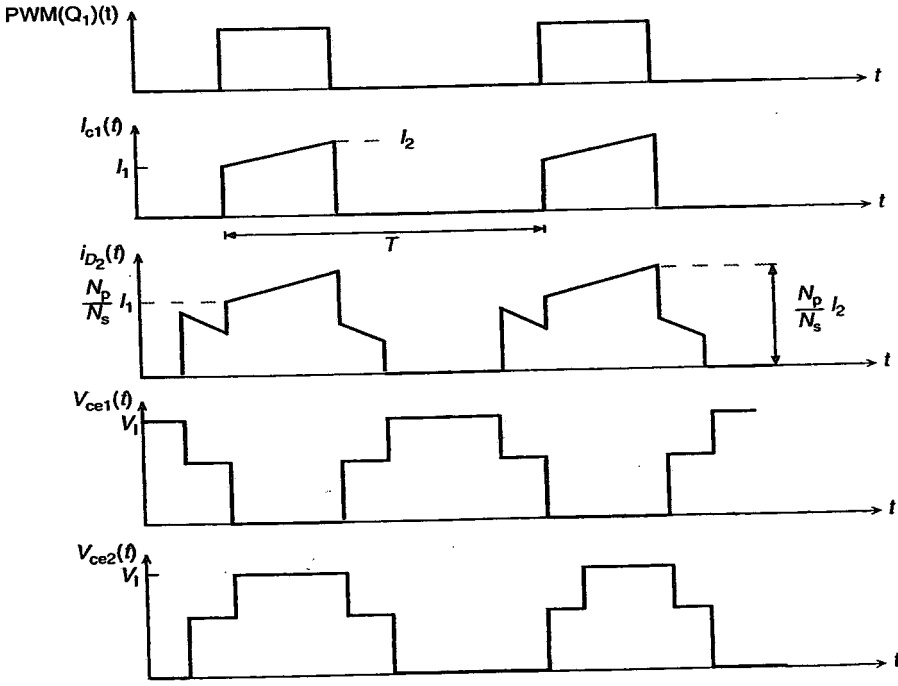

Figure 4.7 Waveforms for the half-bridge converter.

The factor of 2 for t_{on} is to account for the fact the output inductor is charged twice in one switching cycle. The voltage conversion ratio is

$$V_a = V_i\left(\frac{N_s}{N_p}\right)2\left(\frac{t_{on}}{T}\right) \tag{4.20a}$$

or

$$V_a = \left[\left(\frac{V_i}{2} - V_{ce}\right)\frac{N_s}{N_p} - V_d\right]2\left(\frac{t_{on}}{T}\right) \tag{4.20b}$$

when the on-state voltages of the switching transistors and rectifiers are taken into consideration.

The half-bridge switching converter requires a more complex control circuitry. An isolated driver is required for the switching transistor, Q_1, since its emitter is not directly connected to ground. The filter capacitors are usually bulky and costly since they have to handle the full primary current. The full-wave output of the half-bridge switching converter results in the use of smaller output inductor and capacitor when compared to the forward converter. The other important feature of the half-bridge switching converter is that the leakage inductance spikes are clamped to the input supply bus. Thus, any energy stored in the leakage inductance is conducted back to the input bus instead of having to be dissipated in some resistive elements.

4.5 FULL-BRIDGE SWITCHING CONVERTER

The full-bridge converter topology is primarily used in off-line switching converters since their switching transistors are only subjected to the magnitude of the input supply voltage V_i. Figure 4.8 shows the circuit schematic of a full-bridge converter. As shown, the switching transistors are configured in a full- or half-bridge topology. The switching transistor pairs of $Q_1 - Q_4$ and $Q_2 - Q_3$ are switched on alternately during each half cycle of a switching period. When the transistor pair, $Q_1 - Q_4$, is switched on, the dotted end of the primary winding is connected to the input supply voltage, V_i, while the undotted end of the primary winding is connected to near ground potential. Thus, all the dotted ends of the secondary windings are now positive with respect to their undotted ends. The output rectifier, D_2, conducts and delivers the energy to the output inductor. The voltage at the secondary winding is a scaled version of the primary winding voltage. When the transistor pair, $Q_2 - Q_3$, is switched on, the undotted end of the primary winding is now at V_i, while the dotted end is at near ground potential. The output rectifier, D_1, conducts and delivers energy to charge the output

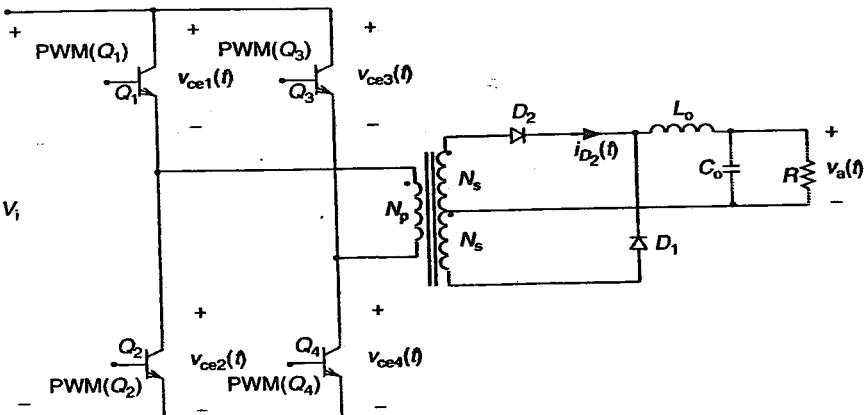

Figure 4.8 Circuit schematic of a full-bridge converter.

inductor. The rectifiers, D_1 and D_2, are freewheeling when both the switching transistor pairs are switched off. Figure 4.9 shows the switching waveforms of the full-bridge converter.

The voltage conversion ratio of the full-bridge converter can be derived by imposing the constant volt-second relationship on the output inductor. The average voltages across the output inductor are $[V_i(N_s/N_p) - V_a]$ and $-V_a$ during t_{on} and t_{off}, respectively. Thus

$$\left(V_i \frac{N_s}{N_p} - V_a\right)\frac{2t_{on}}{T} - V_a \frac{2t_{off}}{T} = 0. \tag{4.21}$$

The voltage conversion ratio is

$$\frac{V_a}{V_i} = 2\left(\frac{N_s}{N_p}\right)\left(\frac{t_{on}}{T}\right), \tag{4.22a}$$

or

$$\frac{V_a}{V_i} = 2\left(\frac{N_s}{N_p}\right)D. \tag{4.22b}$$

The output power of the full-bridge converter is double that of the half-bridge converter because the full input supply voltage, rather than half, is applied to the primary winding. The full-bridge converter has good transformer utilization. However, it requires a more complex driver circuitry that is capable of driving high-side and low-side switching transistors. The flux imbalance is also a potential problem in the full-bridge converter.

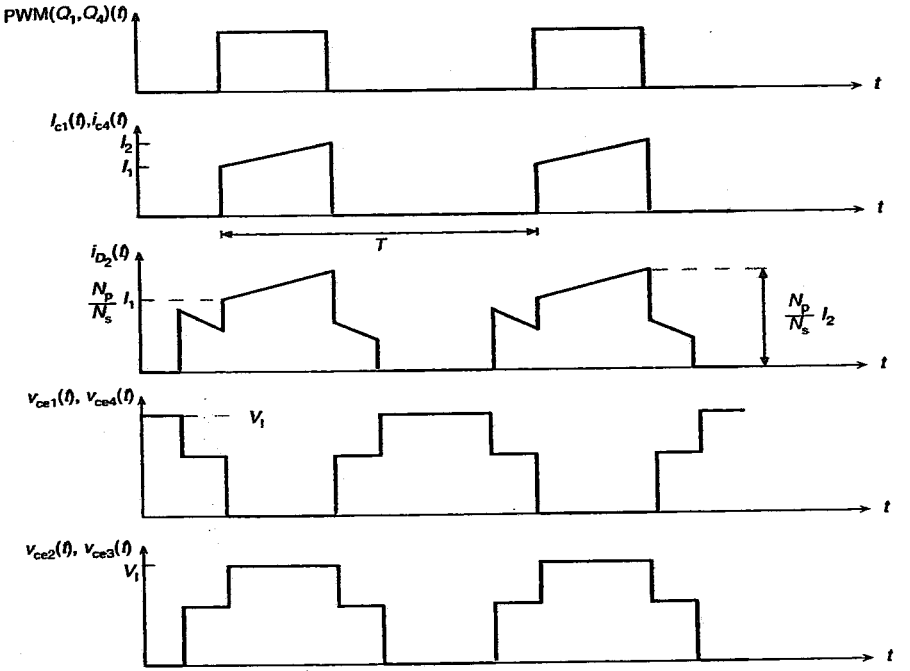

Figure 4.9 Waveforms for the full-bridge converter.

4.6 FLYBACK CONVERTER

The flyback converter is widely used for high voltage as well as offline power supplies applications. It is essentially a constant-output-power switching converter. An output inductor is not required for the flyback converter. As such, it is attractive for multiple output application with a better output voltage tracking than most other switching converter topologies. The savings in cost and size, due to the absence of the output inductor, is a significant advantage over other switching converter topologies.

Figure 4.10 shows the circuit schematic of a flyback converter. When the switching transistor, Q_s, is switched on at $t \leq 0$, the dotted ends of the windings are negative with respect to the undotted ends. As such, the output rectifier, D_1, is reverse-biased. During this time interval, the output load current is maintained by the output capacitor, C_o. It should be noted that a

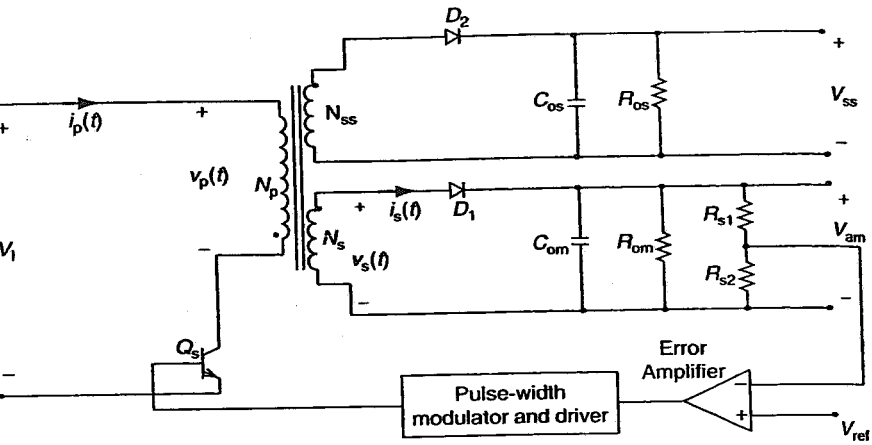

Figure 4.10 Circuit schematic of a flyback.

freewheeling diode is not required for the flyback converter. Neglecting the on-state collector-to-emitter voltage drop of the switching transistor, Q_s, the current in the primary winding increases linearly at a rate determined by

$$\frac{di_p}{dt} = \frac{V_i}{L_p}, \tag{4.23}$$

where L_p is the magnetizing inductance of the primary winding. The peak primary current, $I_{p,max}$, is given by

$$I_{p,max} = \frac{V_i}{L_p} t_{on}, \tag{4.24}$$

where t_{on} is the on-time of the switching transistor. It can be seen that the maximum input current, $I_{p,max}$ does not depend on load variation. Thus, the flyback converter delivers a constant power.

The switching transistor is switched off at $t \leq t_{on}$. Since the current flowing in the primary winding cannot change instantaneously, the voltage across the primary winding reverses its polarity. As such, the dotted ends of the windings are now positive with respect to the undotted ends. The output rectifier, D_1, is now forward-biased and current flows from the secondary winding. The current in the secondary winding decreases linearly at a rate determined by

$$\frac{di_s}{dt} = \frac{V_s}{L_s}, \tag{4.25}$$

where L_s is the magnetizing inductance of the secondary winding and V_s is the voltage across the master secondary winding. The peak secondary current, $I_{s,max}$, is related to the peak primary current and is given by

$$I_{s,\max} = \left(\frac{N_p}{N_s}\right) I_{p,\max}. \tag{4.26}$$

If the current in the secondary winding has decreased to zero before the switching transistor switches on again as shown in Figure 4.11, the flyback converter is said to be operating in the discontinuous mode of operation. Thus, the flyback converter first stores the energy in the trans-

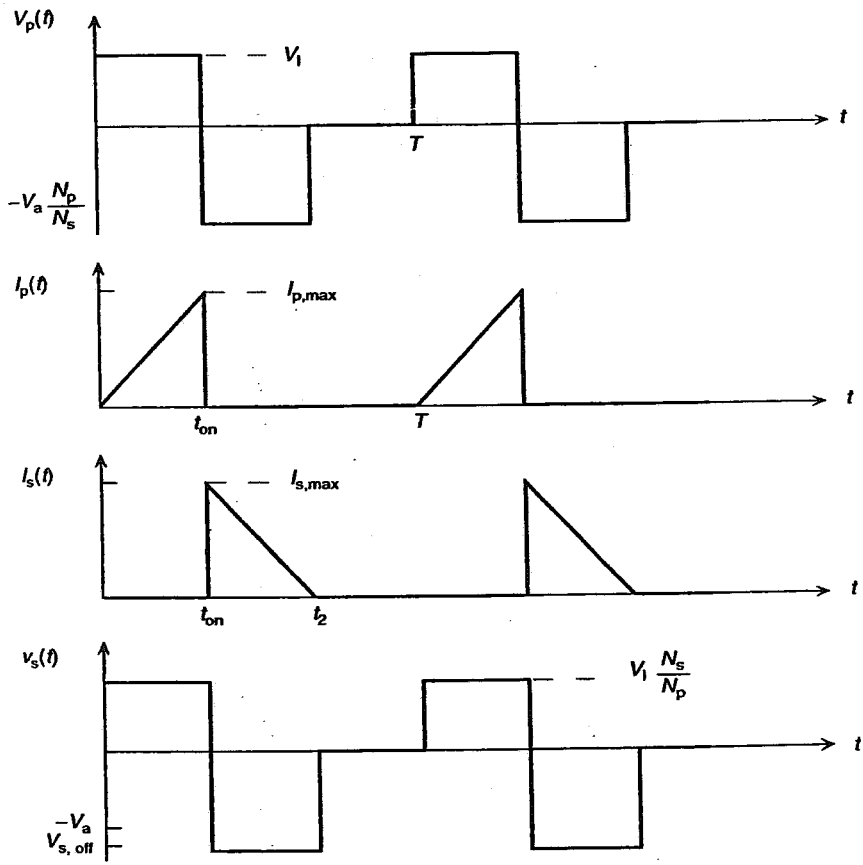

Figure 4.11 Waveforms for the discontinuous-mode flyback converter.

former during the on-time, and subsequently, transfers this energy to the load during the off-time of the switching transistor. The input power, P_i, is defined as

$$P_i = \frac{L_p(I_{p,max})^2}{2T}. \tag{4.27a}$$

From Equation (4.24), the input power can also be expressed as

$$P_i = \frac{(V_i t_{on})^2}{2TL_p}. \tag{4.27b}$$

Since the flyback converter is a constant-power switching converter, its output voltage is maintained by keeping the product $V_i t_{on}$ constant. The efficiency of this converter is defined as

$$\eta = \frac{P_{out}}{P_i} = \frac{(1/2T)I_{s,max}^2}{(1/2T)L_p I_{p,max}^2} = \frac{L_s}{L_p}\left(\frac{I_{s,max}}{I_{p,max}}\right)^2. \tag{4.28}$$

The relationship between the primary and secondary winding currents can be found from Equation (4.28) as:

$$I_{s,max} = \sqrt{\eta}\sqrt{\frac{L_p}{L_s}} I_{p,max}, \tag{4.29a}$$

or

$$I_{s,max} = \sqrt{\eta}\left(\frac{N_p}{N_s}\right) I_{p,max}, \tag{4.29b}$$

since $(N_p/N_s)^2 = (L_p/L_s)$. The average load current, I_a, can be found by integrating the current in the secondary winding over a switching period, T:

$$I_a = \frac{1}{2} I_{s,max}\left(\frac{t_2}{T}\right). \tag{4.30}$$

From Equation (4.30), t_2 can be found:

$$t_2 = \sqrt{\frac{V_a N_p}{V_i N_s}\frac{2L_s}{fR}}, \tag{4.31}$$

where R is the load resistance.

The flyback converter is said to be operating in the continuous mode of operation if the switching transistor is switched on while energy is dumped into the load. The switching waveforms of a continuous mode flyback converter are shown in Figure 4.12. When the switching transistor is switched on at $t \leq 0$, the current in the primary winding increases linearly from a minimum value of $I_{p,min}$ to a maximum value of $I_{p,max}$ in time t_{on} according to:

$$V_i = L_p \frac{I_{p,max} - I_{p,min}}{t_{on}}. \tag{4.32}$$

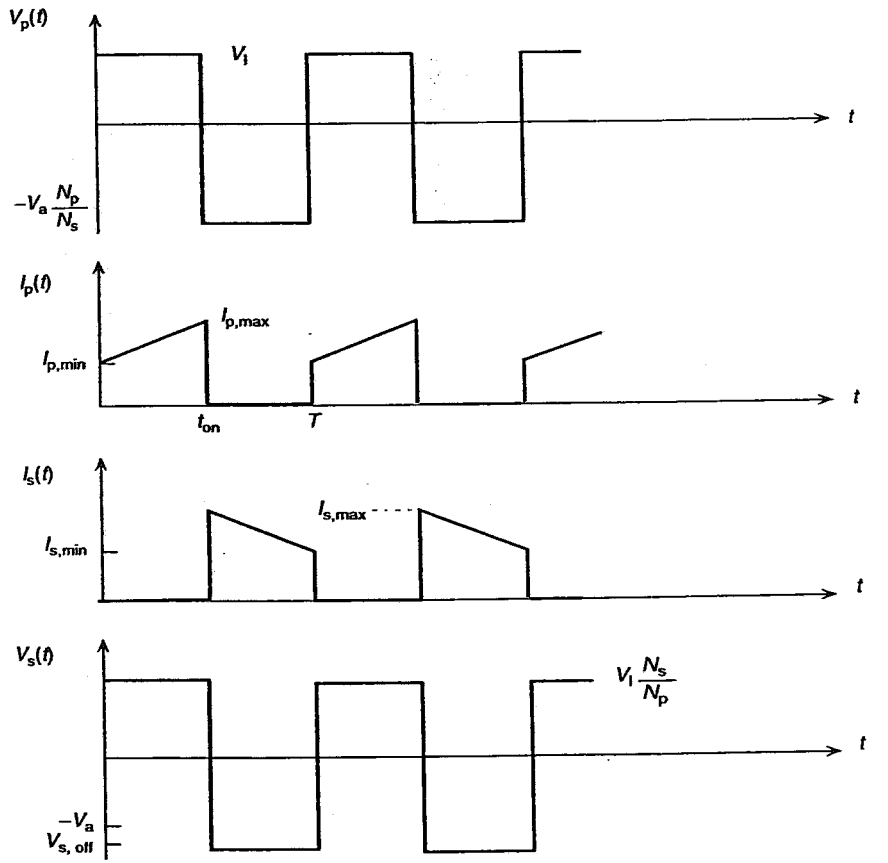

Figure 4.12 Waveforms for the continuous-mode flyback converter.

When the switching transistor is switched off at $t \leq t_{on}$, current appears in the secondary winding and decreases linearly from a maximum value of $I_{s,max}$ to a minimum value of $I_{s,min}$ in time t_{off} according to:

$$V_s = L_s \frac{I_{s,max} - I_{s,min}}{t_{off}}, \tag{4.33}$$

where L_s is the inductance in the secondary winding.

Since the switching transistor is switched on again before the secondary current drops to zero, it is transferred back to the primary through the current, $I_{p,min}$. The secondary current is related to the primary current through the inverse turns-ratio of the transformer:

$$I_{s,max} - I_{s,min} = \frac{N_p}{N_s}(I_{p,max} - I_{p,min}). \tag{4.34}$$

The average output current, I_a, is

$$I_a = \frac{I_{s,max} + I_{s,min}}{2} \frac{t_{off}}{T}. \tag{4.35}$$

The average output voltage, V_a, of the flyback converter operating in the continuous mode is

$$V_a = V_i \left(\frac{N_s}{N_p}\right) \frac{D}{(1-D)}. \tag{4.36}$$

The off-state collector voltage of the switching transistor is

$$V_c = V_i + \frac{N_p}{N_s} V_a. \tag{4.37}$$

The discontinuous mode flyback converter is suited for those applications, which require a constant output current, while the continuous mode flyback converter is suited for applications that require a constant output voltage. The discontinuous mode flyback converter responds more rapidly and with a lower transient output voltage spike to sudden changes in load current or input voltage when compared to the continuous mode flyback converter. However, the peak currents in the discontinuous mode are larger than those in the continuous mode. As such, the discontinuous mode flyback converter requires a flyback transformer with a larger current rating and output capacitor with a larger ripple current rating than those required in the continuous mode flyback converter. The design of the flyback transformer

[3–5] is also critical due to poor transformer utilization. The input supply is isolated from the load so that faults, which occur on the secondary, are not directly reflected to the primary. The flyback converter also has a high output ripple voltage due to the absence of the output inductor. Three flyback converter designs are evaluated in Chapter 10.

Example 4.2. The continuous-mode flyback converter shown in Figure 4.10 has an input voltage of 50 V and an average output voltage of 100 V. The magnetizing inductance of the primary winding, L_p, is 1 mH. The turns ratio, (N_s/N_p), is 4. For a switching frequency, f_s, of 1 kHz, determine (a) the duty cycle and (b) the magnetizing inductance of the secondary winding.

Solution.

(a) From Equation (4.36),

$$\frac{D}{(1-D)} = \left(\frac{V_a}{V_i}\right)\left(\frac{N_p}{N_s}\right) = \left(\frac{100}{50}\right)\left(\frac{1}{4}\right) \leq 0.5.$$

Therefore, the required duty cycle is

$$D = \frac{0.5}{1.5} = 0.333.$$

(b) The magnetizing inductance in the secondary winding, L_s, is

$$L_s = L_p\left(\frac{N_s}{N_p}\right)^2 = (1\,\text{mH})(4)^2 = 16\,\text{mH}.$$

4.7 ZERO-CURRENT-SWITCHING QUASI-RESONANT HALF-BRIDGE CONVERTER [2]

The circuit schematic of a ZCS, half-wave, quasi-resonant half-bridge converter with secondary-side resonance is shown in Figure 4.13. As shown, it is similar to the conventional half-bridge converter except for the resonant capacitor, C_r, connected across the freewheeling diode, D_{fw}. The secondary-side resonant ZCS quasi-resonant converter makes use of the leakage inductance, L_r, of the transformer as the resonant inductor. The operation of this converter can be divided into four modes. All components, except the transformer, are assumed to be ideal. The output inductor, L_o, is much larger than the leakage inductance of the transformer, L_r. Thus, the output inductor, output capacitor, and the load, can be modeled as a constant

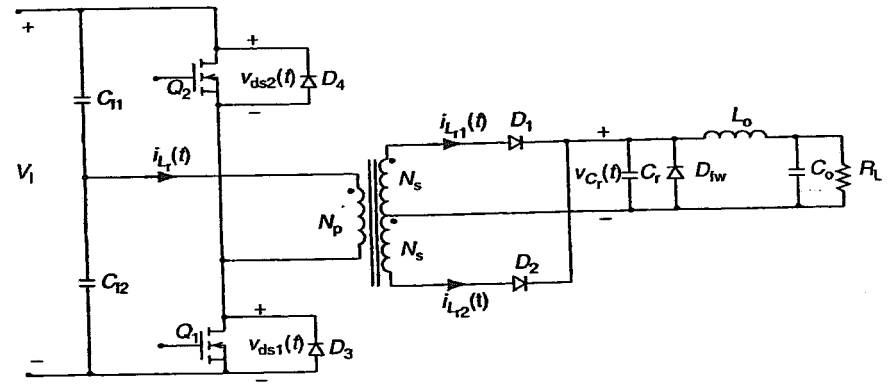

Figure 4.13 Circuit schematic of a ZCS, half-wave, quasi-resonant half-bridge converter.

current sink of I_o. Suppose before the switching transistor, Q_1, is switched on, the freewheeling diode, D_{fw}, carries the steady-state output current, I_o, and the voltage across the resonant capacitor, V_{C_r} ($t \leq 0$), is clamped at zero volt by the freewheeling diode.

Mode 1 ($0 < t \leq t_1$)

Mode 1 begins when the switching transistor, Q_1, switches on at $t = 0$. The current in the upper secondary winding of the transformer, $i_{L_r}(t)$, increases linearly from zero to the steady-state output current of I_o. Its equivalent circuit is shown in Figure 4.14.

The voltage across the upper secondary winding is related to the rate of rise of its current. At the end of mode 1, the voltage across the upper secondary winding, $v_{s,upper}(t_1)$, is given by

$$v_{s,upper}(t_1) = \frac{V_I N_s}{2N_p} = L_r \frac{I_o}{T_1}, \tag{4.38}$$

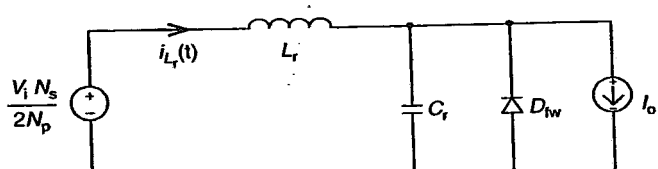

Figure 4.14 Mode 1 equivalent circuit for the ZCS, half wave, quasi-resonant half-bridge converter.

where N_s and N_p are the numbers of turns in the secondary and primary windings, respectively. The duration of mode 1, T_1, is

$$T_1 = \frac{2L_r I_o N_p}{V_i N_s}. \tag{4.39}$$

Thus, mode 1 is characterized by charging of the leakage inductance of the transformer and the storage of electrical energy in magnetic form in the resonant inductor.

Mode 2 ($t_1 < t \leq t_2$)

Mode 2 begins when the current flowing through the upper secondary winding reaches the steady-state output current of I_o. Its equivalent circuit is shown in Figure 4.15.

The voltage across the resonant capacitor, $v_{C_r}(t)$, increases, as it is charged by the difference between the input current, $i_{L_r}(t)$, and output steady-state current, I_o (i.e., $i_{L_r}(t) - I_o$). The freewheeling diode, D_{fw}, is reverse-biased as the voltage across the resonant capacitor increases according to

$$\mathrm{d}\frac{v_{C_r}}{\mathrm{d}t} = \frac{i_{L_r}(t) - I_o}{C_r}. \tag{4.40}$$

The current in the upper secondary winding, $i_{L_r}(t)$, continues to increase in a sinusoidal fashion according to

$$L_r \frac{\mathrm{d}i_{L_r}}{\mathrm{d}t} = \frac{V_i N_s}{2N_p} - v_{C_r}(t). \tag{4.41}$$

The above two first-order differential equations can be solved using the following initial conditions:

$$v_{C_r}(t_1) = 0, \quad i_{L_r}(t_1) = I_o. \tag{4.42}$$

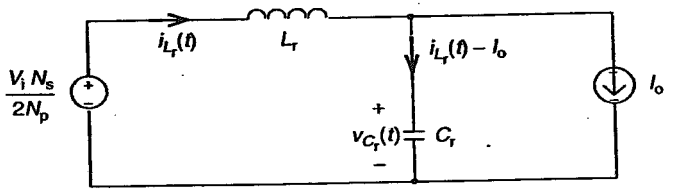

Figure 4.15 Mode 2 equivalent circuit for the ZCS, half wave, quasi-resonant half-bridge converter.

The expression for the resonant inductor current, $i_{L_r}(t)$, is

$$i_{L_r}(t) = I_o + \frac{V_i N_s}{2N_p Z_n} \sin(w_n t) \tag{4.43}$$

and the expression for the resonant capacitor voltage, $v_{C_r}(t)$, is

$$v_{C_r}(t) = \frac{V_i N_s}{2N_p}[1 - \cos(\omega_n t)], \tag{4.44}$$

where $Z_n = \sqrt{L_r/C_r}$ is the characteristic impedance and $\omega_n = 1/\sqrt{L_r C_r}$ is the resonant frequency. Zero-current switching requires that

$$Z_n \leq \frac{V_i N_s}{2N_p I_o}. \tag{4.45}$$

Mode 2 ends when the current in the resonant inductor, $i_{L_r}(t)$, reaches zero. At this time, the switching transistor, Q_1, should be switched off to take advantage of the ZCS condition. The duration of mode 2 can be found by setting Equation (4.43) to zero and solving for $T_2 = t_2 - t_1$:

$$i_{L_r}(T_2) = I_o + \frac{V_i N_s}{2N_p Z_n} \sin(\omega_n T_2) = 0. \tag{4.46}$$

Thus,

$$T_2 = \frac{\sin^{-1}\left[-(2I_o Z_n N_p / V_i N_s)\right]}{\omega_n} = \frac{\alpha}{\omega_n}, \tag{4.47}$$

where α takes on values between π and $3\pi/2$.

Mode 3 ($t_2 < t \leq t_3$)

Mode 3 begins when the current flowing through the resonant inductor, $i_{L_r}(t)$, decreases to zero. Its equivalent circuit is shown in Figure 4.16. Since the unidirectional switching transistor, Q_1, prevents current reversal through the resonant inductor, the resonant capacitor begins to discharge its stored energy to the output. The freewheeling diode, D_{fw}, is still reverse-biased by the voltage across the resonant capacitor. The voltage across the resonant capacitor decreases linearly according to

$$C_r \frac{dv_{C_r}}{dt} = \frac{V_i N_s}{2N_p}(1 - \cos\alpha) - \frac{I_o t}{C_r}. \tag{4.48}$$

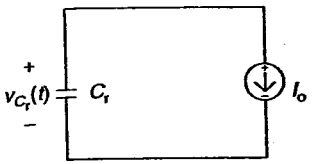

Figure 4.16 Mode 3 equivalent circuit for the ZCS, half wave, quasi-resonant half-bridge converter.

Mode 3 ends when the voltage across the resonant capacitor becomes zero. The duration of mode 3, T_3, is

$$T_3 = \frac{C_r V_i N_s}{2N_p I_o}(1 - \cos\alpha). \tag{4.49}$$

Mode 4 ($t_3 < t \leq T_s/2$)

Mode 4 begins when the voltage across the resonant capacitor decreases to zero at time $t = t_3$. The freewheeling diode, D_{fw}, starts to conduct and the output current is freewheeling through it. Its equivalent circuit is shown in Figure 4.17. The duration of mode 4 is

$$T_4 = \frac{T_s}{2} - T_1 - T_2 - T_3, \tag{4.50}$$

where T_s is the switching period.

Figure 4.18(a) and (b) shows the switching waveforms of the ZCS, quasi-resonant half-bridge converter. The voltage conversion ratio of this converter can be derived by imposing the constant volt-second relationship on the output inductor, L_o. The average voltages across the output inductor are $((V_i N_s/2N_p) - V_a)$ and $-V_a$ during the resonant period T_n and $((T_s/2) - T_n)$ intervals, respectively. Thus,

$$\left(\frac{V_1 N_s}{2N_p} - V_a\right) T_n - V_a\left(\frac{T_s}{2} - T_n\right) = 0. \tag{4.51}$$

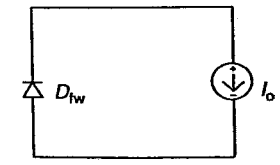

Figure 4.17 Mode 4 equivalent circuit for the ZCS, half wave, quasi-resonant half-bridge converter.

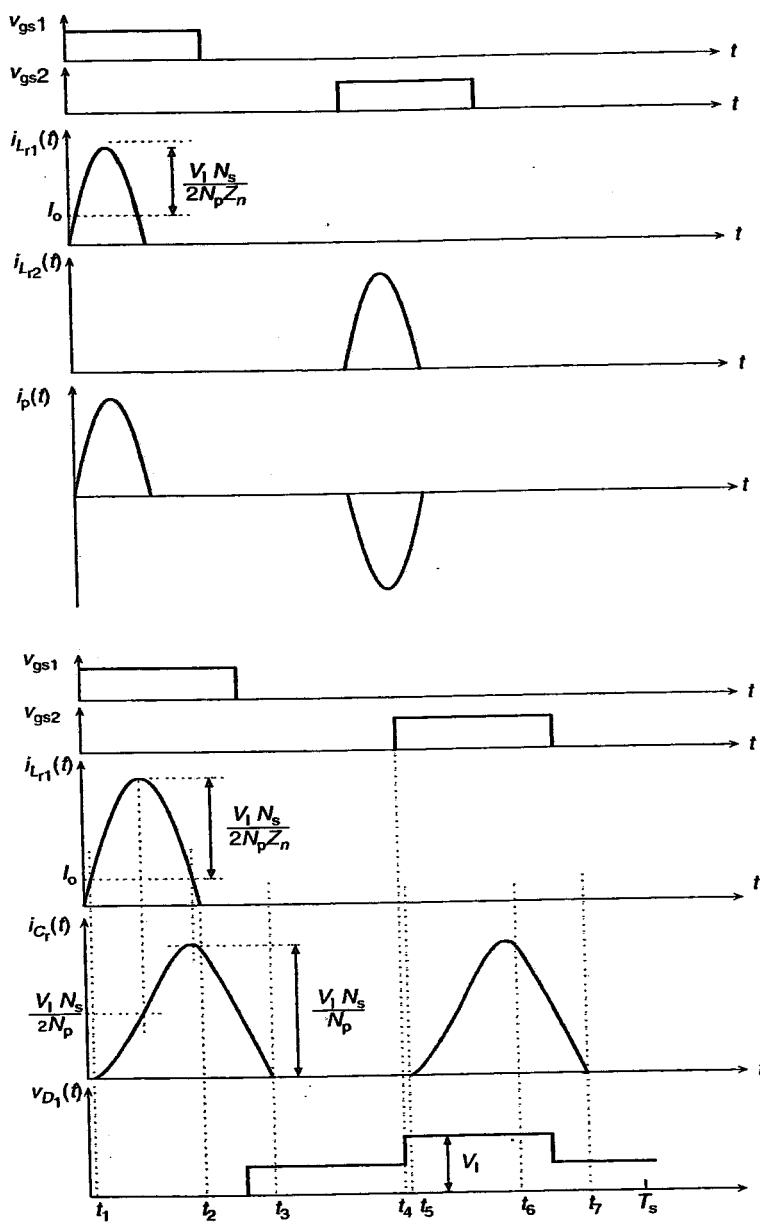

Figure 4.18 Switching waveforms for the ZCS, half-wave, quasi-resonant, hal bridge converter [2].

The voltage conversion ratio for maximum load (i.e., $I_o Z_n = (V_i N_s/2N_p)$) is

$$\frac{V_a}{V_i} = \left(\frac{N_s}{N_p}\right)\left(\frac{f_s}{f_n}\right). \tag{4.52}$$

Figure 4.19 shows the straight-line characteristics of the voltage conversion ratios for several x values [2], where $x = 2I_oZ_nN_p/V_iN_s$.

Example 4.3. The ZCS, half-wave, quasi-resonant half-bridge resonant converter shown in Figure 4.13 has an input voltage, V_i, of 50 V and a steady-state output current, I_o, of 5 A. The capacitance for the resonant capacitor is 10 μF. The turn-ratio of the transformer is 2, with a leakage inductance, L_r, of 10 μH. Determine (a) the peak amplitude of the resonant inductor current, (b) the peak value of the resonant capacitor voltage, and (c) the duration of the resonant mode.

Solution.

(a) From Equation (4.43), the peak value of the resonant inductor current is

$$I_{L_r} = I_o + \frac{V_iN_s}{2N_pZ_n} = 55\text{A}.$$

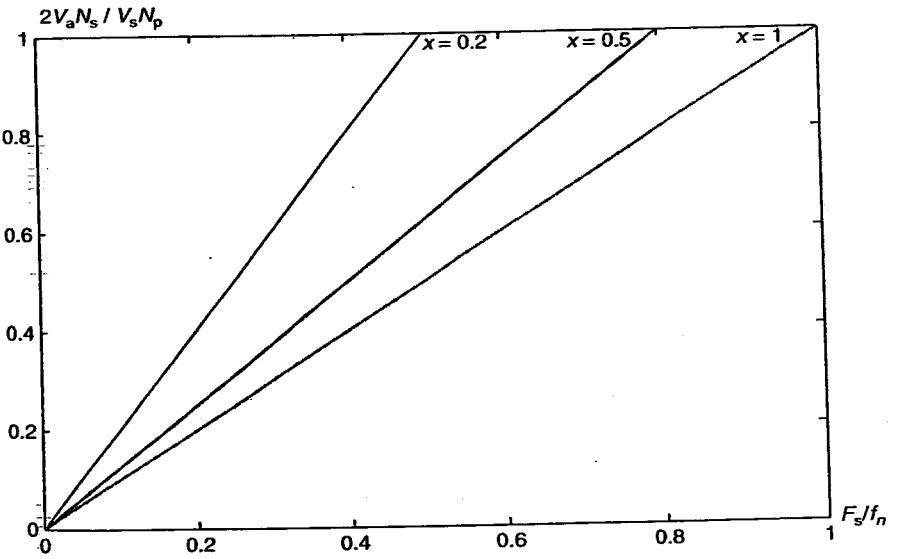

Figure 4.19 Voltage conversion versus f_s/f_n of the ZCS, quasi-resonant half-bridge converter for several normalized output current values [2].

(b) From Equation (4.44), the peak resonant capacitor voltage is

$$V_{C_r} = \frac{V_i N_s}{2N_p} = \frac{(50)(2)}{2} \leq 50\,\text{V}.$$

(c) For a half-wave mode, α takes on values between π and $3\pi/2$. Thus,

$$\sin^{-1}(-0.1) = \pi + 0.1 = 3.1416 + 0.1 \leq 3.2416.$$

From Equation (4.47), the duration of the resonant mode is

$$T_2 = \sin^{-1}\left(\frac{-2I_o Z_n N_p}{V_i N_s}\right)\sqrt{L_r C_r} = 32.4\,\mu\text{s}.$$

PROBLEMS

4.1. The forward converter shown in Figure 4.1 has an input voltage of 50 V and a switching frequency of 1 kHz. The average output voltage is 25 V with a maximum duty cycle of 0.6. The number of turns of the primary winding is 100. Determine (a) the number of turns of the reset winding, (b) the number of turns of the secondary winding, and (c) the duration, t_r, when the secondary current is flowing.

4.2. The discontinuous-mode flyback converter shown in Figure 4.10 has an input voltage of 50 V. The magnetizing inductance of the primary winding is 500 μH with a turns ratio, N_s/N_p, of 4. The switching frequency is 1 kHz with a duty cycle of 20%. Determine (a) the peak value of the primary current, (b) the duration of the secondary current t_r, and (c) the average output voltage.

4.3. The ZCS, half-wave, quasi-resonant half-bridge resonant converter shown in Figure 4.13 has an input voltage of 40 V and a steady-state output current of 5 A. The capacitance for the resonant capacitor is 1 μF. The turn-ratio for the transformer is 2, with a leakage inductance of 10 μH. Determine (a) the peak amplitude of the resonant inductor current, (b) the duration of the resonant mode, and (c) the switching frequency required for the maximum load.

4.4. Derive the expressions for the duty cycle, output voltage, and average input current for a flyback converter operating in the discontinuous mode.

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5

Control Schemes of Switching Converters

5.1 INTRODUCTION

The figure-of-merits in switching converters are the load and line regulations. *Load regulation* is defined as the change in the output voltage corresponding to a 1-mA change in the load current while *line regulation* is defined as the change in the output voltage corresponding to a 1-V change in the input voltage. The load and line regulations of the switching converters depend largely on their control schemes. By varying the on time of the switching transistor in a switching converter, the output voltage can be maintained at a constant during load variations and supply-voltage variations. Pulse-width modulation (PWM) is the most common control scheme for switching converters. The abundance of commercially available PWM integrated-circuit controllers has contributed to making the switching converters a popular choice in many system applications. On the other hand, the resonant switching converters require a variable-frequency controller or frequency modulator to achieve the desired energy conversion. The implementation of the variable-frequency controller is more involved than the

pulse-width-modulated-controller. This chapter presents the most common control techniques for DC–DC switching converters and a description of some commercial controller circuits.

5.2 PULSE-WIDTH MODULATION

The technique of modulating the duration of the ON or OFF pulses, or both, that are applied to the switching transistor is called pulse-width modulation (PWM). The purpose of the PWM is to vary the duty cycle d according to

$$d = t_{on} f_s = \frac{t_{on}}{t_{on} + t_{off}}. \tag{5.1}$$

Thus, modulating either t_{on} or t_{off} or both can vary d. There are two schemes of PWM: the fixed-frequency PWM and the variable-frequency PWM. The variable-frequency PWM can be achieved by: (a) keeping t_{on} fixed and varying t_{off}, (b) keeping t_{off} fixed and varying t_{on}, and (c) changing both t_{on} and t_{off} as shown in Figure 5.1(a)–(c), respectively. The major problem associated with the variable-frequency PWM is the unpredictable electromagnetic interference (EMI) due to the varying switching frequencies. The fixed-frequency PWM is achieved by changing both the t_{on} and t_{off} durations while maintaining a constant switching period, as shown in Figure 5.2. This PWM scheme is the most popular due to its ease of implementation by commercially available integrated-circuit controllers and because its EMI can be filtered without difficulty.

There are two PWM modes of operation depending on the control signals required. The voltage-mode PWM derives its control signal from the output voltage of the switching converter, whereas the current-mode or current-injected PWM utilizes both the output voltage information as well as the information from the inductor current in the switching converter to determine the desired duty cycle applied to the switching transistor.

5.2.1 Voltage-Mode PWM Scheme

The schematic of a fixed-frequency voltage-mode PWM controller is shown in Figure 5.3(a). The error amplifier compares the sampled output voltage V_{sp} with a fixed reference voltage V_{ref} and generates an error voltage V_e given by:

$$V_e = V_{ref} - \frac{Z_2}{Z_1}\left(V_a \frac{R_a}{R_1 + R_2} - V_{ref}\right). \tag{5.2}$$

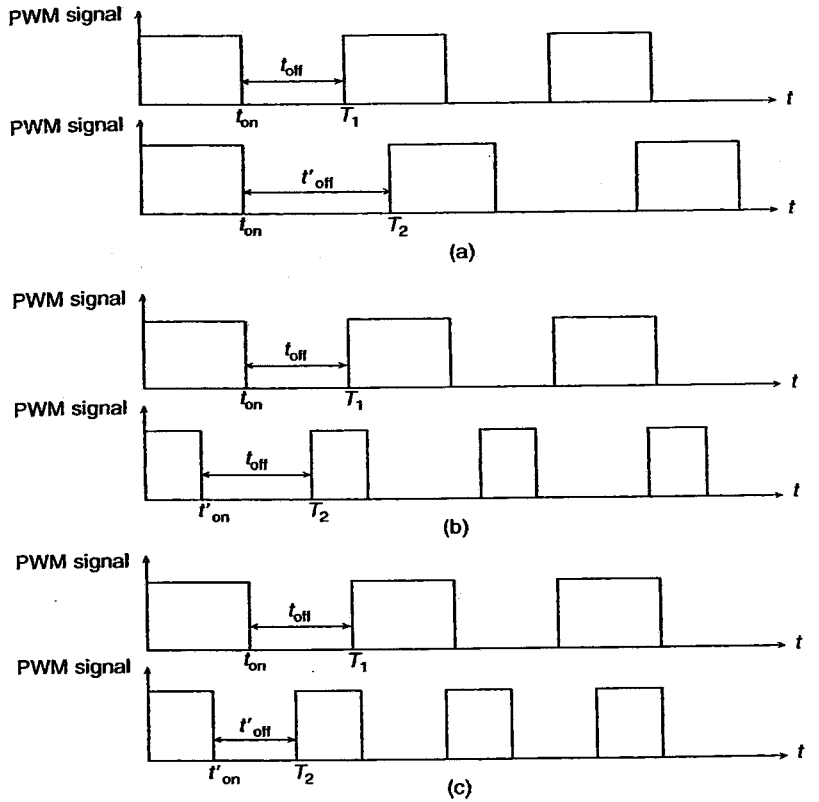


Figure 5.1 Variable-frequency PWM schemes: (a) fixed t_{on}, variable t_{off}; (b) variable t_{on}, fixed t_{off}; and (c) variable t_{on}, variable t_{off}.

This error voltage is then fed to the noninverting input of a comparator that compares the error voltage with a sawtooth signal at its inverting input. The charging and discharging of a capacitor C_c via a switching transistor Q_{st} driven by a fixed-rate clock pulse generates this positive-going sawtooth signal. The frequency of this fixed-rate clock pulse determines the switching frequency of the converter. To achieve a linear positive-going slope, it is assumed that the time constant R_cC_c is much larger than the switching period. The clock pulse should be short, but sufficient to discharge the capacitor C_c through the switching transistor Q_{st}. Due to the large gain of the comparator, its output will swing close to its positive supply rail whenever the noninverting signal is higher than the inverting signal. The output of

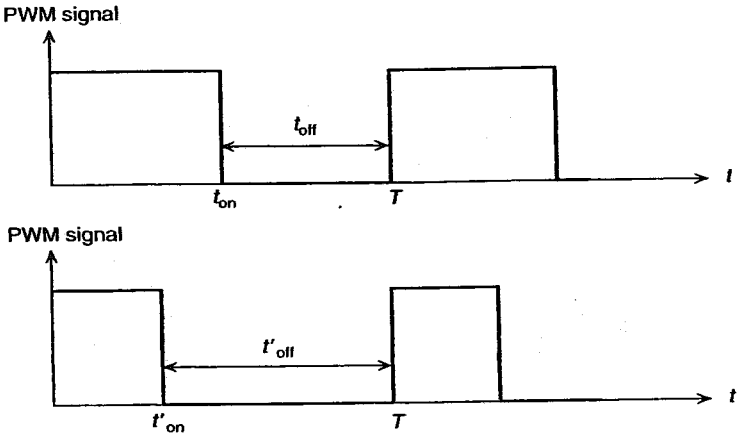


Figure 5.2 Fixed-frequency PWM scheme.

the comparator is a PWM signal shown in Figure 5.3(b). The output is high whenever the error voltage is higher than the sawtooth signal. This PWM signal is then fed to a gate-drive circuitry that drives the switching transistor Q_s of the buck converter. The duty cycle is determined by the time between the reset of the sawtooth generator as the switching transistor Q_{st} switches on, and the intersection of the error voltage with the positive-going sawtooth signal. Consequently, the instantaneous duty cycle d can be approximated by:

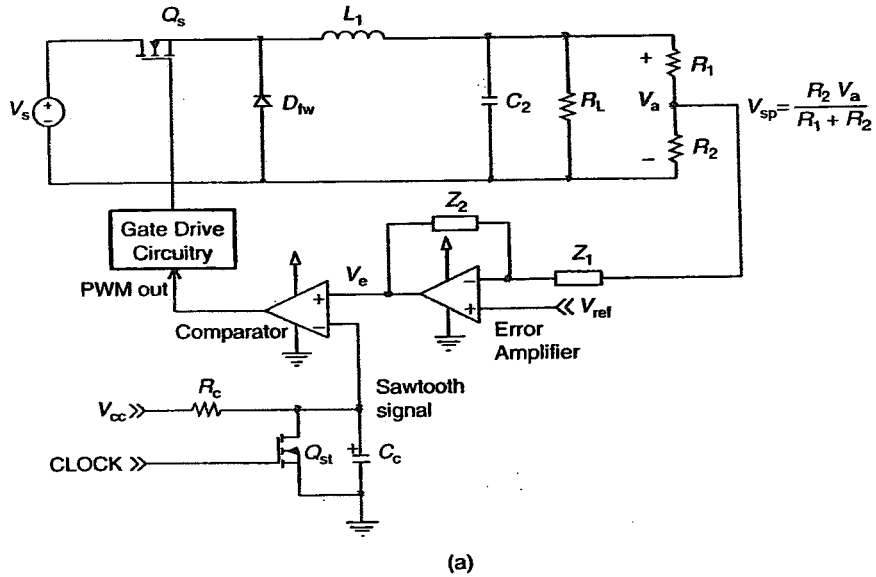
$$d = \frac{v_e}{V_p}, \tag{5.3}$$

where V_p is the maximum amplitude of the sawtooth signal. A lower-than-desired output voltage produces a higher error voltage. This produces a longer on pulse, which, in turn, switches the switching transistor Q_{st} for a longer duration and results in an increased output voltage. The feedback network, Z_1 and Z_2, of the error amplifier helps to stabilize and shape the frequency response of the switching converter (see Chapter 6).

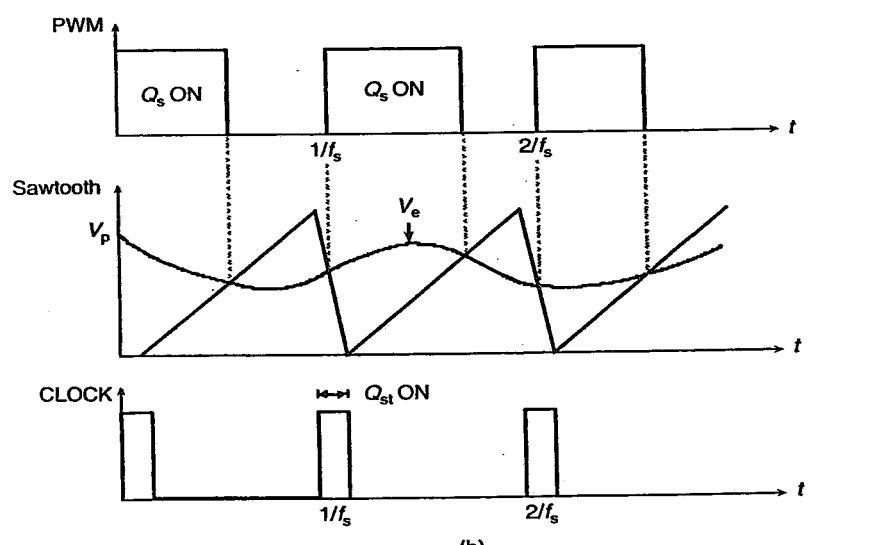
The average output voltage, V_a, of a buck converter in a closed loop configuration employing the PWM control scheme is given by

$$V_a = dV_s = (D + \hat{d})V_s = DV_s + \hat{d}V_s. \tag{5.4}$$

The average output voltage, V_a, therefore contains a steady-state value DV_s and a modulated value $\hat{d}V_s$. The modulated duty cycle, $\hat{d}$, compensates the



(a)



(b)

Figure 5.3 (a) A fixed-frequency PWM controller for a buck converter. (b) Switching waveforms for the fixed-frequency PWM controller.

output voltage for either load or input voltage variations. The value of $\hat{d}$ will be positive when the instantaneous output voltage is less than the desired output voltage, and negative when the instantaneous output voltage is higher than the desired output voltage. The DC open-loop gain is

$$GH(\omega_o) = \frac{dV_s}{V_a'} = \frac{V_c V_s}{V_a' V_p} = \frac{KV_s}{V_p}, \tag{5.5}$$

where $K = (V_c/V_a')$, and V_a' is the open-loop input voltage to the error amplifier and K is the DC gain of the error amplifier.

The PWM controller can be implemented using either a combination of discrete components and integrated circuits or just integrated circuits. An implementation of a voltage-mode PWM controller using a combination of discrete components and integrated circuits is shown in Figure 5.4. The NE555 timer in its astable mode generates an asymmetric square-wave output at a fixed frequency. The capacitor C_1 differentiates this square wave into a sawtooth waveform with its slope determined by the time constant R_1C_1 at the base of Q_1, assuming that the phototransistor is not conducting. The resistor R_2 and the phototransistor in the optoisolator modulate the sawtooth waveform by changing its time constant from R_1C_1 to $R'C_1$, thereby changing the slope of the sawtooth waveform. R' is the parallel combination of R_1, R_2 and the phototransistor. The normally conductive transistor, Q_1, is switched off when the negative-going sawtooth signal is above an emitter-base drop compared to its emitter voltage. The inverter Q_2 inverts the negative-going pulse at the collector of Q_1. This produces a positive-going pulse at its collector. This positive-going pulse switches on Q_3, the upper transistor of the output totem-pole, which in turn switches on the switching transistor Q_5 of the boost converter. The output voltage of the boost converter is regulated by comparing its sampled output voltage with a fixed reference voltage, V_{ref}. The increase in the output voltage, due to either line (i.e., input voltage) or load variations, is detected by the error amplifier that drives the photodiode of the optocoupler, Q_{op}, by modulating its light intensity. Consequently, the negative-going pulse at the base of Q_1 attains a larger negative slope since the effective time constant $R'C_1$ is smaller, causing Q_1, Q_2, and Q_4 to be switched on for a longer duration, while transistors Q_3 and Q_5 are switched on for a shorter duration. Therefore, the output voltage decreases. Thus, the pulse width applied to the switching transistor Q_5 is modulated according to load and line variations, stabilizing the output voltage of the boost converter.

The schematic of an integrated circuit PWM controller is shown in Figure 5.5(a). The error amplifier compares the sampled feedback voltage from the output of a switching converter with a fixed reference voltage, V_{ref}.

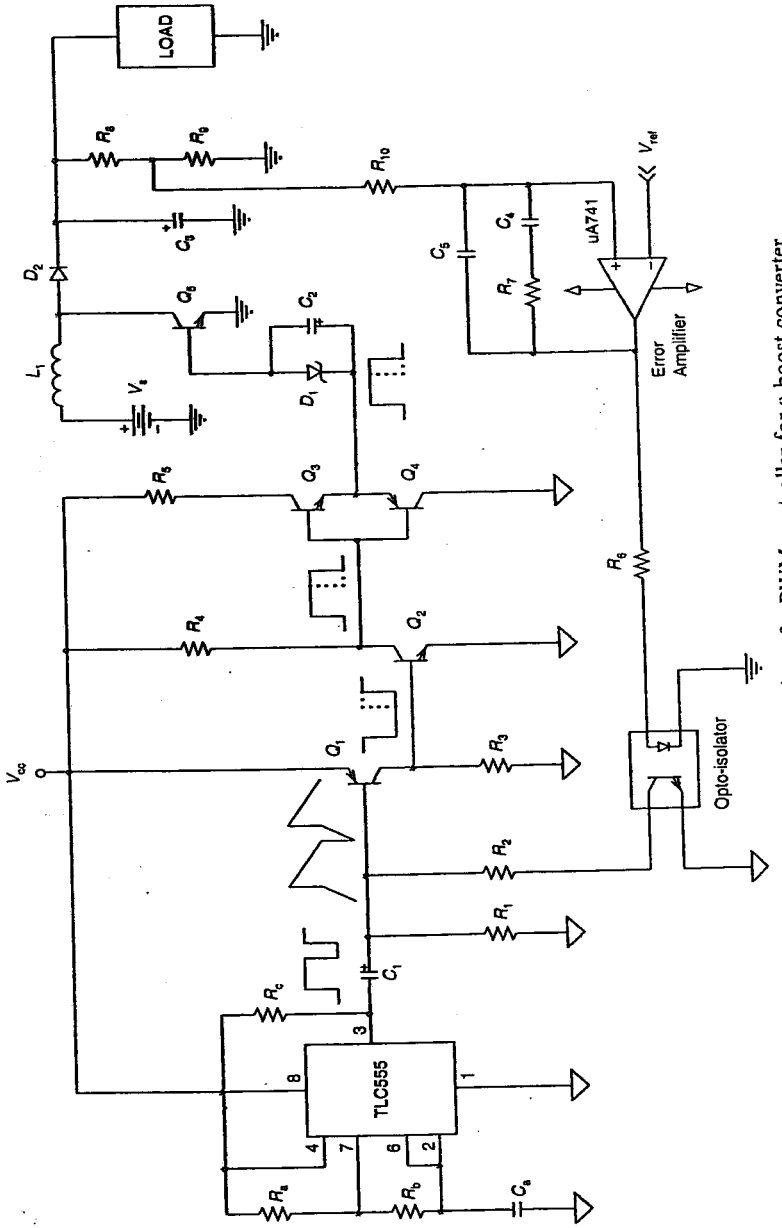
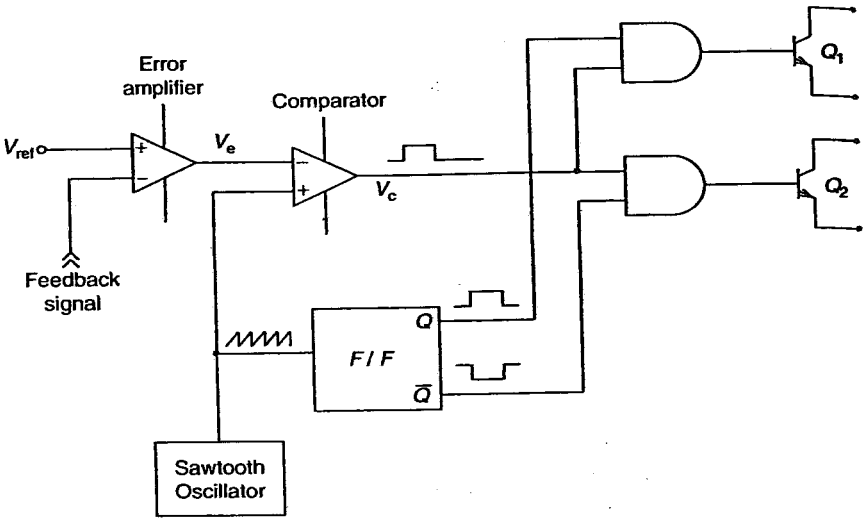
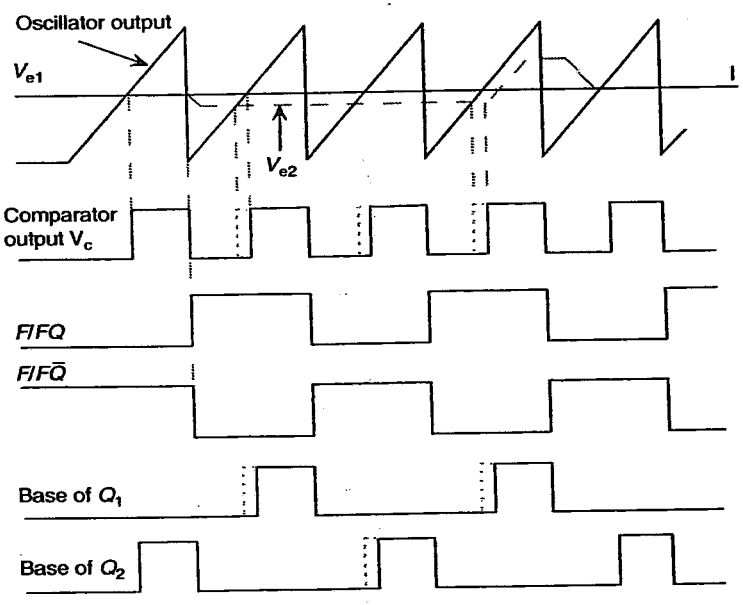


Figure 5.4 A discrete–integrated-circuit implementation of a PWM controller for a boost converter.



(a)



(b)

Figure 5.5 (a) An integrated-circuit PWM controller. (b) Switching waveforms of the integrated-circuit PWM controller.

The error signal is amplified and fed into the inverting input of a comparator. The noninverting input of the comparator accepts a linear-slope sawtooth signal generated by a fixed frequency sawtooth oscillator. The output from the sawtooth oscillator is also used to toggle a trailing-edge-triggered flip-flop that produces square wave outputs Q and $\bar{Q}$. The output of the comparator is high only whenever the sawtooth signal is higher than the error signal. The comparator PWM signal output is used to drive the AND gates, enabling each output only when both inputs to the gate are "high." The result is a variable duty cycle pulse train at the bases of the two uncommitted collector–emitter switching transistors Q_1 and Q_2. The switching waveforms for the integrated PWM controller are shown in Figure 5.5(b).

5.2.2 Current-Mode PWM Scheme

In the current-mode or current-injected PWM scheme, the duty cycle of the switching converter is determined by the time at which the inductor current reaches a threshold value determined by the reference control signal. The current-mode PWM scheme has several advantages over the conventional voltage-mode PWM scheme [1,2]. First, since the switching transistor is switched off when the inductor current reaches the control signal level, failure due to excessive switch current can be prevented by simply limiting the maximum value of the control signal. Second, several switching converters can be operated in parallel without a load-sharing problem because all the switching converters receive the same PWM control signal from the feedback circuit and they carry the same current. During current-mode conversion, the average inductor current follows a reference voltage. As such, the inductor acts as a current source (CS). Thus, the output filter behaves as a voltage-controlled current source that supplies the output capacitor and the load, thereby reducing the order of the system by one. This simplifies its feedback compensation considerably.

The major drawback of the current-mode PWM scheme is its instability. An oscillation generally occurs whenever the duty cycle exceeds 50%, regardless of the type of switching converter. However, this instability can be eliminated by the addition of a cyclic artificial ramp either to the sample of the inductor current or to the voltage control signal [3]. Discrete modeling can also be used to stabilize the loop [4].

Figure 5.6(a) shows a fixed-frequency current-mode PWM boost converter. It contains two feedback loops, an outer one which senses the output voltage and delivers a control signal to an inner loop which senses the current flowing through the switching transistor and keeps the output voltage constant on a pulse-by-pulse basis. For a given cycle of operation, the

turn-on of the switching transistor is coincident with the clock pulse and the turn-off is coincident with the time that the analog voltage of the switch current (coincident with the inductor current) intercepts the error voltage as shown in Figure 5.6(b).

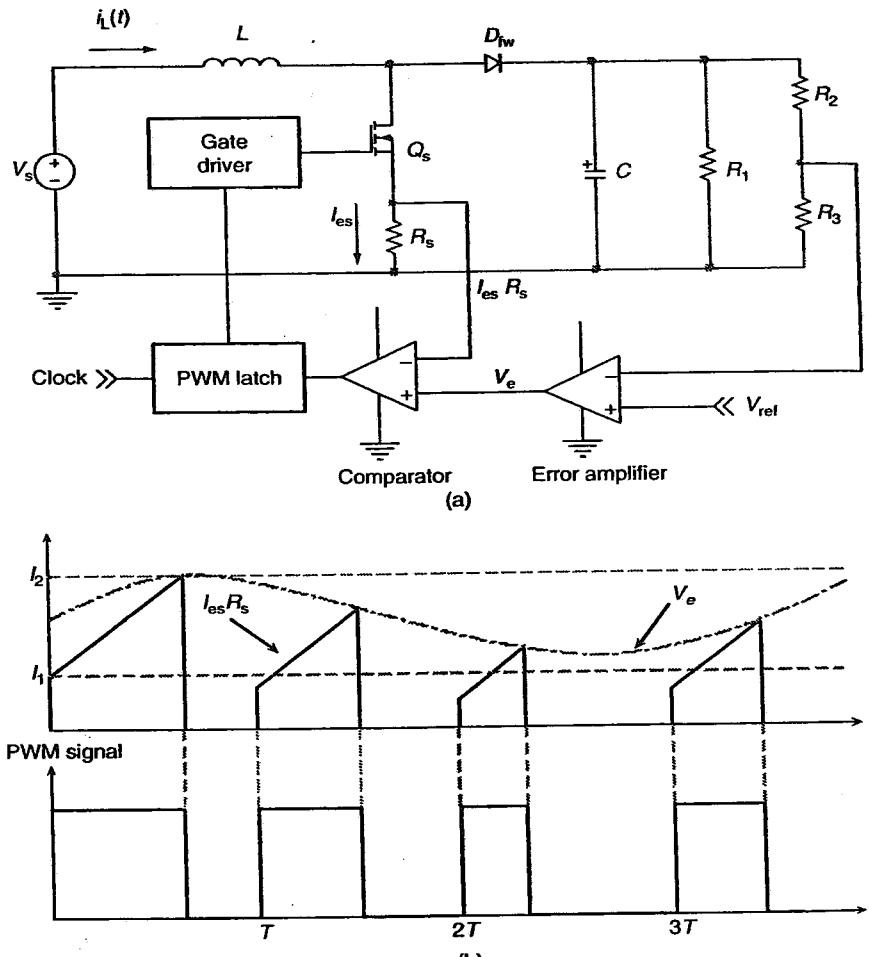


Figure 5.6 (a) A boost converter implemented with a fixed-frequency current-mode PWM controller. (b) Fixed-frequency current-mode PWM controller waveforms.

5.2.2.1 *Instability for D > 50%*

When the duty cycle is greater than 50%, the inductor current shows subharmonic oscillations corresponding to the proportional current-mode control [5]. Figure 5.7 depicts the inductor current waveform, I_L, of a current-mode converter being controlled by an error voltage V_e. As can be seen in Figure 5.7, the instability can be initiated when the system is excited with small perturbations in the inductor current. Assume that the inductor current is perturbed by an amount ΔI_o at the beginning of the switching period, it can be seen that if the duty cycle is greater than 50%, then the perturbation ΔI_1 for the following period is greater. This trend keeps evolving, producing the above-mentioned instability. If the duty cycle is smaller than 50%, the perturbation is

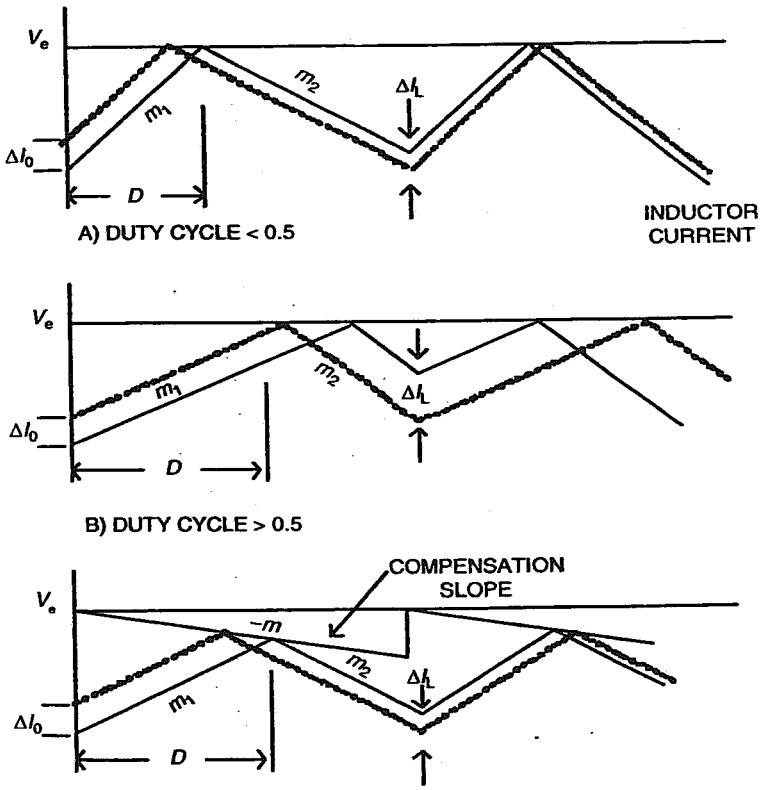


Figure 5.7 Current-mode control instability.

attenuated in the successive periods until it disappears. In this case, the system is stable. Mathematically this can be stated as

$$\Delta I_1 = -\Delta I_o\left(\frac{m_2}{m_1}\right). \tag{5.6}$$

5.2.2.2 Compensation with External Ramp

By introducing a linear ramp of slope $-m$, as shown in Figure 5.7(c), the instability can be compensated. Note that this slope may either be added to the current waveform, or subtracted from the error voltage. The compensating slope can be introduced in Equation (5.6) giving:

$$\Delta I_1 = -\Delta I_o\left(\frac{m_2 + m}{m_1 + m}\right). \tag{5.7}$$

If

$$m > -\frac{1}{2}m_2 \tag{5.8}$$

then $\Delta I_1 < \Delta I_o$, and the effect of the perturbation vanishes.

Therefore, to guarantee the stability of the current loop, the slope of the compensation ramp must be greater than one-half of the down slope of the current waveform. For the buck converter of Figure 5.8, m_2 is a constant equal to $(V_o/L)\,R_s$. The magnitude of the compensating waveform, A, should be chosen such that

$$A > TR_s\frac{V_o}{L} \tag{5.9}$$

to ensure its stability above a 50% duty cycle. It has been shown in Ref. [5], and is easily verified from Equation (5.7), that by choosing the slope compensation m equals $-m_2$, a critically damped transient response is obtained. This allows the current to stabilize in exactly one cycle as illustrated in Figure 5.9. If an external voltage control loop is added, then it has also to be compensated to achieve the desired transient response.

5.3 HYSTERESIS CONTROL: SWITCHING CURRENT SOURCE

In this control strategy, the main switch is switched on when the inductor current goes below a certain value, and it is switched off when the inductor

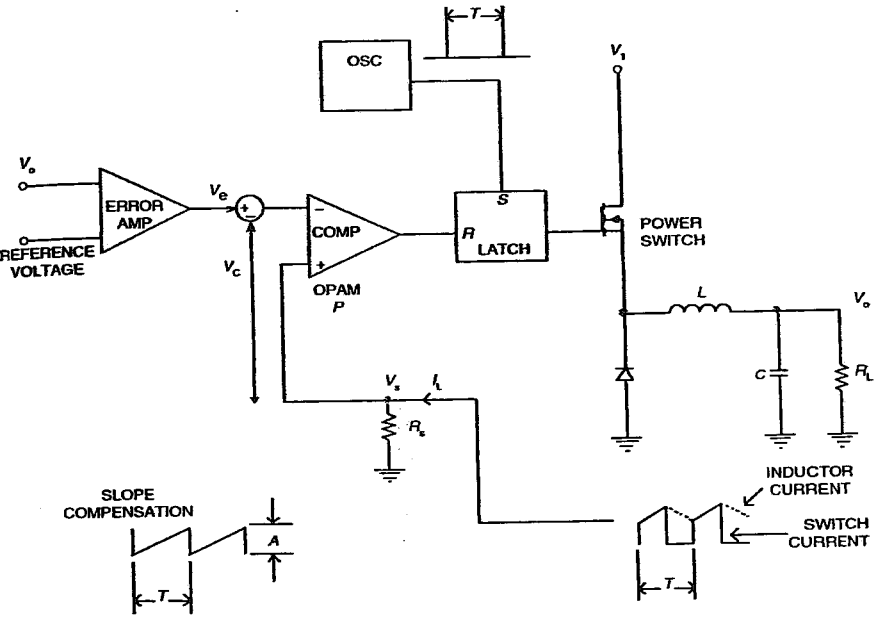


Figure 5.8 A current-mode controlled buck regulator with slope compensation.

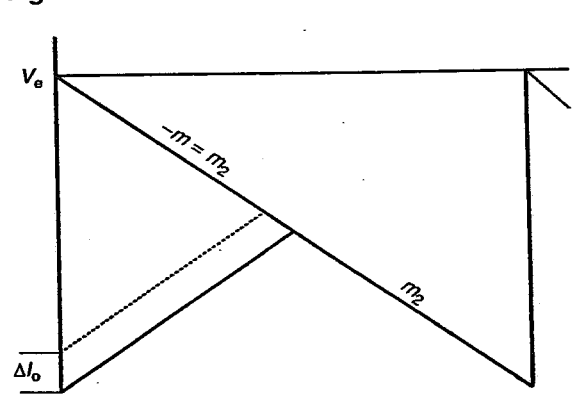


Figure 5.9 Slope compensation m equals $-m_2$.

current goes above a specified maximum value. Thus, the amplitude of the current becomes bounded between these two limits. Hysteresis control finds its main application in power inverters, motor drives, and power factor correction circuits; nevertheless, it can be used to control a switching current source.

The natural way to implement a regulated switching current source is to sample its output current and compare this value with a reference signal to close the regulator loop. A switching current source should have large output impedance. When the feedback loop is closed, this output impedance will become even larger. A switching current source usually has an inductor at its output. A basic switching current source using a hysteresis control is shown in Figure 5.10.

Figure 5.11 shows the output current of the current source using a hysteresis control. The desired DC current value is represented by $IM = 1$ A; while the maximum and minimum current values are *IPN* and *IVN*, respectively. A load transition occurs at $t = 5$ msec. Notice that the frequency of the current waveform changes at the load transition, while their maximum

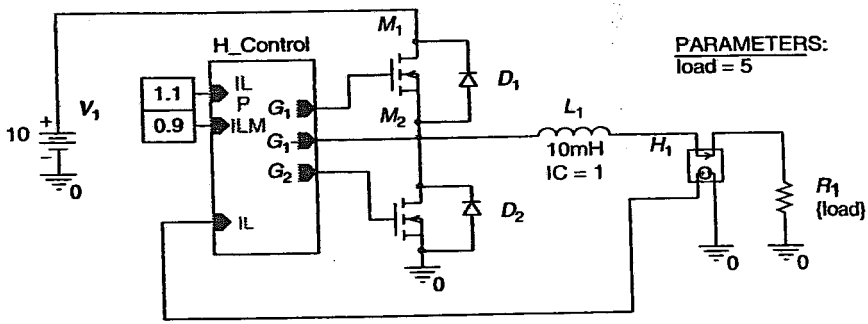


Figure 5.10 Switching current source with hysteresis control.

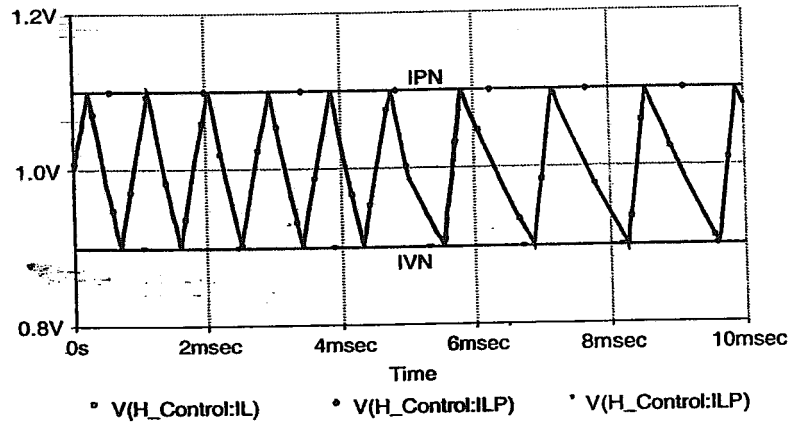


Figure 5.11 Hysteresis control waveforms.

and minimum values remain unchanged. The width of the hysteresis band sets the maximum operating frequency; therefore, the narrower the band, the higher the switching frequency. By an appropriate choice of the hysteresis band, the current ripple can be made triangular. If the band is too wide, the current ripple follows the exponential charge–discharge law of an LR circuit. The main disadvantage of the hysteresis control is the variable switching frequency, which makes EMI a more challenging problem to deal with.

5.3.1 Steady-State Analysis During t_{on}

Figure 5.12 displays the equivalent circuit of the switching current source during t_{on}.

The voltage across the inductor is

$$v_L = L\frac{di}{dt} = L\frac{\Delta i}{\Delta t} = L\frac{\Delta i}{t_{on}} = V_c - V_o. \tag{5.10}$$

Then,

$$t_{on} = L\frac{\Delta i}{V_c - V_o}. \tag{5.11}$$

For a small hysteresis band, the output current can be considered constant, then

$$V_o = I_o R, \tag{5.12}$$

and

$$t_{on} = L\frac{\Delta i}{V_c - I_o R}. \tag{5.13}$$

During t_{off}, the left end of the inductor is grounded and the energy stored in the inductor keeps the current flowing in the same direction, as shown in Figure 5.13,

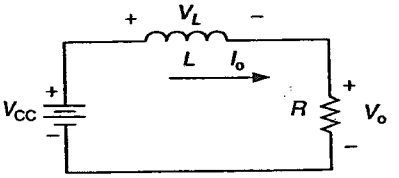


Figure 5.12 Equivalent circuit during t_{on}

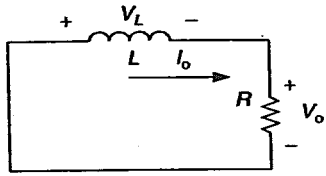


Figure 5.13 Equivalent circuit during t_{off}.

V_L is given by

$$V_L = L\frac{di}{dt} = L\frac{-\Delta i}{\Delta t} = L\frac{-\Delta i}{t_{off}} = -V_o. \tag{5.14}$$

Then, t_{off} becomes

$$t_{off} = L\frac{\Delta i}{V_o} = L\frac{\Delta i}{I_o R}, \tag{5.15}$$

since

$$T = t_{on} + t_{off}, \tag{5.16}$$

then

$$T = L\Delta i\left(\frac{1}{V_{cc} - I_o R} + \frac{1}{I_o R}\right). \tag{5.17}$$

The switching period versus the load resistance is shown in Figure 5.14. When the load changes, its switching frequency automatically adjusts to maintain the output current within the bounds.

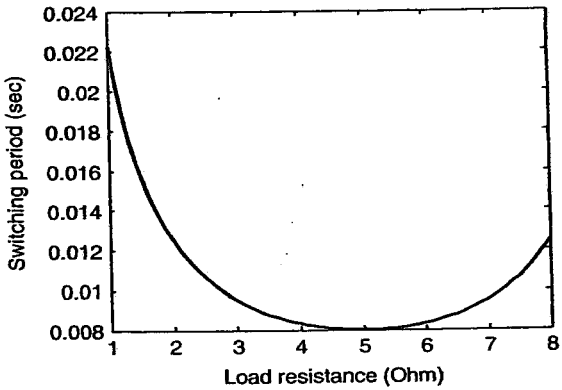


Figure 5.14 Switching period versus load resistance.

5.4 COMMERCIAL INTEGRATED CIRCUIT CONTROLLERS

5.4.1 Fixed-Frequency Voltage-Mode SG3524 Controller [6]

The SG3524, originally introduced by Silicon General Corporation, is the first commercially available fixed-frequency voltage-mode integrated circuit PWM control chip. A functional block diagram of the SG3524 is shown in Figure 5.15. A programmable sawtooth oscillator generates a 3.5-V sawtooth waveform V_{st} with a base DC voltage of about 0.5 V. The period of the sawtooth waveform $T = R_t C_t/(1.15)$ is set by external timing-resistor R_t and timing-capacitor C_t at pins 6 and 7, respectively. The timing-resistor R_t establishes a constant charging current for C_t that result in a linear voltage ramp at pin 7, which is fed to the voltage comparator. An error amplifier compares the sampled output voltage (pin 1) with a fixed reference voltage V_{ref} (pin 2) and produces an error voltage V_e at pin 9. The high impedance at the output of the error amplifier (pin 9) presents some difficulties in the use of the conventional feedback compensation scheme for this error amplifier. A current-limit comparator compares the voltage proportional to the output current to a fixed reference voltage of 200 mV.

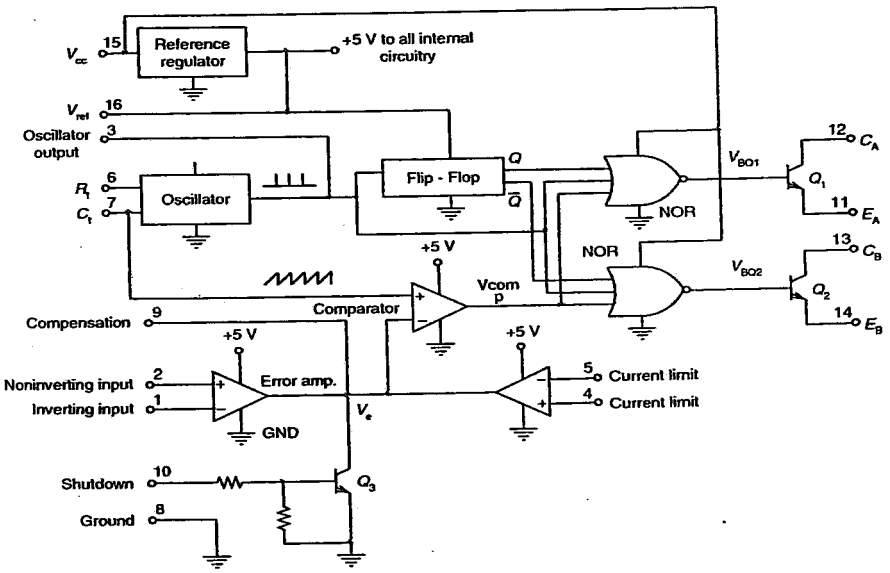


Figure 5.15 Functional block diagram of the SG3524 PWM controller. ([6], Reprinted by permission of Texas Instruments.)

Its purpose is to shut down the output transistors should an overcurrent situation arises, when the sample of the output current is higher than 200 mV. The output of the error amplifier is compared to the sawtooth V_{st} in a voltage comparator. Since the sawtooth V_{st} is fed to the noninverting input and the error voltage V_e is fed to the inverting input, the comparator output is high only whenever the sawtooth signal voltage is higher than the error signal, as shown in Figure 5.16. Thus, the comparator output is a pulse

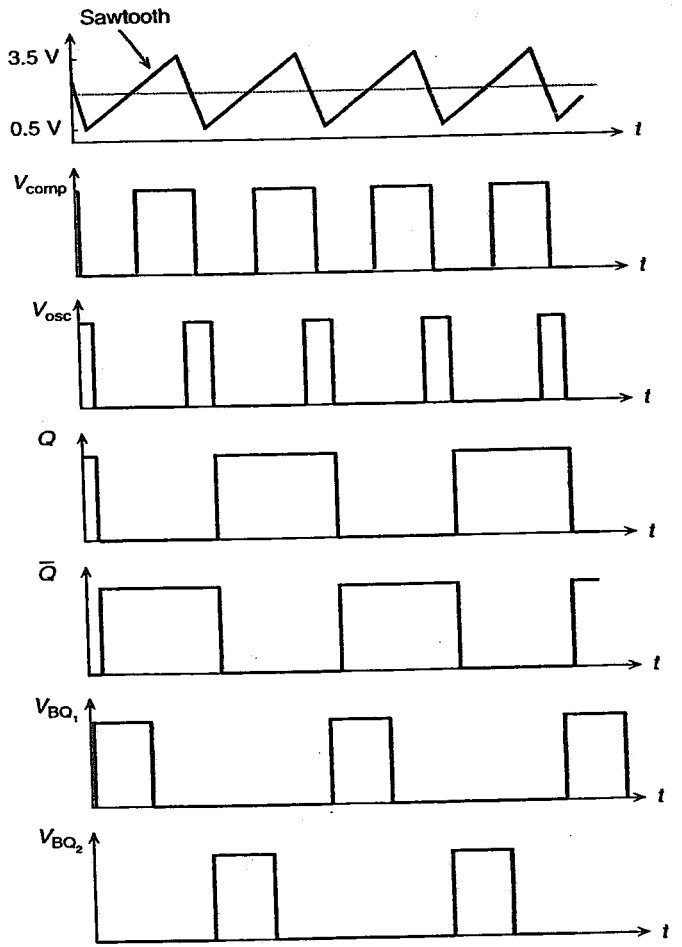


Figure 5.16 Switching waveforms of the SG3524 controller.

with a width corresponding to the time while the sawtooth voltage is higher than the error voltage. The resulting trailing-edge modulated pulse is then steered to the appropriate output transistor by the pulse-steering flip-flop, which is synchronously toggled by the oscillator output. The oscillator output pulse also serves as a blanking pulse to assure that both the output transistors are never switched on simultaneously during the transition times, otherwise a catastrophic "shoot through," resulting in overcurrent damage to the transistors may occur.

The SG3524 is designed for push–pull switching converters which have a switching frequency half that of the oscillator. The output transistors may also be connected in parallel for single-ended switching converters in which the switching frequency is the same as the oscillator frequency.

Example 5.1. Design a pulse-width modulator using the SG3524 for a buck converter with an input voltage of 10 V and an average output voltage of 5 V. The switching frequency is 1 kHz. The values for the output inductor and filter capacitor are 45 mH and 62.5 μF, respectively.

Solution. The switching frequency of the SG3524 is given as

$$f_s = \frac{1.15}{R_t C_t} = 1\,\text{kHz}.$$

Hence, if a C_t of 0.1 μF is chosen, then

$$R_t = \frac{1.15}{f_s C_t} = 11.5\,\text{k}\Omega.$$

The required steady-state duty cycle is 50%. Since the sawtooth signal of the SG3524 increases from 0.7 to 3.5 V, the required error voltage is

$$\frac{(V_e - V_m)}{(V_p - V_m)} = D,$$

or

$$V_e = 1.4 + V_m = 2.1\,\text{V}.$$

From operational amplifier theory,

$$V_e = V_{ref} - \frac{R_2}{R_1}(V_{sp} - V_{ref}).$$

Assuming a reference voltage of 2.5 V and unity gain with $R_1 = R_2 = 100\,\text{k}\Omega$, the sampling voltage, V_{sp}, is

$$V_{sp} = \frac{R_2}{R_1}(V_{ref} - V_e) + V_{ref} = \frac{100K}{100K}(2.5 - 2.1) + 2.5 = 2.9\,\text{V}.$$

The sampling network can now be designed. Using the voltage divider rule,

$$V_{sp} = \frac{R_{s2}}{R_{s1} + R_{s2}} V_a,$$

or

$$5R_{s2} = 2.9(R_{s1} + R_{s2}).$$

If R_{s1} is chosen to be 1 kΩ, then R_{s2} is equal to 1.38 kΩ. Figure 5.17 shows the SG3524 PWM for the buck converter.

5.4.2 Variable-Frequency Voltage-Mode TL497 Controller [7]

The Texas Instruments' TL497 is a fixed on time variable-frequency voltage-mode PWM controller. Its functional block diagram is shown in Figure 5.18. The on time of this controller is determined by an external capacitor C_t

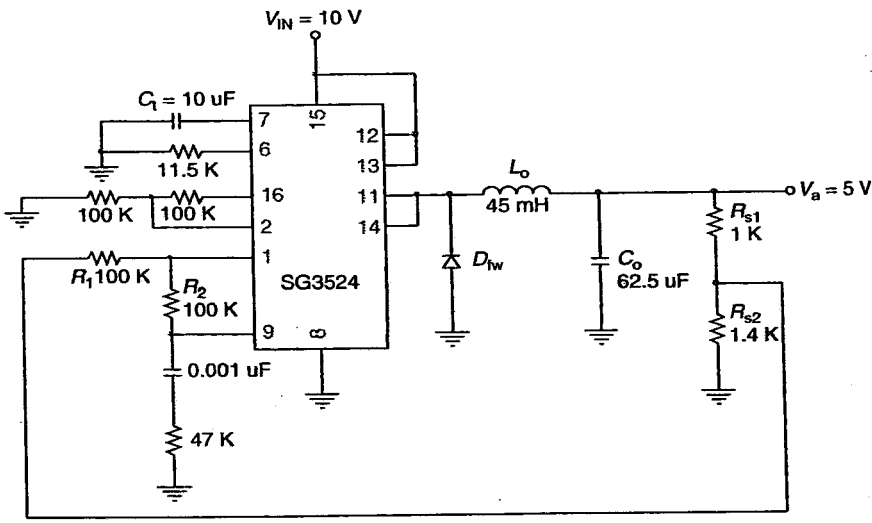


Figure 5.17 Circuit schematic of the SG3524 PWM in Example 5.1.

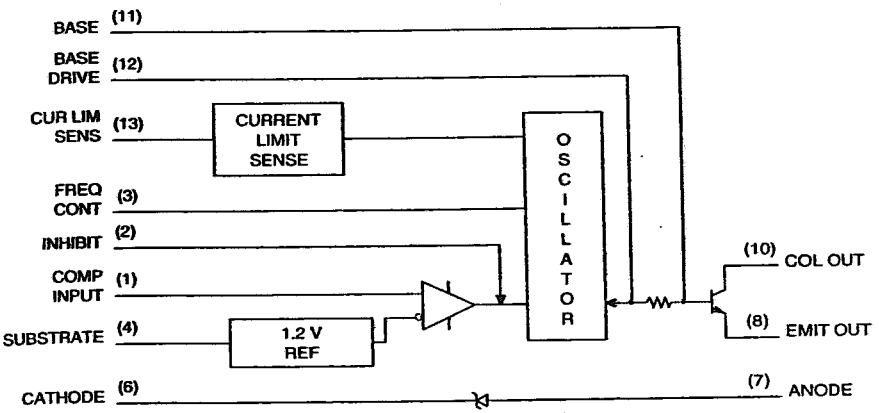


Figure 5.18 Functional block diagram of the TL497 controller. ([7], Reprinted by permission of Texas Instruments.)

connected between the frequency-control pin 3 and ground. The timing-capacitor is charged by an on-chip constant-current source to a predetermined threshold. The on time varies from 19 μs for a C_t of 200 pF to 180 μs for a C_t of 2000 pF. A comparator compares the feedback voltage at pin 1 with the internal fixed reference voltage of 1.2 V. The oscillator is enabled only when the feedback voltage is below 1.2 V. The uncommitted collector–emitter output transistor is switched on during the charging of the timing capacitor as shown in Figure 5.19. The oscillator is disabled whenever the feedback voltage is higher than 1.2 V. Thus, the off time and the switching frequency are varied according to the duration of the feedback voltage above 1.2 V. A programmable current-limit circuit protects the output transistor against excessive peak current. It is activated when 0.7 V is developed across the sense resistor connected between pin 13 and the supply voltage. An inhibit input (pin 2) is available for external gating. The controller is switched off when the inhibit input is high.

5.4.3 Fixed-Frequency Current-Mode UC3842 PWM Controller [8,9]

The Unitrode's UC3842 is the first commercially available fixed-frequency current-mode PWM controller. Figure 5.20 shows the functional block diagram of the UC3842. The feedback voltage V_{fb} (pin 2) is compared with an internal fixed reference voltage of 2.5 V in an error amplifier. The output of the error amplifier (pin 1) is available for external frequency

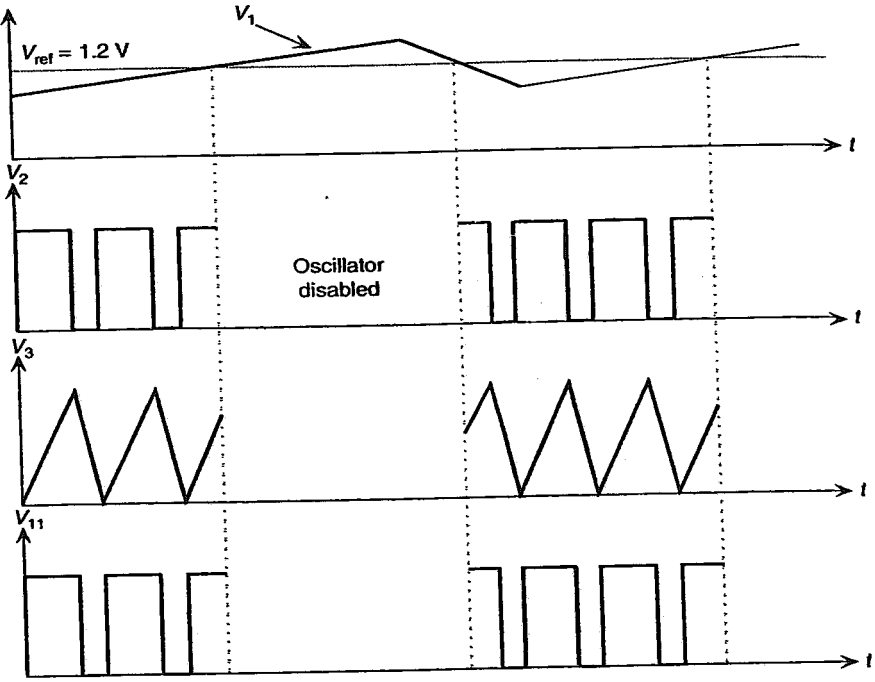


Figure 5.19 Switching waveforms of the TL497 controller.

compensation. The error voltage is fed to the inverting input of the current-sense comparator via a voltage level shifter, while the sample of the inductor current is fed to the noninverting input of this comparator. This constitutes the inner current feedback loop of the current-mode controller. The on time is determined by both the voltage-sensing error amplifier output, V_e, and the current-sense comparator, which compares the error voltage V_e with the top of a ramp-on-a-step analog voltage from an external current sensing resistor. The comparator output is high only when the voltage error signal is higher than the sample of the inductor current. The UC3842 also includes an under-voltage-lockout feature that will only enable the controller if the supply voltage is above 16 V with a 6 V hysteresis, i.e., it will pull in when the supply voltage is 16 V and drop out when the supply voltage drops to about 10 V.

Current sensing and limiting. The UC3842 current sense input is configured as shown in Figure 5.21. Current-to-voltage conversion is per-

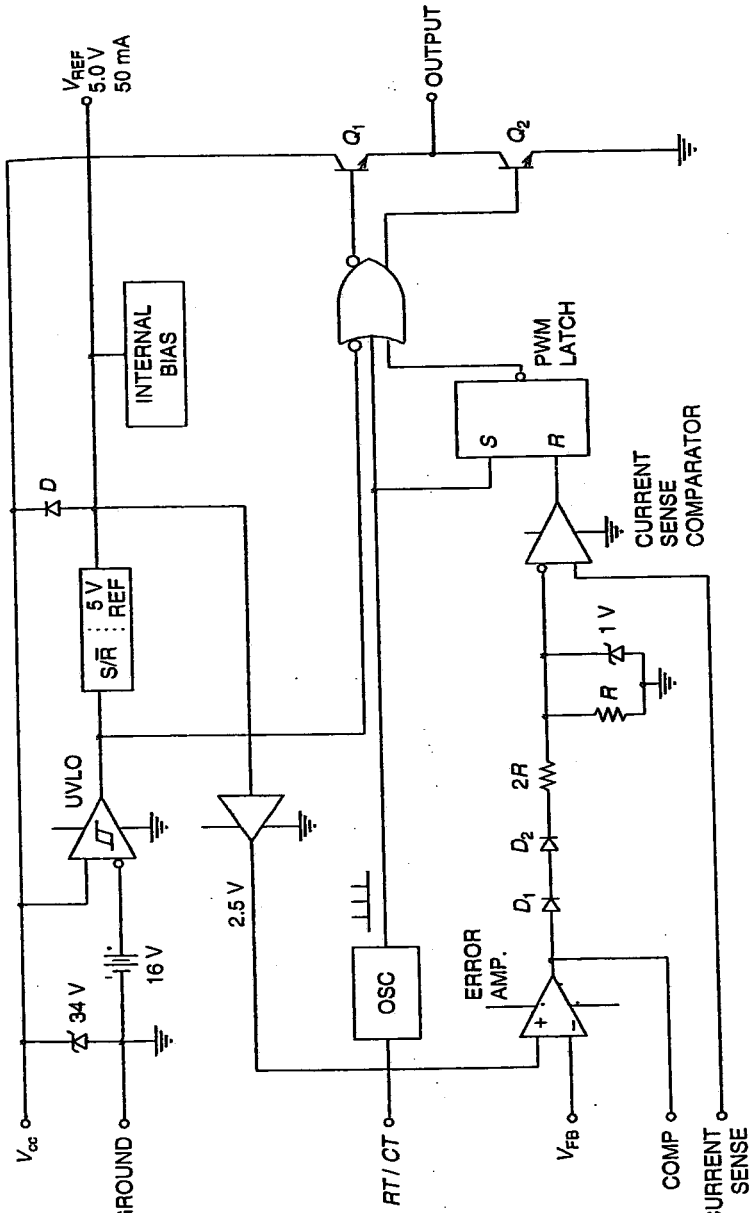


Figure 5.20 Functional block diagram of the UC3842 PWM controller. ([8], Reprinted by permission of Texas Instruments.)

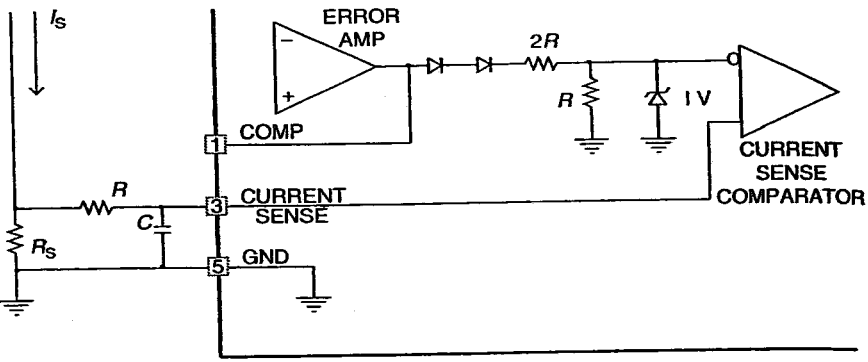


Figure 5.21 UC3842 current sensing.

formed externally using a ground-referenced resistor R_s. Under normal operation, the peak voltage across R_s is determined by the error amplifier according to the following relation:

$$I_p = \frac{V_c - 1.4\,\text{V}}{3R_s}, \tag{5.18}$$

where V_c is the control voltage and is equal to the output voltage of the error amplifier.

For purposes of small-signal analysis, the control-to-sensed-current gain is:

$$\frac{i_p}{v_c} = \frac{1}{3R_s}. \tag{5.19}$$

When the sensing current is flowing through a switching transistor, a large current spike at its leading edge is always present. This is due to the reverse recovery of the diode or the interwinding capacitance present in the power transformer, or both. If this transient is not attenuated, the output pulse may be prematurely terminated. A simple RC filter as shown in Figure 5.21 is usually sufficient to suppress this spike. The RC time constant should be approximately equal to the duration of the current spike that usually lasts for a few hundred nanoseconds.

The inverting input to the UC3842 current-sense comparator is internally clamped to 1 V. Current limiting occurs if the voltage at pin 3 reaches this threshold value, i.e., the current limit is defined by:

$$i_{max} = \frac{1\,\text{V}}{R_s}. \tag{5.20}$$

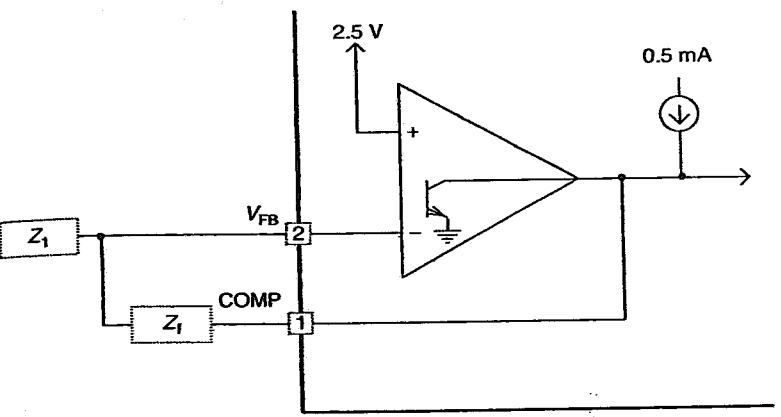


Figure 5.22 Error amplifier configuration.

Error amplifier. The error amplifier (E/A) configuration is shown in Figure 5.22. The noninverting input is not brought out to a pin, but is internally biased to 2.5 V ± 2%. The output of the error amplifier is available at pin 1 for external compensation, allowing the user to choose the desired closed-loop frequency response of the switching converter. Figure 5.23 shows a typical application for the UC3842 family in an off-line flyback switching power supply. The detailed design of this off-line power supply will be presented in Chapter 10.

5.4.4 TinySwitch-II Family of Low Power Off-Line Switchers [10]

In the TinySwitch-II family, a 700 V power MOSFET, oscillator, high voltage switched current source, current limit, and thermal shutdown circuitry are integrated to yield a controller with four effective pins, namely "Drain," "Source," "Enable," and "Bypass." In the normal operation of this device, a heat sink is not required. Unlike conventional PWM controllers, TinySwitch-II uses a simple ON/OFF control to regulate the output voltage. Figure 5.24 shows the functional block diagram along with some of its important features. The start-up and operating power are derived directly from the voltage on the "Drain" pin, eliminating the need for a bias winding and associated circuitry. In addition, the TinySwitch-II devices incorporate auto-restart, line undervoltage sense, and frequency jittering. The design also minimizes audio frequency components to practically eliminate audible noise with standard taped–varnished transformer construction. The auto-restart circuit limits the output power during fault conditions, such as output short circuit or open loop.

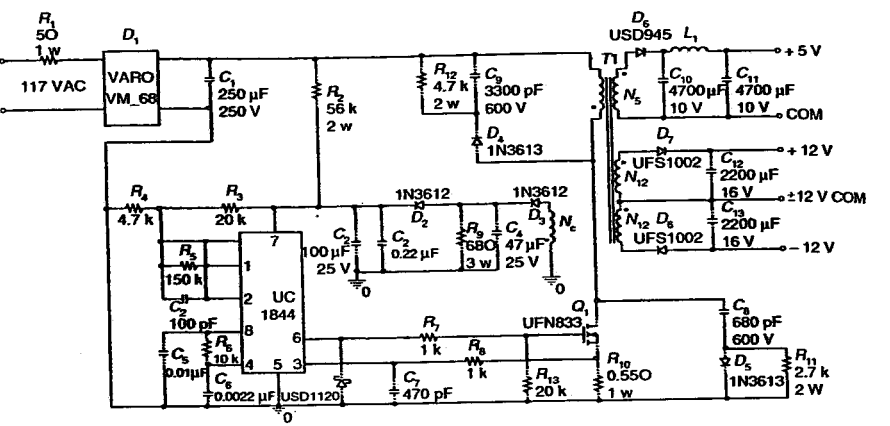


Figure 5.23 Off-line flyback regulator.

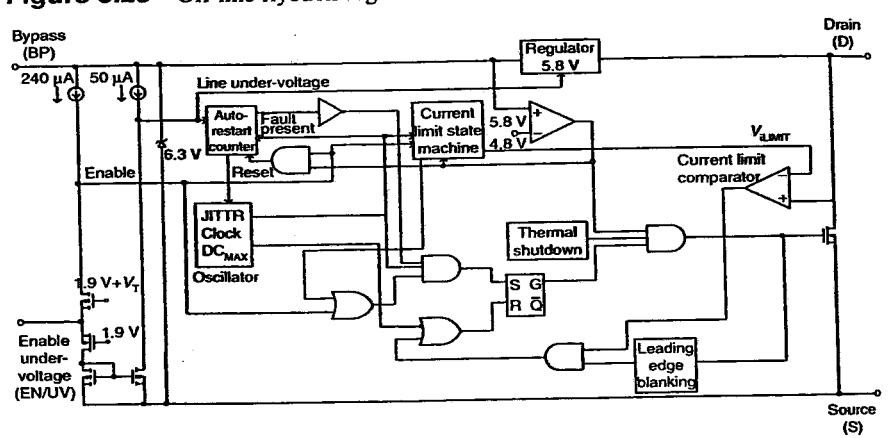


Figure 5.24 TinySwitch-II Functional block diagram. ([10], Reprinted by permission of Power Integrations, Inc.)

An optional line sense resistor externally programs a line under-voltage threshold, which eliminates power down glitches caused by the slow discharge of input storage capacitors in applications such as standby supplies. The operating frequency of 132 kHz is jittered to significantly reduce both the quasi-peak and average EMI, minimizing filtering cost.

TinySwitch-II devices operate in the current limit mode. When enabled, the oscillator turns the power MOSFET on at the beginning of

each cycle. The MOSFET is turned off when the current ramps up to the current limit or when the DCMAX limit is reached. Since the highest current limit level and frequency of the TinySwitch-II design are constant, the power delivered to the load is proportional to the primary inductance of the transformer and peak primary current squared. Hence, designing the supply involves calculating the primary inductance of the transformer for the maximum output power required. If the TinySwitch-II is appropriately chosen for the power level, the current in the calculated inductance will ramp up to current limit before the DCMAX limit is reached. Figure 5.25 shows a typical application of the TinySwitch, implementing a universal power supply, where the input AC voltage can range from 85 to 265 V.

5.5 CONTROL SCHEMES FOR RESONANT CONVERTERS

The output of the resonant converter is regulated by changing its switching frequency. As in the conventional converters, the output voltage is first compared with a fixed reference voltage in an error amplifier. The output of the error amplifier determines the frequency of the output waveform of a voltage-control-oscillator (VCO). This VCO controller can be implemented using a combination either of digital–analog integrated circuits or by a microprocessor. A circuit schematic of a digital–analog implementation of this VCO controller for a push–pull resonant converter is shown in Figure 5.26. It consists of a CD4046 digital phase-locked-loop, a CD4013 D-flip-flop, a CD4528 retriggerable–resetable monostable multivibrator, a CD4050 hex buffer, and two CD4081 AND gates. The CD4046 generates switching pulses of varying frequencies, $v_y(t)$, according to the error voltage, $v_x(t)$,

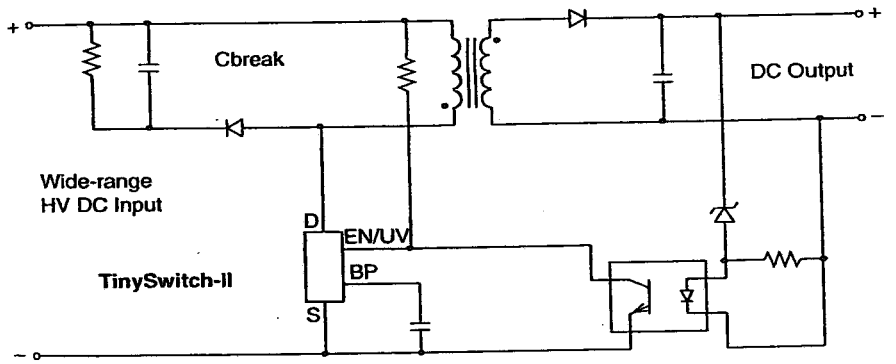


Figure 5.25 TinySwitch typical standby application. (From TNY 264/266-268 TinySwitch-II. Family data sheets, Power Integrations, Inc., April 2003. With permission.)

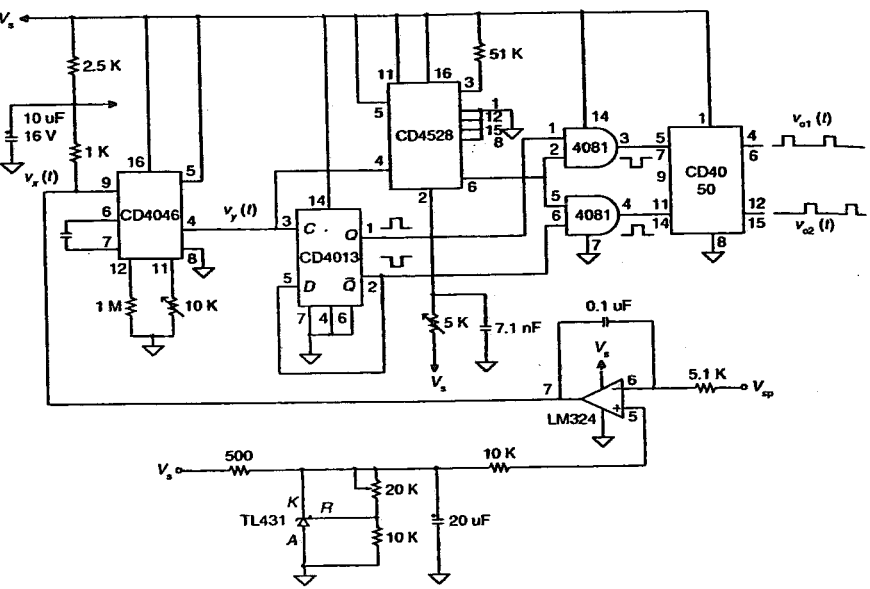


Figure 5.26 Circuit schematic of a digital–analog integrated circuit implementation of a VCO for push–pull resonant converter.

from the error amplifier, as shown in Figure 5.27. These variable-frequency pulses are fed to the inputs of the CD4013 D-FF and the CD4528 monostable multivibrator. The CD4013 D-FF generates an out-of-phase signal to yield the out-of-phase signals Q and $\bar{Q}$, necessary to drive the push–pull converter topology. The pulse-width of these pulses is controlled by the combination of the CD4528 and CD4011 through the adjustment of the 5-kΩ potentiometer, connected to pin 2 of the CD4528 multivibrator. The CD4050 hex buffer provides the drive capability to the gate drive circuitry and usually consists of a totem-pole configuration for fast switching in power MOSFET output transistors.

Current-mode control eliminates the need for a voltage-controlled-oscillator in some quasi-resonant converters [11]. This control scheme also increases the noise immunity of the quasi-resonant converter since the function of the voltage-controlled oscillator is now replaced by a simple voltage comparator whose operation is far less noise sensitive. Figure 5.28 shows a circuit schematic of a direct-inductor current sensing implementation of a current-mode control for a quasi-resonant buck converter. The error amplifier compares the sampled output voltage, V_a', with a fixed reference voltage V_{ref}. The output of the error amplifier is then compared

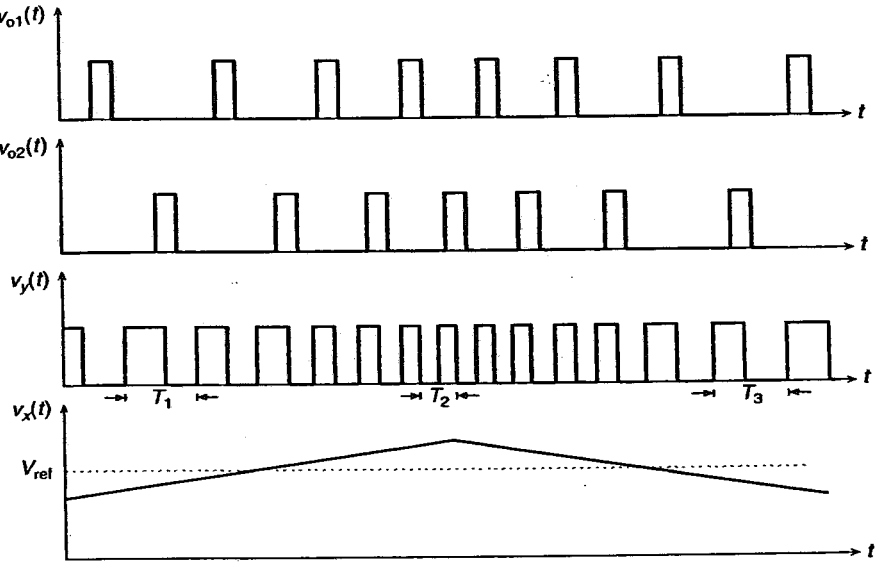


Figure 5.27 Waveforms for the VCO controller.

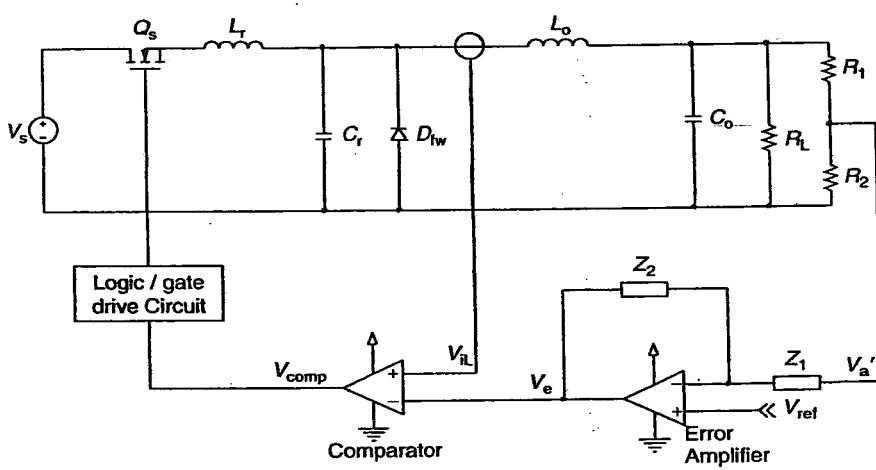


Figure 5.28 A current-mode-controlled quasi-resonant buck converter.

with the sample of the output inductor current, v_{iL}, in a voltage comparator. The output of the comparator is then used to provide constant on time pulses to the switching transistor Q_s via a combination of logic and drive circuitry. The switching transistor Q_s is switched on when the down-slope of the sample of the output inductor current intersects the error voltage as shown in Figure 5.27.

5.5.1 Off-Line Controllers for Resonant Converters

Half-bridge quasi-resonant controllers are available commercially for off-line switching converter applications. Their main applications are in universal power supplies for TVs and monitors, battery chargers, power supplies for telecommunications equipment and car radios, and high-voltage power supplies.

5.5.1.1 L6598 Operation [12,13]

The STMicroelectronics' L6598 is designed for applications based on half-bridge topology, using a 50% duty cycle at variable frequency. In this type of switching converter, control of the output parameters will be accomplished by changing the switching frequency. Figure 5.29 shows the functional block diagram for the L6598 controller. This controller has an under-voltage lock-out (UVLO) feature. Below the UVLO threshold, both the high- and low-side drivers for the external power MOSFETs remain off. As the supply voltage is beyond the UVLO threshold, the circuit is operational. The low side driver is active during the first half switching period, fully charging the bootstrap capacitor. One salient feature is that the integrated bootstrap function does not require an external diode to charge the bootstrap capacitor. By choosing the appropriate biasing using R_{fmin} and R_{fstart}, one can define the minimum and maximum frequency operation limits of the current controlled oscillator. The device has a soft start function with a delay capacitor, C_{ss}, which controls the time for the soft start. At start up, the frequency is set to the maximum value (F_{max}) and will gradually decrease to the desired operating frequency. The oscillator controls the power stage circuit from the low and high side gate drivers that are connected to the external power MOSFETs. The closed-loop frequency is controlled by the value of R_{fmin}. The high current carrying capability of the high- and low-side drivers (typically 450 mA source and 250 mA sink), ensures fast switching transitions for the external power MOSFETs. At the same time, the internal logic ensures a typical dead time of 300 ns between the turn on and off of both switches.

A typical application for the L6598 is the multiresonant zero-current-switching (ZCS) converter for a high-end TV power supply as shown in Figure 5.30. Its simplified schematic is shown Figure 5.31. A half-bridge resonant topology is chosen due to its small size, high efficiency, and low

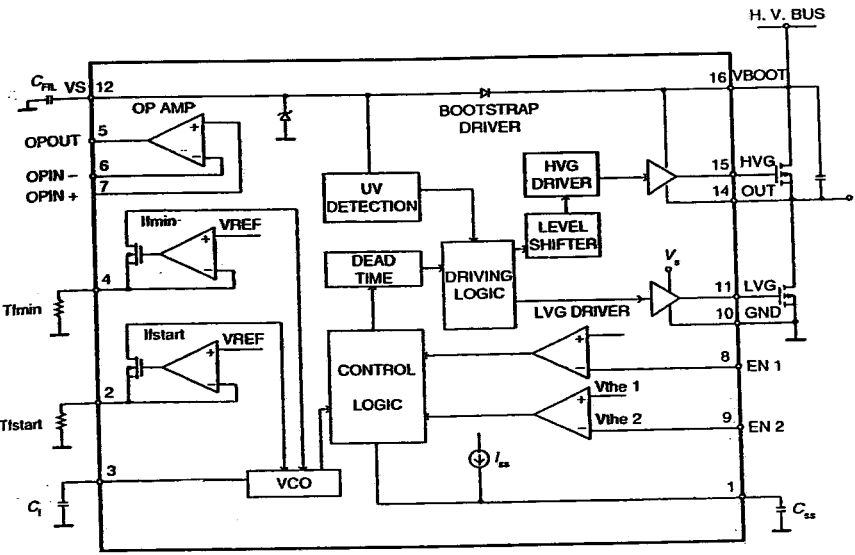


Figure 5.29 Block diagram of the L6598. ([12], Reprinted by permission of STMicroelectronics.)

noise operation. The operating waveforms are shown in Figure 5.32. This half-bridge converter consists of the power MOSFETs, Q_1 and Q_2, the resonant inductor L_1, the magnetizing inductance of the transformer L_2, the resonant capacitors C_1 and C_2, rectifier diodes D_1 and D_2, and the output capacitor C_{out}. C_{Q1} and C_{Q2} are the parasitic capacitors of the Q_1 and Q_2, respectively. D_{Q1} and D_{Q2} are the parasitic reverse diodes of Q_1 and Q_2, respectively. The two power MOSFETs, Q_1 and Q_2, are switched on alternatively at near 50% duty cycle. This circuit has three modes of operation.

Mode 1. In this mode, the series resonance of the circuit formed by L_1 and $C_1 + C_2$, supplies power to the load.

Mode 2. Resonance occurs between $L_1 + L_2$ and $C_1 + C_2$, without supplying power to the load.

Mode 3. In this mode of operation, resonance occurs between $C_{Q1} + C_{Q2}$, $L_1 + L_2$ and $C_1 + C_2$, allowing the zero-voltage switching of the MOSFET. There are eight operating intervals as shown in Figure 5.31.

$t_0 - t_1$. During this time interval, a reverse current flows in Q_1 through the parasitic diode, D_{Q1}. Q_2 is switched off. The initial value of the resonant current between L_1 and $C_1 + C_2$ at t_0 is $-I_2$, which coincides with the current flowing through L_2. The current flowing through L_2 increases at the rate of

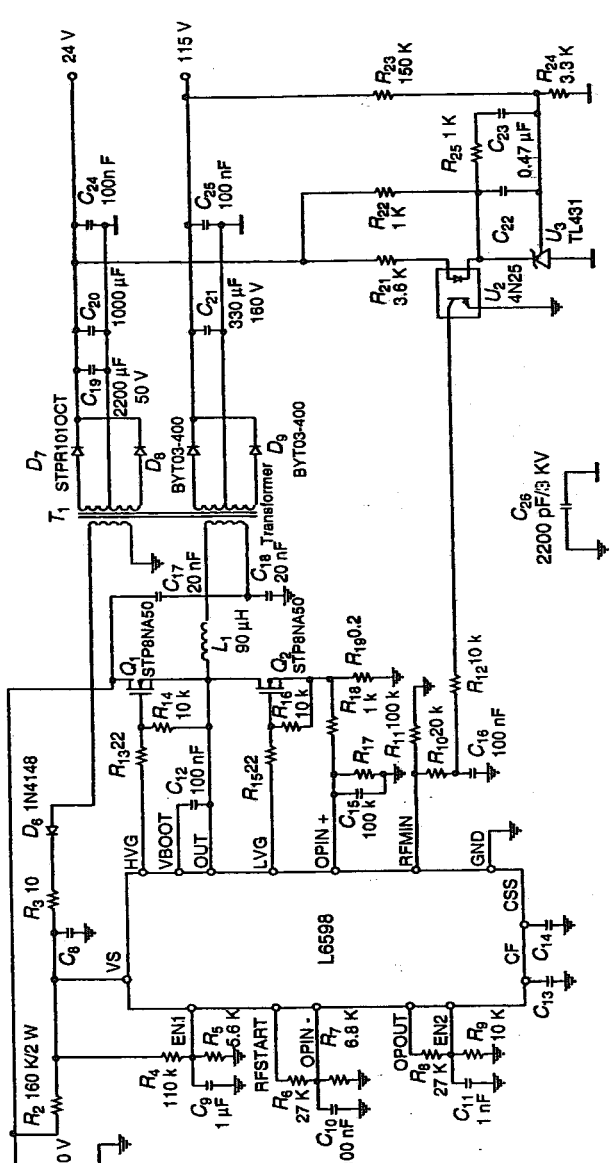


Figure 5.30 Resonant converter with the L6598: Electrical diagram. ([13], Reprinted by permission of STMicroelectronics.)

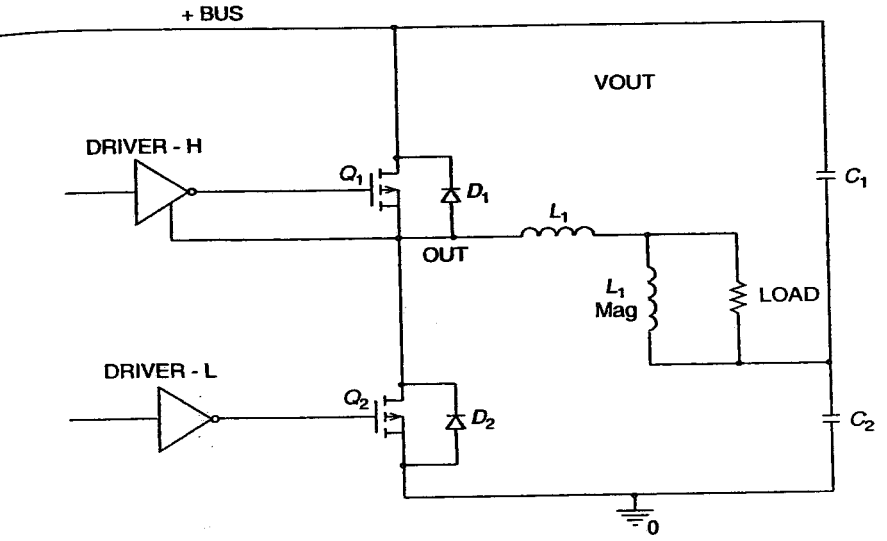


Figure 5.31 Typical application of the L6598. ([13], Reprinted by permission of STMicroelectronics.)

nV_{out}/L_2, where $n = N_1/N_2$ and $N_2 = N_3$. At t_0, C_{Q1} is completely discharged; therefore, the voltage across Q_1 becomes zero and zero-voltage switching (ZVS) is achieved. The voltage across C_2 decreases while C_2 is discharged.

$t_1 - t_2$. During this time interval, Q_1 is switched on and Q_2 is switched off. The resonant current flows through Q_1 in the positive direction. The resonant current increases sinusoidally and reaches the maximum value, then deceases until it coincides with the current in L_2 at t_2. The difference between the resonant current and the current in L_2 flows through the primary winding N_1 of the transformer (see Figure 5.30). In this interval, power is supplied to the load.

$t_2 - t_3$. During this time interval, Q_1 remains on and Q_2 remains off. The current I_1 flowing through L_1 coincides with the current in L_2 at t_2. No current flows through the secondary winding of the transformer. In this mode, $L_1 + L_2$ and $C_1 + C_2$ resonate.

$t_3 - t_4$. This interval starts when Q_1 switches off at t_3. Both Q_1 and Q_2 are off. The charge stored in the parasitic capacitor C_{Q2} of Q_2 is discharged by means of the resonant current between $L_1 + L_2$ and $C_1 + C_2$. At the same time C_{Q1} is charged.

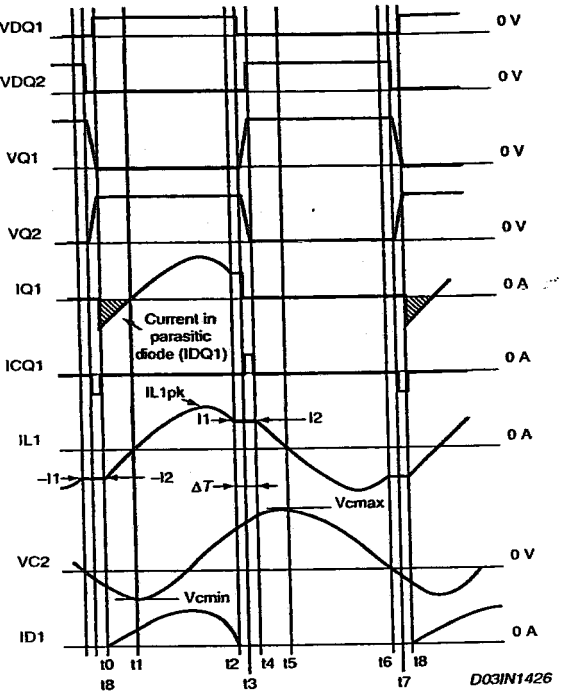


Figure 5.32 Switching waveforms. ([13], Reprinted by permission of STMicroelectronics.)

$t_4 - t_5$. During this time interval, Q_1 remains off and the resonant current flows through the parasitic diode of Q_2, D_{Q_2}. At t_4, C_{Q_2} is completely discharged and the voltage across Q_2 becomes zero, achieving the ZVS. The voltage of C_2 increases further.

$t_5 - t_6$. During this time interval, Q_1 remains off and Q_2 is switched on. The resonant current flows through Q_2 in the opposite direction that was flowing during the time interval from t_4 to t_5. The resonant current decreases sinusoidally and reaches the minimum value; then increases until it coincides with the current in L_2 at t_6. The difference between the resonant current and the current in L_2 flows through the primary winding N_1 of the transformer. In this interval, power is supplied to the load.

$t_6 - t_7$. During this time interval Q_1 remains off and Q_2 remains on. The current $-I_2$ in L_1 is equal to the current flowing through L_2 at t_6. No current flows through the secondary winding of the transformer. In this mode, $L_1 + L_2$ and $C_1 + C_2$ resonate.

$t_7 - t_8$. During this time interval, Q_2 turns off at t_7. Thus, Q_1 and Q_2 are both switched off during this interval. The parasitic capacitor C_{Q_2} of Q_2 is charged by means of the resonant current that flows through $L_1 + L_2$ and $C_1 + C_2$. At the same time, C_{Q_1} is discharged. At time t_8, the circuit returns to the first mode and the cycle is repeated.

A main feature of this resonant converter is the ZVS of the power MOSFETs. However, there are still turn-off switching losses, but they can be reduced by placing small snubber capacitors directly across the MOSFETs. Discharge resistors are not needed in the snubber, because the capacitor is not discharged by turning on the power MOSFET, but rather by turning off the opposite power MOSFET. The switching losses due to C_{oss} and C_{rss} are also eliminated by the snubbers. The energy stored in the capacitors across the switching device is returned to the DC source through the opposite device when turned off.

PROBLEMS

5.1. A pulse-width modulator is shown in Figure 5.33. Operational amplifiers for the error amplifier and the comparator are considered to be ideal. The minimum sawtooth signal is 1 V with a peak of 3 V and a frequency of 1 kHz. Determine the error voltage, V_e, of the error amplifier if the feedback voltage is 2 V and the reference voltage is 1.8 V. Sketch waveforms at the outputs of the AND gates for four switching periods.

5.2. Design a pulse-width modulator based on the SG3524 for the boost converter shown in Figure 2.11. The input voltage, V_s, is 9 V and the average output voltage, V_a, is 12 V. The switching frequency is 1 kHz. Component values for the boost converter are: $C = 100\ \mu F$, $L = 10\ mH$, and $R_L = 10\ \Omega$.

5.3. Design a 5-W continuous conduction mode flyback converter using the UC3842 current-mode controller. The line input voltage is 110 V at 60 Hz. The load requires an output voltage of 5 V $\pm$ 50 mV at a load current of 1 A.

5.4. A solar cell panel provides the energy for a meteorological station that gathers data and sends them via an RF link. The terminal voltage of the solar cell depends on the energy from the photons impacting on its surface. Therefore, the available DC voltage across the solar panel fluctuates between 17 and 21 V during the daylight hours (when the equipment is used). The electronic equipment requires a DC voltage of 5 V $\pm$ 5%; as such voltage regulation is required at the load. The load

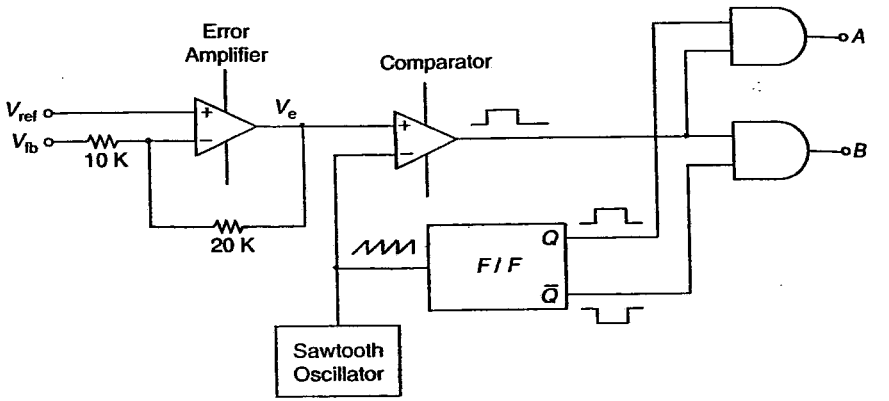


Figure 5.33 Pulse-width modulator for Problem 5.1.

current may change from 300 mA to 1 A. Design a switching voltage regulator using the integrated circuit TL494 that would provide the appropriate voltage to the meteorological station. The regulator has to be designed to operate in the discontinuous mode.

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6

Dynamic Analysis of Switching Converters

6.1 INTRODUCTION

In the preceding chapters, analyses of switching converter topologies have so far been performed under the steady state condition. Predicting its dynamic characteristics has not been easy due to the complexity of the operation of the switching converter. The dynamic characteristic of the switching converter can be used to predict: (a) the margin of stability of the switching converter, (b) the input supply ripple rejection and the transient response due to input supply perturbation, (c) the output impedance and the transient response due to load perturbation, and (d) the compatibility with the input electromagnetic interference (EMI) filter [1]. Thus, dynamic or small-signal analysis of the switching converter enables designers to predict the dynamic performance of the switching converter to reduce prototyping cost and design cycle time. Generally, dynamic analysis can be either numerical or analytical. Numerical methods can be useful for computer simulations, but they cannot reveal basic relationships among circuit elements in the switching converter. Switching converters are

nonlinear time-variant circuits. Nevertheless, it is possible to derive a continuous time-invariant linear model to represent a switching converter. Continuous-time models are easier to handle, but not very accurate. Since a switching converter is a sampled system, a discrete model gives a higher level of accuracy, and also models some aspects of the converter (like the instability in current-mode control) that are not covered by a continuous model. A discrete-time modeling technique, such as sampled data modeling [2,3] must be used for this last case, or when more accurate results are needed.

This chapter is divided in two parts; the first part discusses continuous-time models for switching converters, while the second part presents a discrete-time model.

In Part I, classical control techniques are used to analyze and stabilize closed-loop switching converters. A brief review of negative feedback applied to electronic circuits is performed. The stability analysis is performed using Bode plots, and a compensator is calculated to shape the loop gain to a desired phase margin. Variations on the load are modeled as a small-signal current source at the output of the converter. The output impedance is calculated to evaluate the effect of the variations of the output current on the output voltage. Output impedance and load variations are related to stability and transient response. The concept of audio susceptibility is introduced and the corresponding transfer function calculated.

After a review of linear system analysis using state–space representation, the state–space averaging model developed by Middlebrook and Cûk [4] is introduced. The transfer function and loop compensations are calculated using state–space representation. A method based on full-state feedback is explained, which permits locating the closed-loop poles of the converter to achieve a desired dynamic response. This method is more precise than using the phase margin method. In Section 6.2.12, the need for an EMI filter is described and its influence on the converter stability is analyzed.

Part II discusses the discrete-time modeling of switching converters. This modeling technique is more accurate than the continuous-time modeling and suitable for controller implementation using a DSP chip. After developing a discrete-time model, a full-state feedback technique is used to place the closed-loop poles to obtain a desired transient response. The use of additional dynamics permits achieving a zero steady-state error. Both voltage-mode and current-mode control schemes are discussed.

6.2 CONTINUOUS-TIME LINEAR MODELS

6.2.1 Switching Converter Analysis Using Classical Control Techniques

Within certain limits, classical control techniques can be applied to switching converters. Different degrees of accuracy can be achieved depending on the model. A basic small-signal linear model of a switching converter is first introduced.

6.2.1.1 Basic Linear Model of the Open-Loop Switching Converter

This model considers all the constitutive blocks of the switching converter as de-coupled blocks. Therefore, it is not applicable to all cases. Nevertheless, it provides a first insight to the calculation of the gain of each individual block. The block diagram and small-signal linear model for a switching converter are shown in Figure 6.1.

The reference voltage, V_{ref}, enters the pulse-width modulation (PWM) block to generate the nominal duty cycle, D, that drives the switches of the

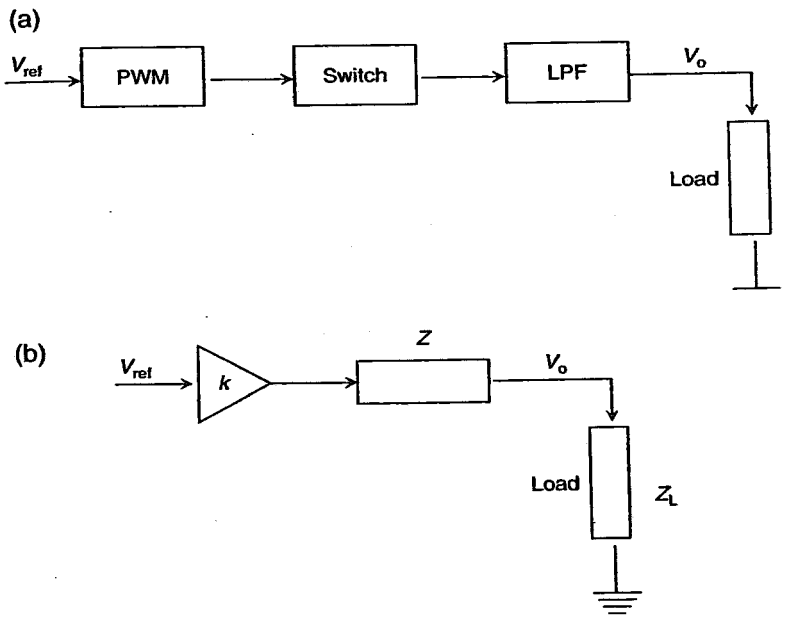

Figure 6.1 Linear model of a switching converter.

power stage. Since this is a small-signal linear approximation of the switching converter, no switching action takes place in the power stage. Instead, the output of the power stage is a modulated DC value, which is a function of D multiplied by the unregulated DC input voltage, V_{DC}. This waveform enters the low-pass filter, allowing only the DC component and the low-frequency dynamics of the circuit to reach the load. A linear circuit approximation of the switching converter is shown in Figure 6.1(b), where Z_o is the output impedance of the switching converter, Z_L is the load impedance and K is the open-circuit gain. The DC output voltage is given by:

$$V_o = \frac{Z_L}{Z_o + Z_L} k V_{ref}, \tag{6.1}$$

where k is a function of V_{DC} that depends on the PWM modulator implementation. Then, if Z_L or V_{DC} varies, it will be reflected in the output voltage. If V_o needs to be bounded between certain limits, then a closed-loop controller is required. Various models for the constitutive blocks of the block diagram of the linear switching converter shown in Figure 6.1(a) are discussed in the following sections.

6.2.1.2 PWM Modulator Model

6.2.1.2.1 Voltage-mode control. The PWM modulator generates the duty cycle, D, by comparing a sawtooth (or triangular) signal to the reference voltage, V_{ref}. For a voltage-mode constant-frequency PWM modulator, the sawtooth signal is applied to the inverting input while the V_{ref} is applied to the noninverting input of the error amplifier. The output of the comparator is high at the beginning of the switching period, and remains high until the ramp reaches the reference voltage and the output changes to a low level. The width of the output pulse is DT. The DC gain of the PWM modulator can be easily calculated from Figure 6.2 using a geometric method. Consider a sawtooth signal of period T and amplitude V_p, for the nominal reference voltage, V_{ref}, the nominal duty cycle, D, is given by:

$$D = \frac{V_{ref}}{V_p}. \tag{6.2}$$

When a perturbation on the reference voltage $\hat{v}_{ref}$ is applied, it produces a variation on the duty cycle, $\hat{d}$, which can be calculated by comparing the two shaded areas, yielding

$$\hat{d} = \frac{D}{V_{ref}} \hat{v}_{ref} = \frac{1}{V_p} \hat{v}_{ref} \tag{6.3}$$

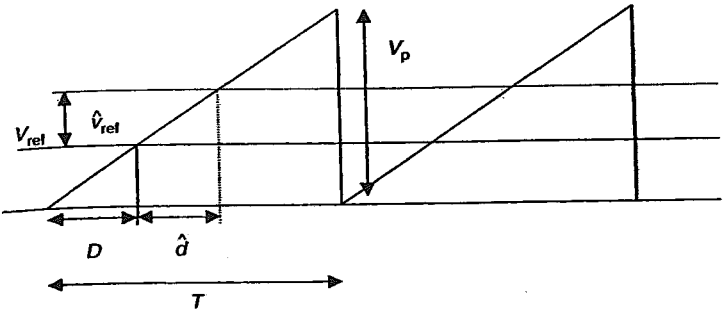

Figure 6.2 Sensitivity of the duty cycle with respect to v_{ref}.

6.2.1.2.2 Current-mode control. In current-mode control, the inductor current is compared with a reference current, I_p, to determine the nominal duty cycle, D. At the beginning of each switching cycle, the inductor current increases linearly, until it reaches the amplitude set by I_p. The switch driving the inductor is turned off and the current decreases linearly until the next switching cycle.

The positive slope of the inductor current is given by

$$\frac{di_L}{dt} = \frac{V_L}{L} = \frac{I_p - I_1}{D}, \tag{6.4}$$

where I_1 is the magnitude of the inductor current at the beginning of the switching cycle.

Then, the nominal duty cycle is determined by

$$D = \frac{(I_p - I_1)L}{V_L}. \tag{6.5}$$

A linear expression for $\hat{d}$ can be found by approximating the function with the linear terms of its Taylor series expansion. Thus,

$$\hat{d} = \frac{\partial d}{\partial i_L}\hat{i}_L + \frac{\partial d}{\partial v_c}\hat{v}_c + \frac{\partial d}{\partial I_p}\hat{I}_p. \tag{6.6}$$

The sensitivities of Equation (6.6) are different for every switching converter. They are usually evaluated by a geometrical analysis, similar to the one performed in Figure 6.2.

Example 6.1. Calculate the approximate linear expression of $\hat{d}$ for a current-mode buck converter operating in the continuous-conduction mode.

Solution. The first term on the right-half hand of Equation (6.6) represents the sensitivity of the duty cycle as a function of the current through the inductor. Figure 6.3 shows the variation of the duty cycle due to a perturbation $\hat{i}_L > 0$ on the inductor current at $t = 0$.

If the input and output voltages are considered constant during t_{on}, then the slope of the ramp corresponding to the inductor current does not change. There is only a vertical shift given by $\hat{i}_L$. The slope of the ramp in this interval is given by:

$$r = \frac{V_d - V_c}{L}. \tag{6.7}$$

An analysis of the figure shows that:

$$\hat{i}_L = r(-\hat{d}T) \tag{6.8}$$

and solving:

$$\hat{d} = -\frac{L}{(V_d - V_c)T}\hat{i}_L. \tag{6.9}$$

Therefore,

$$\frac{\partial \hat{d}}{\partial \hat{i}_L} = -\frac{L}{(V_d - V_c)T}. \tag{6.10}$$

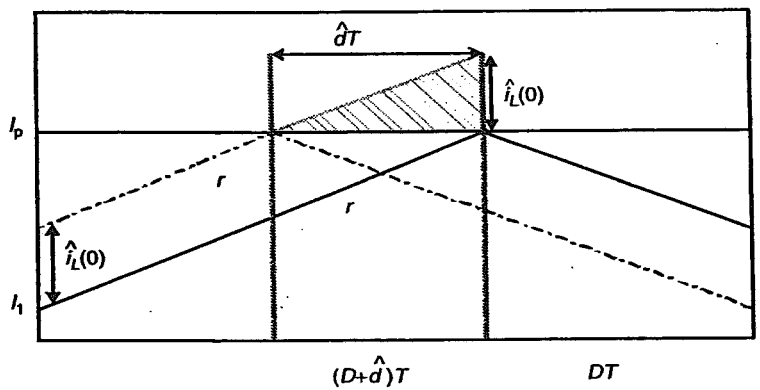

Figure 6.3 Variation of the duty cycle due to a perturbation in the inductor current.

The sensitivity of the duty cycle as a function of the voltage across the capacitor can be evaluated from Figure 6.4. A perturbation on the output voltage changes the slope of the inductor current waveform during t_{on}.

To obtain the expression for $\hat{d}$ as a function of $\hat{v}_c$, the equations for the slopes corresponding to the nominal (r_1) and perturbed (r') cases are analyzed.

$$r_1 = (V_d - V_c)/L \tag{6.11}$$

$$r' = [V_d - (V_c + \hat{v}_c)]/L. \tag{6.12}$$

Also, from the figure

$$r_1 = \Delta I/DT \tag{6.13}$$

$$r' = \Delta I/(D + \hat{d})T. \tag{6.14}$$

Dividing r_1 by r',

$$\frac{r_1}{r'} = \frac{\Delta I/DT}{\Delta I/(D+\hat{d})T} = \frac{(V_d - V_c)/L}{[V_d - (V_c + \hat{v}_c)]/L} \tag{6.15}$$

and solving for $\hat{d}$ yields:

$$\hat{d} = D\left[\frac{\hat{v}_c}{V_d - V_c - \hat{v}_c}\right]. \tag{6.16}$$

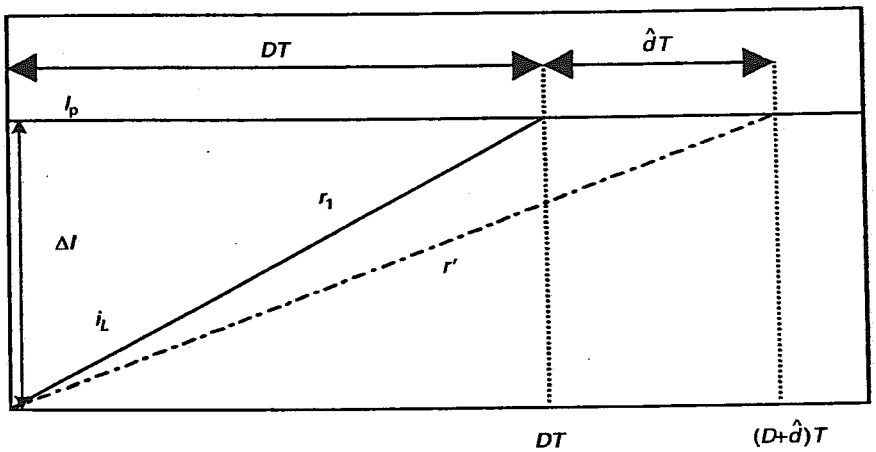

Figure 6.4 Variation of the duty cycle due to a perturbation in the output voltage.

Considering $\hat{v}_c \ll (V_d - V_c)$ the following approximation can be obtained:

$$\hat{d} = \hat{v}_c \left[\frac{D}{V_d - V_c}\right]. \tag{6.17}$$

Thus,

$$\frac{\partial \hat{d}}{\partial \hat{v}_c} = \left[\frac{D}{V_d - V_c}\right]. \tag{6.18}$$

The sensitivity of the duty cycle as a function of the control variable I_p may be evaluated from Figure 6.5. The peak current through the inductor, I_p, will be set by the control strategy. A perturbation on its value has the following effects on the nominal duty cycle:

$$\hat{d}T = \frac{\hat{I}_p}{r}, \tag{6.19}$$

where

$$r = \frac{V_d - V_c}{L}. \tag{6.20}$$

Then,

$$\hat{d} = \frac{\hat{I}_p}{T} \frac{L}{V_d - V_c}. \tag{6.21}$$

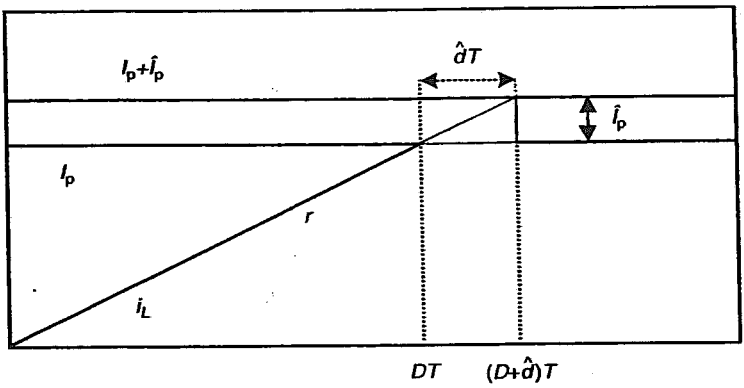

Figure 6.5 Variation of the duty cycle due to a perturbation on the peak current.

Thus,

$$\frac{\partial \hat{d}}{\partial \hat{I}_p} = \frac{1}{T} \frac{L}{V_d - V_c}. \tag{6.22}$$

6.2.1.3 Averaged Switching Converter Models

6.2.1.3.1 Averaged-switch model for voltage-mode control. Vorpérian [5] developed an averaged-switch model, which replaces the nonlinear switching action of the converter using a simple small-signal equivalent circuit. This model can be used for all two-switch PWM converters in either the continuous-conduction mode or discontinuous-conduction mode of operation. Figure 6.6 shows the three-terminal averaged switch model. The amplitudes of the two dependent sources are determined by the DC operating conditions of the power stage.

The voltage source, v_1, is determined by the steady-state DC voltage across the active and passive terminals, and the duty cycle of the power stage; i.e.,

$$v_1 = \frac{V_{ap}}{D} \hat{d}. \tag{6.23}$$

The current source is determined by the steady-state DC current, I_c, of the common terminal.

$$i_1 = I_c \hat{d}. \tag{6.24}$$

Both dependent sources are controlled by the duty cycle modulation, $\hat{d}$. The polarities and current directions must be consistent throughout the analysis. Figure 6.7 shows the small-signal models with an averaged switch for the buck and boost converters. Notice that the averaged switch replaces both the

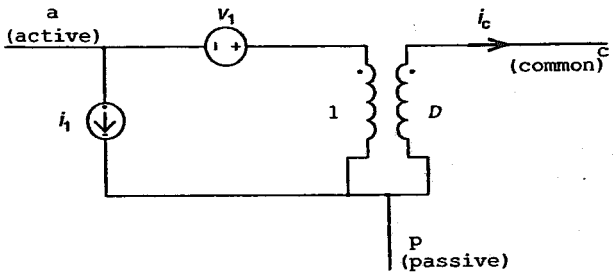

Figure 6.6 Three-terminal averaged-switch model

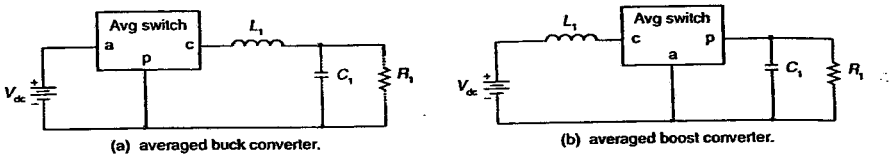

Figure 6.7 Examples of switching converters with an averaged switch.

transistor and the diode. The common terminal is connected to the node where the transistor and the diode are connected together. The active terminal is the other end of the transistor and the passive terminal is the other end of the diode.

The main advantage of this model is that once the switching devices have been replaced by the averaged switch model, linear circuit analysis techniques can be applied to analyze the circuit. Moreover, PSpice can be used to simulate the small-signal AC and transient behaviors of the converter. The library swit_rav.lib, included in PSpice, contains averaged-switch models for voltage-mode, current-mode, continuous-conduction and discontinuous-conduction modes of operation.

The averaged switch model for the discontinuous conduction mode [5] is shown in Figure 6.8. The values of the parameters are given by:

$$g_i = \frac{I_a}{V_{ac}}, \quad I_1 = 2\frac{I_a}{D}\hat{d}, \quad I_2 = 2\frac{I_p}{V_{ac}}\hat{v}_{ac}, \quad I_3 = 2\frac{I_p}{D}\hat{d}, \quad g_o = \frac{I_p}{V_{cp}}. \tag{6.25}$$

Notice that the sources are controlled by the modulation of the duty cycle in both the continuous and discontinuous conduction models. Therefore, most averaged-switch components for circuit simulation program have a

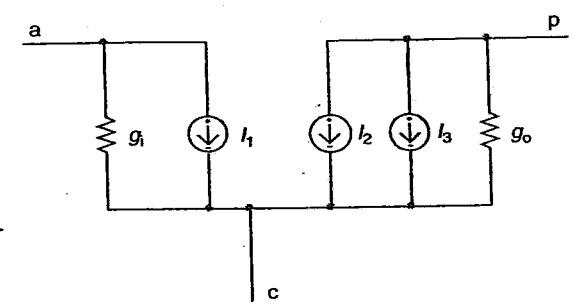

Figure 6.8 Small-signal averaged-switch model for the discontinuous mode.

fourth terminal to incorporate the duty cycle modulation. The PWM modulator has to be modeled on a separate block, as shown in Section 6.2.1.2.

6.2.1.3.2 Averaged-switch model for current-mode control. Ridley [6] expanded the voltage-mode averaged-switch model for current-mode control that is valid up to half the switching frequency. All the small-signal characteristics of current-mode control are predicted, including low-frequency effects and high-frequency subharmonic oscillation. This model can also be used for all switching converters using constant frequency, constant on-time, or constant off-time control [7]. The linearized continuous sampled data model is approximated by a second-order system as follows:

$$H_e(s) = 1 + \frac{s}{\omega_n Q_z} + \frac{s^2}{\omega_n^2}, \tag{6.26}$$

where

$$Q_z = \frac{-2}{\pi} \tag{6.27}$$

and

$$\omega_n = \frac{\pi}{T_s}, \tag{6.28}$$

where T_s is the period of the compensating ramp.

As shown in Figure 6.9, the power stage model remains the same as that in Figure 6.7, except that current-sensor and gain blocks have been added to represent the current feedback. The resistance R_i is the linear gain of the current-sense network, and $H_e(s)$ models the sampling action of the current-mode control. With no current feedback, R_i and the gains k_f and k_r are zero. In this case, the model consists of only the voltage-mode control loop. Other parameters are:

$$k_f = \frac{-DT_sR_i}{L}\left(1 - \frac{D}{2}\right), \quad k_r = \frac{(1-D)^2 T_s R_i}{2L}, \quad F_m = \frac{1}{(S_n + S_c)T_s}, \tag{6.29}$$

where F_m is the modulator gain, S_n and S_c are the slopes of the sensed-current ramp and the compensation ramp, respectively. Contrary to the averaged-switch model, the PWM modulator is included in this model. Therefore, the control input for Ridley's average model is the error voltage, $\hat{v}_c$.

Other averaged models of the switching converters have been developed, like the averaged-inductor model by Yaakov [8]. This model replaces the inductor and the switches by a block that models their average behavior.

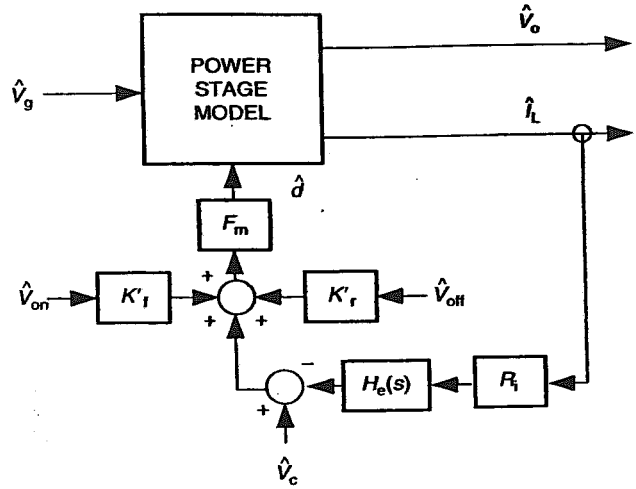

Figure 6.9 Small-signal model for current-mode control. (From Figure 5 of Ridley, R.B., A new continuous-time model for current-mode control, *IEEE Trans. Power Electron.*, pp. 271–280, April 1991. With permission.)

In contrast with the averaged-switch-based PSpice components, a different component is needed in PSpice for each averaged-inductor switching converter model. Chapters 9 and 10 include examples of the use of averaged models in PSpice simulations.

6.2.1.4 Switch Losses

The ON resistance of the MOSFET transistor will only affect the amplitude of the square waveform applied to the low-pass filter, according to $D\,R_{on}$, where D is the duty cycle and R_{on} is the on resistance of the switching device. The voltage drop across the diode may be modeled by an ideal voltage source in series with the passive terminal of the small-signal model circuit.

6.2.1.5 Switch Delay

The time delay associated with the switch may play an important role in the evaluation of the phase margin. The time delay contribution to the phase margin is:

$$\text{phase (delay)} = -360 \times t_{delay} \times f_1, \tag{6.30}$$

where t_{delay} is the time delay in seconds and f_1 is the unity-gain crossover frequency. This phase delay must be added to the loop phase to determine a

more accurate phase margin. The phase delay degrades the phase margin because its sign is negative.

6.2.1.6 Output Filter Model

The output filter model can only be calculated separately for those switching converters where the switching devices cannot be merged into the output filter such as in a buck converter. For all the other topologies, the filter transfer function is affected by the switching action. Therefore, the switching converter transfer function is generally evaluated using an averaged model.

The output filter of a buck converter is used as an example to evaluate the response of a second-order system. The frequency response of the output filter often dictates the required feedback compensation in a buck-switching converter. The output filter L_oC_o is essentially a second-order low-pass filter. The transfer function of this output filter can be derived by transforming the reactive components into their s-domain parameters, as shown in Figure 6.10. The output voltage $V_o(s)$ is

$$V_o(s) = \frac{R_o//(1/sC_o)}{sL_o + (R_o//(1/sC_o))} V_s(s). \tag{6.31}$$

The transfer function of the output filter is then

$$\frac{V_o(s)}{V_s(s)} = \frac{(1/C_oL_o)}{s^2 + (s/C_oR_o) + (1/L_oC_o)}. \tag{6.32}$$

It can be shown from feedback system theory [9] that the transfer function of a second-order system can be represented as

$$H(s) = \frac{\omega_o^2}{s^2 + 2\zeta\omega_o s + \omega_o^2}, \tag{6.33}$$

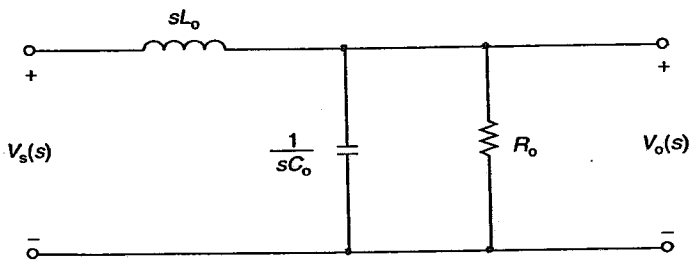

Figure 6.10 Output filter of a switching converter.

where ζ is the (dimensionless) damping ratio and ω_o is the natural frequency of the system. When $\zeta = 1$, the response is critically damped. When $\zeta < 1$, the response is underdamped. The response is increasing oscillatory as ζ approaches zero. When $\zeta > 1$, the response is overdamped. Comparing Equation (6.33) to Equation (6.32), the damping ratio and natural frequency of the output filter are

$$\zeta = \frac{1}{2R\sqrt{(C_o/L_o)}} \tag{6.34}$$

and

$$\omega_o = \frac{1}{\sqrt{L_o C_o}}. \tag{6.35}$$

The magnitude and phase can be evaluated at any ω using Equations (6.36) and (6.37), respectively:

$$20\log|G(\omega)| = -10\log\left(\left(1-\left(\frac{\omega}{\omega_o}\right)^2\right)^2 + 4\left(\zeta\frac{\omega}{\omega_o}\right)^2\right), \tag{6.36}$$

$$\Phi(\omega) = -\tan^{-1}\left(\frac{2\zeta(\omega/\omega_o)}{1-(\omega/\omega_o)^2}\right). \tag{6.37}$$

Figure 6.11 and Figure 6.12 show the magnitude and phase responses versus normalized frequency (i.e., (f/f_o)) of the output filter for several values of the output resistance R_o. The magnitude response has a constant value up to the natural frequency f_o of the output filter. It then decreases linearly with a slope of -40 dB/decade. As shown, the magnitude response is critically damped when the output resistance, R_o, is equal to the characteristic impedance $\sqrt{(L_o/C_o)}$ of the output filter. The response is underdamped whenever $R_o > \sqrt{(L_o/C_o)}$ and it is overdamped whenever $R_o < \sqrt{(L_o/C_o)}$. The phase transition becomes sharper as the response becomes more underdamped. The rapid phase shift with frequency is to be avoided in the second-order system, since this may lead to instability.

In a practical switching converter, the equivalent-series-resistance (ESR) in the output capacitor must be taken into account in feedback compensation. Figure 6.13 shows the equivalent circuit of the output filter when considering the capacitor ESR. The corresponding transfer function of the output filter of the buck converter is

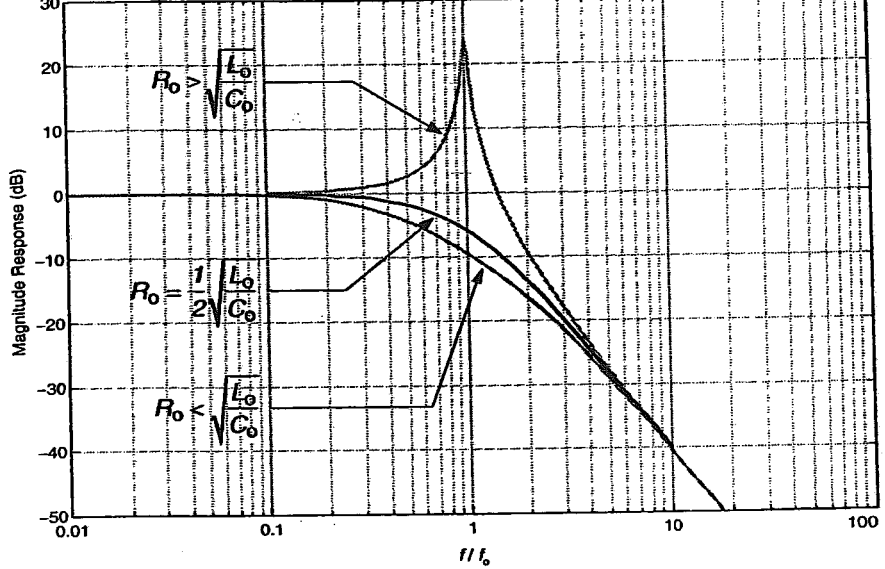

Figure 6.11 Magnitude response of the output filter for several values of the output resistance R_o.

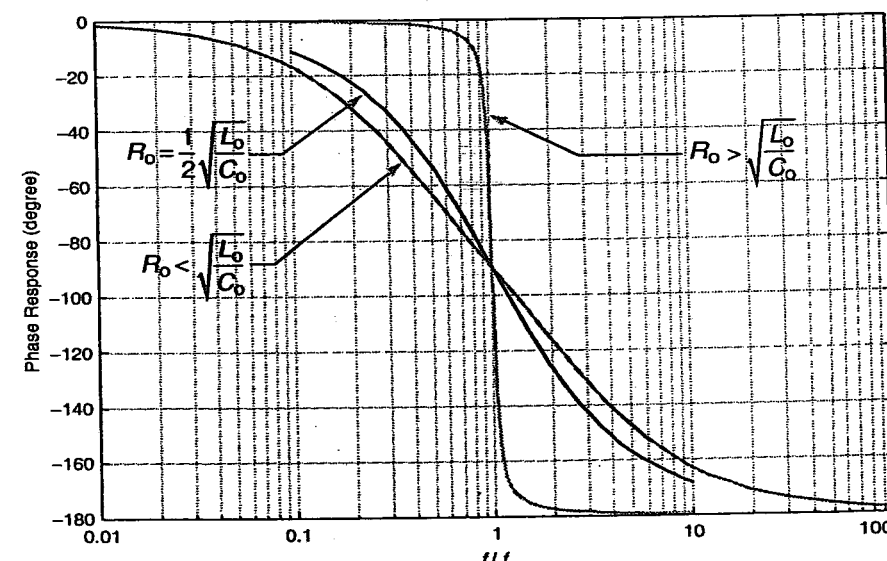

Figure 6.12 Phase response of the output filter for several values of the output resistance R_o.

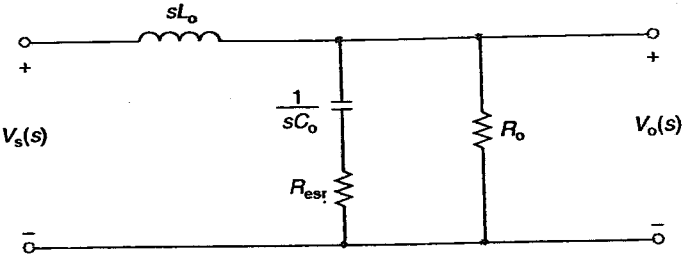

Figure 6.13 Output filter with a capacitor R_{esr}.

$$H(s) = \frac{R_o R_{esr}}{L_o(R_o + R_{esr})} \frac{s + (1/C_o R_{esr})}{s^2 + ((L_o + C_o R_o R_{esr})/L_o C_o (R_o + R_{esr}))s + (R_o/L_o C_o (R_o + R_{esr}))} \quad (6.38)$$

Thus, the capacitor ESR, R_{esr}, introduces a zero at $f_{ESR} = (1/2\pi R_{esr} C_o)$, when the capacitive impedance is equal to R_{esr}. The magnitude response of the output filter is modified by the presence of the ESR in the output capacitor, as shown in Figure 6.14. Figure 6.15 shows the phase response of the output filter as a function of R_o. The magnitude response before the f_{ESR} is unaffected. Beyond f_{ESR}, the magnitude response decreases linearly at a slope equal to −20 dB/decade. This is because after f_{ESR}, the impedance contribution from the output capacitor C_o is increasingly small compared to R_{esr}. As such, the output filter is now an RL rather than a LC circuit. The effect of the ESR in the output capacitor is to contribute with a phase angle equal to $\tan^{-1}(f/f_{ESR})$. Hence, the *phase lag* of the output filter considering the capacitor ESR at any given frequency f is

$$\theta_{LC} = \tan^{-1}\left(\frac{2\zeta(f/f_o)}{(1-(f/f_o))}\right) - \tan^{-1}\left(\frac{f}{f_{ESR}}\right). \quad (6.39)$$

While the magnitude response is

$$20\log|G(\omega)| = 10\log(1+\omega^2\tau^2) - 10\log\left(\left(1-\left(\frac{\omega}{\omega_o}\right)^2\right)^2 + 4\left(\zeta\frac{\omega}{\omega_o}\right)^2\right), \quad (6.40)$$

where

$$\omega_o = \sqrt{\frac{R_o}{L_o C_o (R_o + R_{esr})}}, \quad (6.41)$$

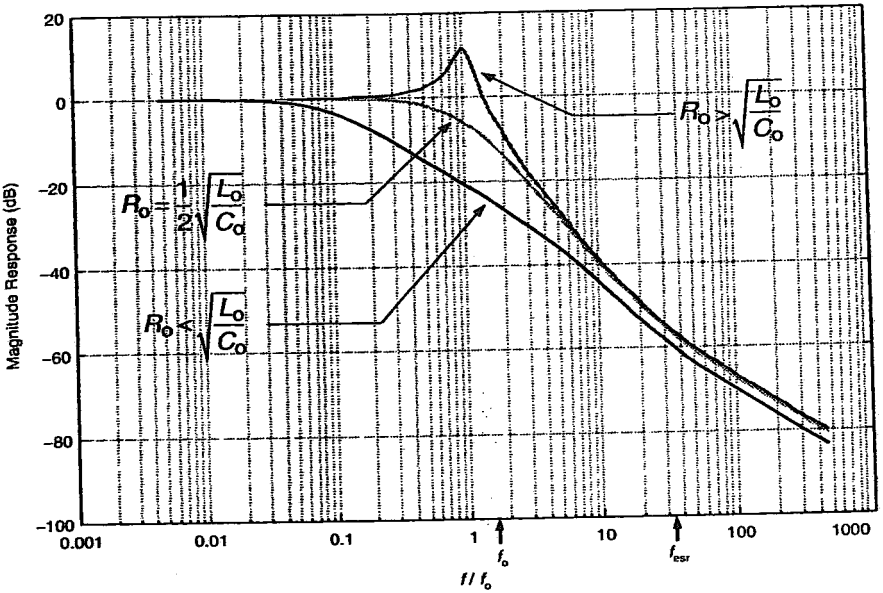

Figure 6.14 Magnitude response of an output filter with a capacitor having a R_{esr} for several values of the output resistance R_o.

$$\zeta = \left(\frac{L_o}{R_o} + C_o R_{esr}\right)\frac{\omega_o}{2}, \tag{6.42}$$

$$\tau = C_o R_{esr}. \tag{6.43}$$

Example 6.2. The output filter of a buck converter shown in Figure (6.10) has an inductor of 1 mH and a capacitor of 100 μF. Determine: (a) the corner frequency and (b) the load resistance R_o for a critically damped output response.

Solution.

(a) The corner frequency of the output filter is

$$f_o = \frac{1}{2\pi\sqrt{L_o C_o}} = \frac{1}{2\pi\sqrt{10^{-3}(100 \times 10^{-6})}} = 503.3\,\text{Hz}.$$

(b) For a critically damped output response, the load resistance is

$$R_o = \frac{1}{2}\sqrt{\frac{L_o}{C_o}} = \frac{1}{2}\sqrt{\frac{10^{-3}}{100 \times 10^{-6}}} = 1.58\,\Omega.$$

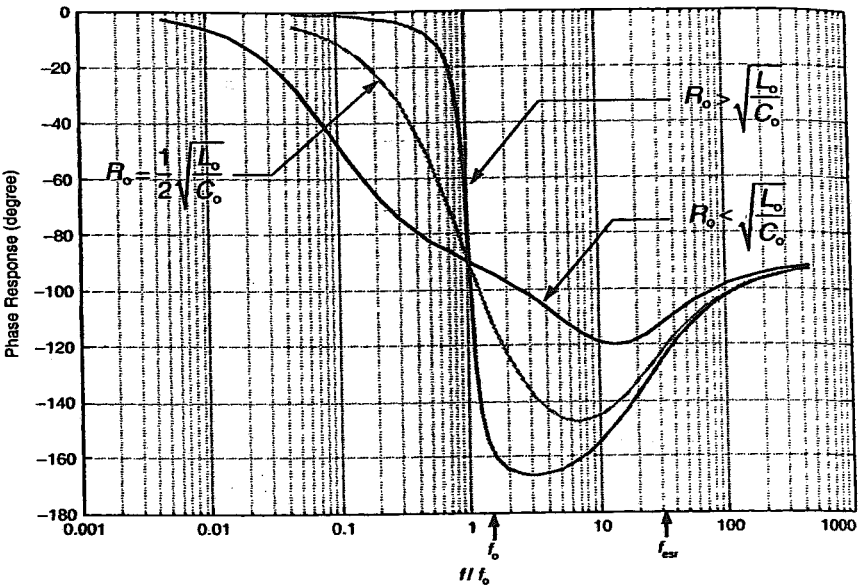

Figure 6.15 Phase response of an output filter with a capacitor having a R_{esr} for several values of the output resistance R_o.

Example 6.3. The output filter of the buck converter shown in Figure 6.13 has a capacitance of 200 μF with an equivalent series resistance of 0.1 Ω, an output inductor of 1 mH and a load resistor of 10 Ω, respectively. Determine (a) the corner frequency and (b) the zero introduced by the R_{esr}.

Solution.

(a) The corner frequency of the output filter is

$$f_o = \frac{1}{2\pi\sqrt{L_o C_o}} = \frac{1}{2\pi\sqrt{10^{-3}(200 \times 10^{-6})}} = 355.9\,\text{Hz}.$$

(b) The zero introduced by the R_{esr} is

$$f_{ESR} = \frac{1}{2\pi C_o R_{esr}} = \frac{1}{2\pi(200 \times 10^{-6})0.1} = 7.96\,\text{kHz}.$$

Example 6.4. The boost converter shown in Figure 2.10 has the following parameters: $V_{in} = 10\,\text{V}$, $V_o = 20\,\text{V}$, $f_s = 1\,\text{kHz}$, $L = 10\,\text{mH}$, $C = 100\,\mu\text{F}$, and $R_L = 20\,\Omega$. The reference voltage is 5 V. The converter operates in

the continuous-conduction mode under the voltage-mode. Using (a) the averaged-switch model, calculate the output-to-control transfer function and (b) MATLAB®, draw the Bode plot of the transfer function found in (a).

Solution.

(a) The nominal duty cycle can be calculated as

$$\frac{V_o}{V_d} = \frac{1}{1-D} \Rightarrow 1 - D = \frac{V_d}{V_o} \Rightarrow D = 1 - \frac{V_d}{V_o}$$

for the given input and output voltages, we have $D = 0.5$.

The averaged-switch model of the boost converter is shown in Figure 6.16, where the switching devices have been replaced by their averaged model. The parameters for the averaged model are

$$I_c = -(1-D)I_o = -(1-D)\frac{V_o}{R_o} \text{ and } V_{ap} = -V_o.$$

The small-signal gain, $(\hat{v}_o/\hat{d})$, can be calculated using linear circuit analysis. The two mesh equations that include the transformer are

$$\begin{cases} \hat{v}_o + v_2 - i_2 sL = 0 \\ \hat{v}_o + v_1 - \frac{V_{ap}}{D}\hat{d} = 0. \end{cases}$$

Solving for v_1 yields:

$$v_1 = \frac{V_{ap}\hat{d}}{D} - \hat{v}_o.$$

Thus,

$$\hat{v}_o + D\left(\frac{V_{ap}\hat{d}}{D} - \hat{v}_o\right) - i_2 sL = 0.$$

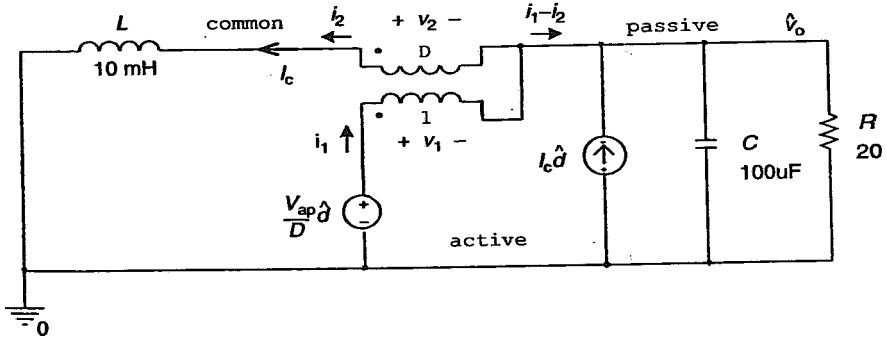

Figure 6.16 Small-signal model of the boost converter.

The current i_2 is given by:

$$i_2 = \frac{\hat{v}_o + V_{ap}\hat{d} - D\hat{v}_o}{sL}.$$

The currents i_1 and i_2 are related by the transformer ratio by

$$i_1 = Di_2,\ i_2 = \frac{i_1}{D}.$$

Then,

$$i_1 - i_2 = i_1 - \frac{i_1}{D} = i_1\left(1 - \frac{1}{D}\right) = i_1\left(\frac{D-1}{D}\right).$$

The current flowing out of the passive terminal is given by

$$i_p = i_1 - i_2 + I_c\hat{d} = i_1\left(\frac{D-1}{D}\right) + I_c\hat{d} = Di_2\left(\frac{D-1}{D}\right) + I_c\hat{d}$$

or

$$i_p = (D-1)\frac{\hat{v}_o + V_{ap}\hat{d} - D\hat{v}_o}{sL} + I_c\hat{d}.$$

The output voltage can be found:

$$\hat{v}_o = i_p\left(\frac{R/sC}{R + (1/sC)}\right) = \left[(D-1)\frac{\hat{v}_o + V_{ap}\hat{d} - D\hat{v}_o}{sL} + I_c\hat{d}\right]\left(\frac{R/sC}{R + (1/sC)}\right)$$

Replacing i_p, the output voltage becomes

$$\hat{v}_o = \left[\frac{(D-1)\hat{v}_o}{sL} + \frac{V_{ap}\hat{d}(D-1)}{sL} - \frac{(D-1)D\hat{v}_o}{sL} + I_c\hat{d}\right]\frac{R}{sCR+1}.$$

Rearranging

$$\hat{v}_o\left[\frac{sCR+1}{R} + \frac{(1-D)}{sL} - \frac{D(1-D)}{sL}\right] = \hat{d}\left[\frac{V_{ap}(D-1)}{sL} + I_c\right].$$

Solving for the output-to-control transfer function, yields:

$$\frac{\hat{v}_o}{\hat{d}} = \frac{((V_{ap}(D-1) + I_c sL)/sL)}{((sCR+1)/R) + ((1-D)/sL) - ((D(1-D))/sL)}$$
$$= \frac{V_{ap}(D-1) + sLI_c}{s^2LC + (sL/R) + (1-D) - D(1-D)}$$
$$= \frac{V_{ap}(D-1) + sLI_c}{s^2LC + s(L/R) + (1-D)^2}.$$

Finally, we have

$$\frac{\hat{v}_o}{\hat{d}} = \frac{V_{ap}(D-1) + sLI_c}{(1-D)^2\left[s^2\left(LC/(1-D)^2\right) + s\left(L/\left(R(1-D)^2\right)\right) + 1\right]}.$$

The natural frequency and the damping factor are

$$\frac{1}{\omega_m^2} = \frac{LC}{(1-D)^2} \Rightarrow \omega_m = \frac{(1-D)}{\sqrt{LC}},$$
$$\frac{2\xi}{\omega_m} = \frac{L}{R(1-D)^2} \Rightarrow \xi = \frac{\omega_m}{2}\frac{L}{R(1-D)^2} = \frac{(1-D)}{\sqrt{LC}}\frac{L}{2R(1-D)^2} \Rightarrow \xi = \sqrt{\frac{L}{C}}\frac{1}{2R(1-D)}.$$

The PWM modulator gain ($\hat{d}/\hat{v}_c$) can be calculated by using Equation (6.3)

$$\frac{\hat{d}}{\hat{v}_c} = \frac{1}{V_p}.$$

The amplitude of the sawtooth signal of the PWM modulator, V_p, is

$$\frac{V_p}{1} = \frac{V_c}{D} \Rightarrow V_p = \frac{V_{ref}}{D} = 10\,\text{V}.$$

(b) The following MATLAB program evaluates the parameters of the model and draws the Bode plot.

```
% Boost example
L=10 e-3;
C=100 e-6;
Vd=10
Vo=20
```

```
fs=1000
Ro=20
Vref=5
D=1 - (Vd/Vo)
Vp=Vref/D
Vap=-Vo
Ic=- (1 - D)*Vo/Ro
num=[L* Ic Vap*(D - 1)]
den=[L*C/power((1 - D),2) L/(Ro *power((1 - D),2)) 1]
k=1/(Vp* power((1 - D),2))
sys1=k*tf(num,den)
bode(sys1)
```

As shown in Figure 6.17, the boost converter behaves as a second-order system, with an additional right-half plane zero at a frequency near 300 Hz.

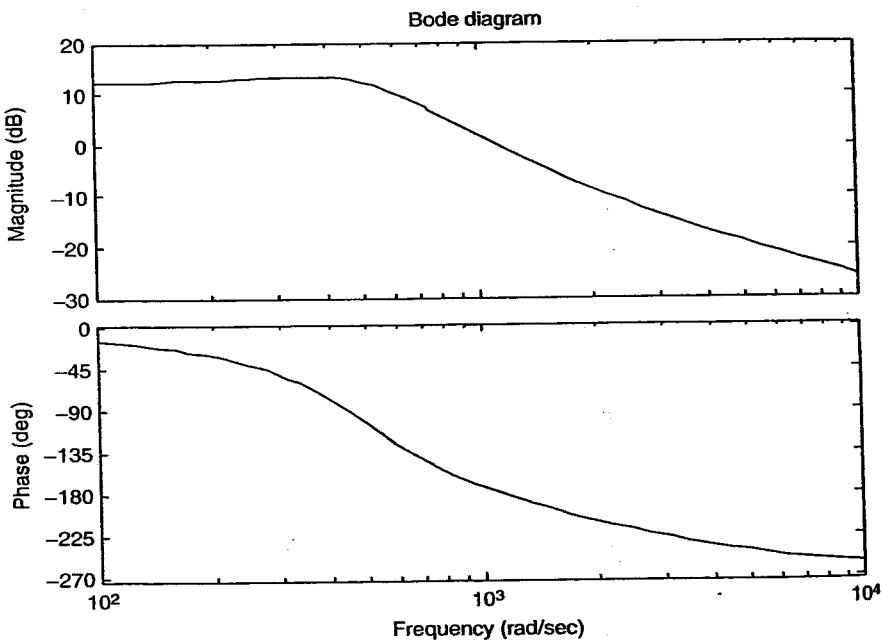

Figure 6.17 Bode plot of the small-signal transfer function of the boost converter.

6.2.2 Summary of Small-Signal Models of Switching Converters

Table 6.1 to Table 6.5 summarize the small-signal models of the basic switching converter topologies, operating in the current and voltage modes and in the continuous- and discontinuous-conduction modes. The tables are compiled from several sources [5,10–14]. The models were obtained using the averaged models described in Section 6.2.1. It can be seen that depending on the mode of operation, the conversion ratio of a linear converter may become nonlinear and vice versa. Also, the order of the transfer function of the switching converter is reduced by one order when operating either in the current mode or in the discontinuous mode. In addition to the left half-plane zero introduced by R_{esr}, some topologies (e.g., boost, flyback) have a right half-plane zero that causes a nonminimal phase response. This is an unwanted phenomenon in voltage regulators because any output voltage variation becomes larger before the controller can correct it (see Table 6.1 to Table 6.5 for the notations).

6.2.3 Review of Negative Feedback Using Classical-Control Techniques

6.2.3.1 Closed-Loop Gain

Figure 6.18 displays a block diagram representation of a closed-loop system. The feedback network, β, produces a voltage, V_f, which is a sample

Table 6.1 List of Symbols Used in the Models

Symbol	Definition
f_s	Switching frequency
R	Output load resistance
R_{esr}	Output capacitor's ESR
C	Output capacitor
V_i	Input voltage
V_o	Output voltage
L	Filter inductor
D	Duty cycle
V_c	Control voltage
k	$I_{peak,max}/V_{c,max}$
I_{peak}	kV_c
M	V_{out}/V_i Conversion ratio
L_{sec}	Secondary transformer inductor $= L_pN^2$
$1: N = N_p: N_s$	Transformer ratio

Table 6.2 Small-Signal Model of the Buck Converter

	Continuous conduction	Discontinuous conduction
Buck voltage mode		
Frequency of the first-order pole	—	$\frac{2-M}{2\pi(1-M)RC}$
Frequency of the second-order pole	$\frac{1}{2\pi\sqrt{LC}}$	None because of DCM
Frequency of the left half-plane zero	$\frac{1}{2\pi R_{esr}C}$	$\frac{1}{2\pi R_{esr}C}$
Frequency of the right half-plane zero	—	—
V_o/V_i DC gain	D	$\frac{2}{1+\sqrt{1+(8(L/R)T/D^2)}}$
V_o/V_e DC gain	V_i	$\frac{\sqrt{V_i(V_i-V_o)}}{\sqrt{2(L/R)T}}$
Buck current mode		
Frequency of the first-order pole	$\frac{1}{2\pi RC}$	$\frac{2-M}{2\pi(1-M)RC}$
Frequency of the second-order pole	None because of CM	None because of DCM
Frequency of the left half-plane zero	$\frac{1}{2\pi R_{esr}C}$	$\frac{1}{2\pi R_{esr}C}$
Frequency of the right half-plane zero	—	—
V_o/V_i DC gain	D	See Ref. [14]
V_o/V_e DC gain	kR	See Ref. [14]

of V_o. The error signal, $V_e = V_{ref} - V_f$, is multiplied by the plant transfer function, $A(s)$, to obtain the output voltage, V_o.

The closed-loop transfer function can be derived as

$$\frac{V_o}{V_{ref}} = \frac{A}{1+\beta A}. \tag{6.44}$$

Table 6.3 Small-Signal Model of the Boost Converter

	Continuous conduction	Discontinuous conduction
Boost voltage-mode		
Frequency of the first-order pole		$\dfrac{2+\left(1/\sqrt{1+(4D^2/(2Lf_s/R))}\right)}{2\pi RC}$
Frequency of the second-order pole	$\dfrac{(1-D)}{2\pi\sqrt{LC}}$	High frequency
Frequency of the left half-plane zero	$\dfrac{1}{2\pi R_{esr}C}$	$\dfrac{1}{2\pi R_{esr}C}$
Frequency of the right half-plane zero	$\dfrac{(1-D)^2R}{2\pi L}$	High frequency
V_o/V_i DC gain	$\dfrac{1}{(1-D)}$	$\dfrac{1+\sqrt{1+(2D^2R/Lf_s)}}{2}$
V_o/V_e DC gain	$\dfrac{V_o^2}{V_i}$	$\dfrac{V_i}{\sqrt{(2Lf_s/R)}}\dfrac{\sqrt{1-(V_i/V_o)}}{1-(V_i/2V_o)}$
Boost current-mode		
Frequency of the first-order pole	$\dfrac{1}{\pi RC}$	$\dfrac{2+\dfrac{1}{\sqrt{1+\dfrac{4D^2}{(2Lf_s/R)}}}}{2\pi RC}$
Frequency of the second-order pole	None	High frequency
Frequency of the left half-plane zero	$\dfrac{1}{2\pi R_{esr}C}$	$\dfrac{1}{2\pi R_{esr}C}$
Frequency of the right half-plane zero	$\dfrac{(1-D)^2R}{2\pi L}$	High frequency
V_o/V_i DC gain	$\dfrac{1}{(1-D)}$	$\dfrac{2+\left(1/\sqrt{(1/4)+[kV_c/V_i]^2(1/(2Lf_s/R))}\right)}{RC}$
V_o/V_e DC gain	$\dfrac{k}{2}\dfrac{RV_i}{V_o}$	$\dfrac{k}{\sqrt{(2Lf_s/R)}}\dfrac{\sqrt{1-(V_i/V_o)}}{1-(V_i/2V_o)}$

The loop gain T_L is defined as follows:

$$T_L = \beta A. \tag{6.45}$$

Table 6.4 Small-Signal Model of the Buck–Boost Converter

	Continuous conduction	Discontinuous conduction
Buck–boost voltage mode		
Frequency of the first-order pole		$\frac{1}{\pi RC}$
Frequency of the second-order pole	$\frac{(1-D)}{2\pi\sqrt{LC}}$	High frequency
Frequency of the left half-plane zero	$\frac{1}{2\pi R_{esr}C}$	$\frac{1}{2\pi R_{esr}C}$
Frequency of the right half-plane zero	$\frac{R(1-D)^2}{2\pi LD}$	High frequency
V_o/V_i DC gain	$\frac{D}{(1-D)}$	$D\sqrt{\frac{R}{2Lf_s}}$
V_o/V_e DC gain	$\frac{V_i}{(1-D)^2}$	$V_i\sqrt{\frac{R}{2Lf_s}}$
Buck–boost current mode		
Frequency of the first-order pole		$\frac{1}{\pi RC}$
Frequency of the second-order pole	$\frac{(1+D)}{2\pi RC}$	High frequency
Frequency of the left half-plane zero	$\frac{1}{2\pi R_{esr}C}$	$\frac{1}{2\pi R_{esr}C}$
Frequency of the right half-plane zero	$\frac{R(1-D)^2}{2\pi LD}$	High frequency
V_o/V_i DC gain	$\frac{D}{(1-D)}$	$kV_c\sqrt{\frac{RLf_s}{2}}$
V_o/V_e DC gain	$kR\frac{V_i}{2V_o+V_i}$	$k\sqrt{\frac{RLf_s}{2}}$

For $T_L \gg 1$, the closed-loop gain becomes independent of the gain A, and depends only on the feedback network. Therefore,

$$\frac{V_o}{V_{ref}} = \frac{1}{\beta}. \tag{6.46}$$

Table 6.5 Small-Signal Model of the Flyback Converter

	Continuous conduction	Discontinuous conduction
Flyback voltage mode		
Frequency of the first-order pole		$\frac{1}{\pi RC}$
Frequency of the second-order pole	$\frac{(1-D)}{2\pi\sqrt{L_{sec}C}}$	High frequency
Frequency of the left half-plane zero	$\frac{1}{2\pi R_{esr}C}$	$\frac{1}{2\pi R_{esr}C}$
Frequency of the right half-plane zero	$\frac{R(1-D)^2}{2\pi L_{sec}D}$	High frequency
V_o/V_i DC gain	$\frac{D}{(1-D)}N$	$ND\sqrt{\frac{R}{2L_{sec}f_s}}$
V_o/V_e DC gain	$\frac{V_i}{(1-D)^2}N$	$V_iN\sqrt{\frac{R}{2L_{sec}f_s}}$
Flyback current mode		
Frequency of the first-order pole		$\frac{1}{\pi RC}$
Frequency of the second-order pole	$\frac{(1-D)}{2\pi\sqrt{L_{sec}C}}$	High frequency
Frequency of the left half-plane zero	$\frac{1}{2\pi R_{esr}C}$	$\frac{1}{2\pi R_{esr}C}$
Frequency of the right half-plane zero	$\frac{R(1-D)^2}{2\pi L_{sec}D}$	High frequency
V_o/V_i DC gain	$\frac{D}{(1-D)}N$	$ND\sqrt{\frac{R}{2L_{sec}f_s}}$
V_o/V_e DC gain	$\frac{kR}{N}\frac{V_i}{2V_o+V_i}$	$\frac{k}{N}\sqrt{\frac{RL_{sec}f_s}{2}}$

If the feedback network is made with precision components, then V_o is proportional to V_{ref}. This is usually the goal in designing a closed-loop switching converter.

6.2.3.2 *Stability Analysis*

A system becomes unstable when the denominator of its transfer function is zero. In this case, at least one of its poles lies on the imaginary axis. This situation implies that

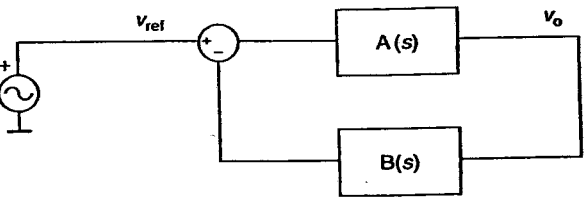

Figure 6.18 Block diagram representation for a closed-loop system.

$$\beta A = -1 \text{ or } \begin{cases} |\beta A| = 1 \\ \text{phase}(\beta) + \text{phase}(A) = 180°. \end{cases} \tag{6.47}$$

6.2.3.2.1 Relative stability. The relative stability is a measure of how far the system is from instability. The relative stability of a feedback system can be inferred from its gain and phase margins. The *gain margin* is defined as the increment of the loop gain required to drive the feedback system into instability. This is the amount of the loop gain necessary to reach 0 dB when the phase shift of the loop gain differs −180° from the phase at DC.[1] The *phase margin* is defined as the phase shift necessary to reach −180°[2] when the loop gain is unity (or 0 dB), as shown in Figure 6.19. Both the gain margin and the phase margin must be positive for the system to be stable. To ensure a stable loop response of the switching converter, the usual practice is to design for a gain margin of at least 6 dB and a phase margin of about 45°. Under these conditions, a second-order system would have a critically damped step response.

6.2.3.2.2 Stability analysis using Bode plots. A Bode plot is a plot of the magnitude and phase versus frequency. It is a very convenient method of determining the stability of a switching converter. Consider the Bode plot of the three-pole system of Figure 6.20, where the amplitude and phase of the loop gain has been graphed. The loop gain crosses the horizontal axis at f_1 (i.e., the amplitude of the loop gain is 1 or 0 dB at frequency f_1). At this frequency, the phase of the loop gain is close to −270°, giving a negative phase margin. Thus, the system is unstable.

The gain margin of this system is determined at frequency f_p, where the phase of the loop gain is 180°. At this point, the magnitude of the loop gain is positive, and so is the gain margin. Since one of the two stability margins is negative, the system is unstable.

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[1] Assuming that the system has singularities at high frequencies only.
[2] From the phase at DC.

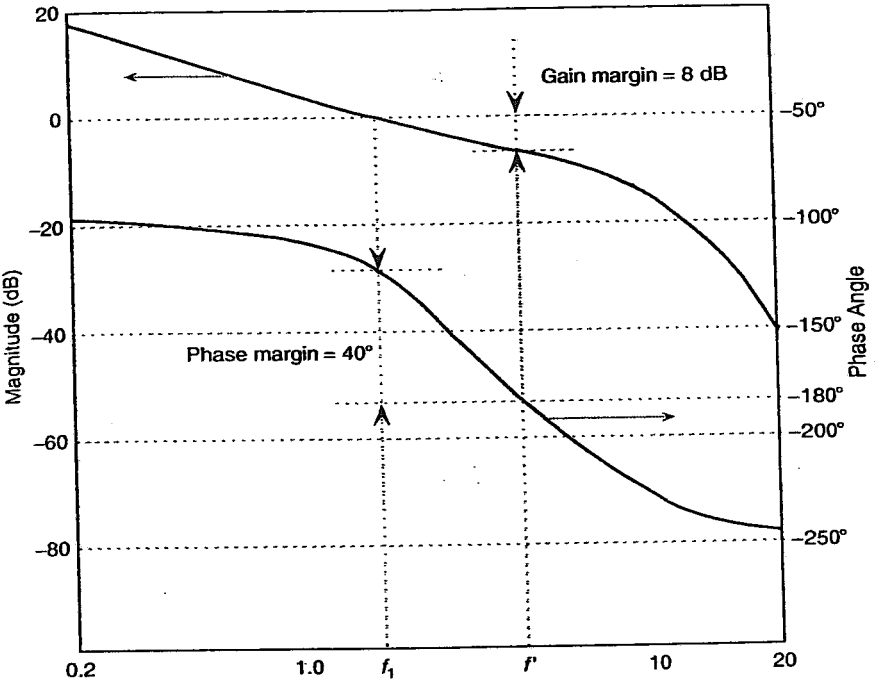

Figure 6.19 Definitions of gain and phase margins.

6.2.3.3 *Linear Model of the Closed-Loop Switching Converter*

A closed-loop model of the switching converter displayed in Figure 6.21 is analyzed next.

6.2.3.3.1 Feedback network. The feedback network is usually formed by a voltage divider (R_1 and R_2 in Figure 5.26). Then its transfer function is given by

$$V'_a = V_o \frac{R_2}{R_1 + R_2}. \tag{6.48}$$

6.2.3.3.2 Error amplifier compensation networks. When the loop is closed, the switching converter may become unstable or exhibit an undesirable transient response. The switching converter can be stabilized by addition of a compensator network in the error amplifier to increase the phase

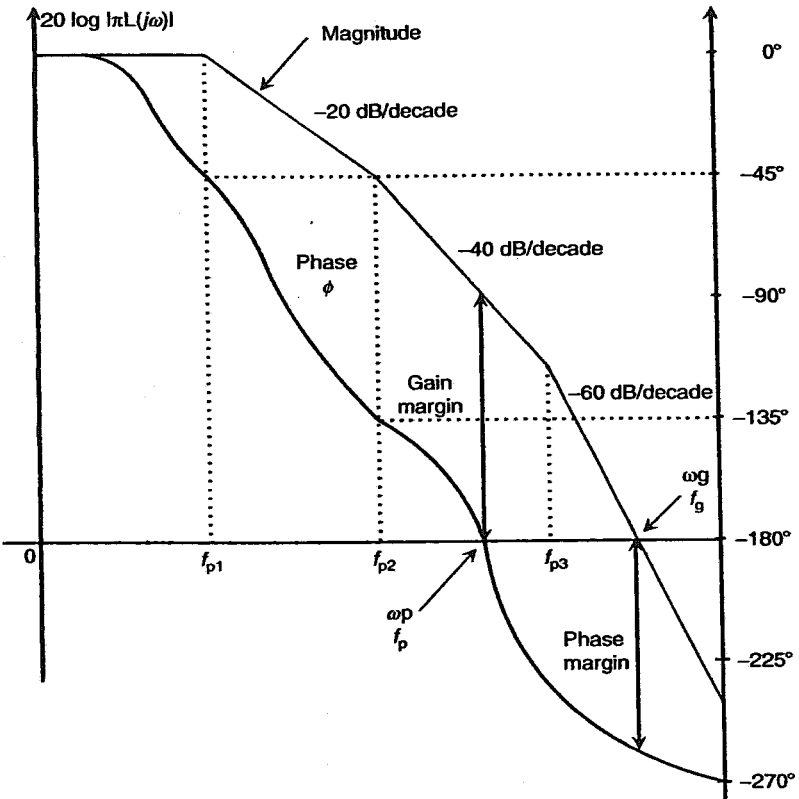

Figure 6.20 Loop gain of a system with three poles.

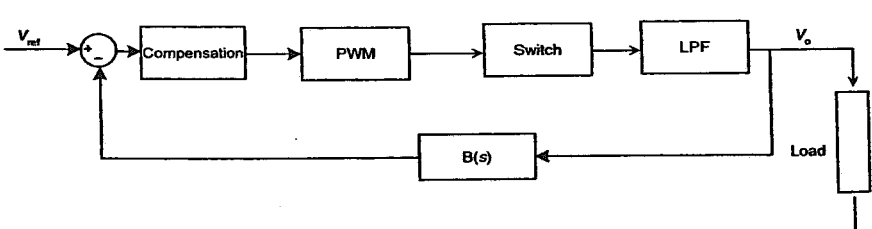

Figure 6.21 Closed-loop switching converter.

margin. At the same time, the compensator can also serve to shape the loop transfer function to achieve a desired transient response. The following subsections introduce the basic concept of frequency compensation for switching converters. A more detailed treatment of the feedback loop stabilization can be found in Pressman [15].

According to Nyquist sampling theory, the unity-gain crossover frequency, f_1, must be less than half the switching frequency to ensure system stability. The usual practice is to choose a unity-gain crossover frequency to be one-fourth to one-fifth of the switching frequency in order to reduce the switching ripple at the output of the switching converter [15]. The unity-gain crossover frequency should be high enough to allow the switching converter to respond quickly to its output transients [15]. Having set the unity-gain crossover frequency, the gain of the error amplifier is selected to yield a total loop gain of 0 dB at the unity-gain crossover frequency. The magnitude response of the error amplifier is designed to cross 0 dB at a slope equal to −20 dB/decade with the desired gain margin.

PI compensation network — There are many compensation networks for the error amplifier. Figure 6.22 shows a compensation network that consists of two capacitors and two resistors connected to the error amplifier in an inverting configuration to conform to a PI controller. The corresponding transfer function is

$$H(s) = \frac{(1/sC_2)(R_2 + (1/sC_1))}{R_1(R_2 + (1/sC_1) + (1/sC_2))}. \tag{6.49}$$

Since C_1 is generally much larger than C_2, the transfer function of Equation (6.49) can be simplified to

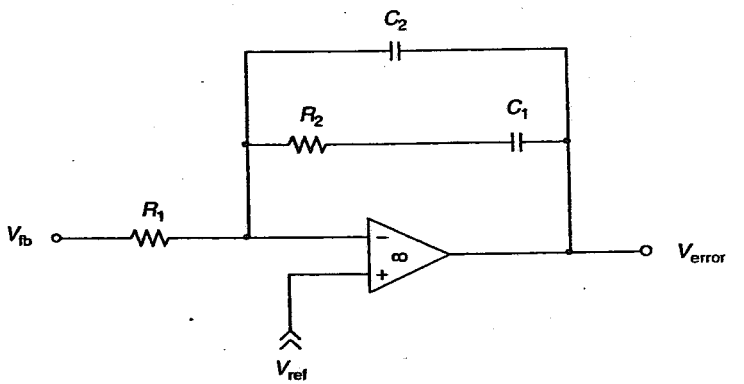

Figure 6.22 Compensation network with two poles and a zero.

$$H(s) = \frac{1 + sR_2C_1}{sR_1(C_1 + C_2 + sR_2C_1C_2)}. \tag{6.50}$$

The magnitude response of the compensation network is shown in Figure 6.23. It has two poles, one at the origin and the other at $f_p = 1/2\pi R_2C_2$. The zero of this compensation network is at $f_z = 1/2\pi R_2C_1$. The high-frequency pole serves to attenuate the high-frequency gain of the switching converter to reduce high-frequency switching noise. The low-frequency pole serves to maintain a sufficient gain at low frequencies in order to minimize the steady-state error in the average output voltage. The locations of the pole and zero define the component values of the compensation network. The phase response of the compensation network is shown in Figure 6.24. It starts at $-90°$ due to the pole at the origin. The low-frequency zero, f_z, causes a phase boost, while the high-frequency pole, f_p, introduces a phase lag and causes the phase response to approach $-90°$ again. This compensation network is used when the slope of the open-loop magnitude response of the switching converter at the unity-gain crossover frequency is -20 dB/decade, usually due to the contribution of the output capacitor ESR.

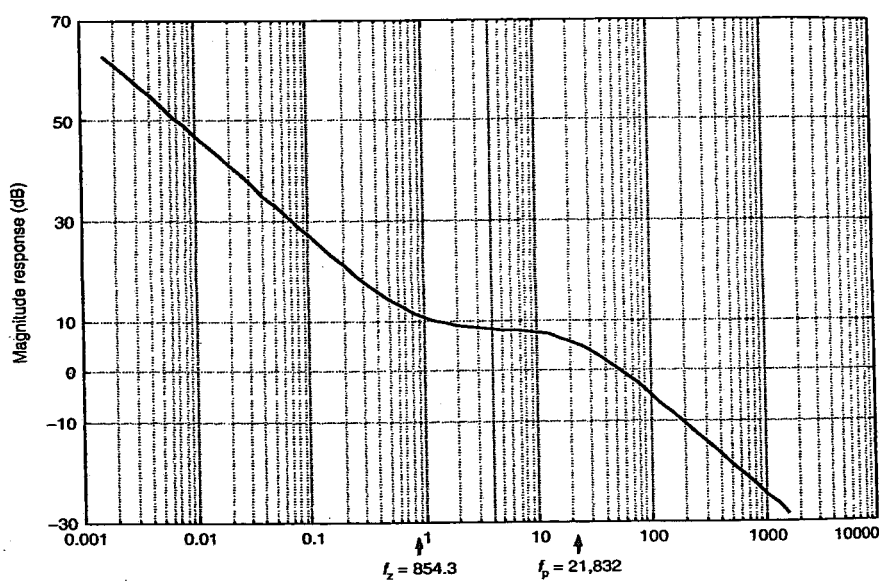

Figure 6.23 Frequency response of the compensation network shown in Figure 6.22.

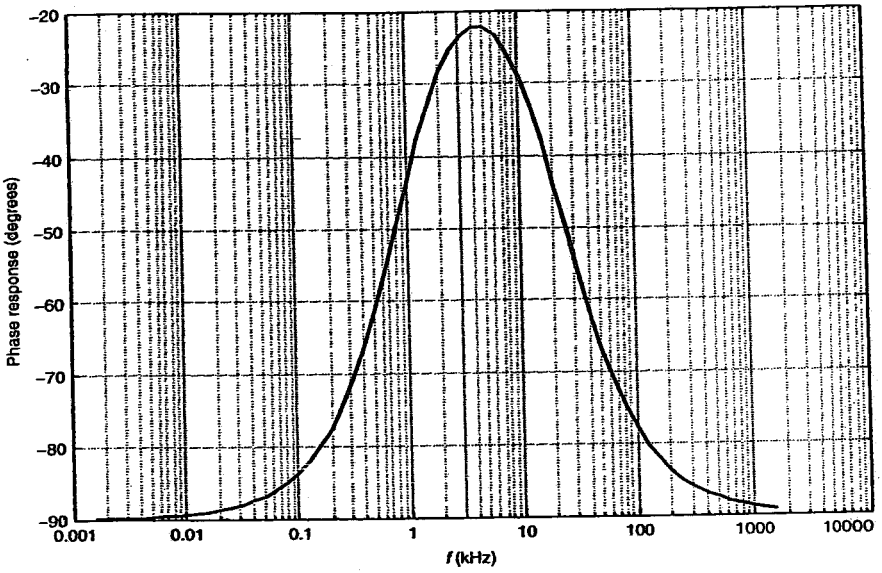

Figure 6.24 Phase response of the compensation network shown in Figure 6.22.

The zero introduces a phase lead while the pole introduces a phase lag. At the unity gain frequency, the phase lead due to the zero is

$$\theta_{\text{lead}} = \tan^{-1}\left(\frac{f_1}{f_z}\right) \tag{6.51}$$

while the phase lag due to the pole is

$$\theta_{\text{lag}} = \tan^{-1}\left(\frac{f_1}{f_p}\right). \tag{6.52}$$

The total phase lag introduced by the compensation network and the error amplifier at the unity-gain crossover frequency, f_1, is

$$\theta_{\text{lag}} = 270° - \tan^{-1}\left(\frac{f_1}{f_z}\right) + \tan^{-1}\left(\frac{f_1}{f_p}\right). \tag{6.53}$$

The 270° phase lag is due to phase inversion introduced by the inverting error amplifier (180°) and the pole at the origin introduced by the compensation network (90°). Thus, the locations of the pole and zero are chosen to yield the desired phase margin.

Proportional-integral-derivative (PID) compensation network — Figure 6.25 shows a 3-pole, 2-zero compensation network. This compensation is also known as PID because it provides terms, which are proportional, integral, and derivative of the error signal. The integration is provided by a third pole, located at zero, which is used to minimize the steady-state error. The transfer function for this compensation network is

$$H(j\omega) = \frac{(1 + j\omega R_2 C_1)}{-\omega^2 R_2 C_1 C_2 + j\omega(C_1 + C_2)} \frac{(1 + j\omega(R_1 + R_3)C_3)}{R_1 + j\omega R_1 R_3 C_3} \tag{6.54}$$

having one pole at zero and two high-frequency poles, one at $f_{p1} = 1/2\pi R_3 C_3$ and the other at $f_{p2} = (C_1 + C_2)/2\pi R_2 C_1 C_2$. The zeros are at $f_{z1} = 1/2\pi R_2 C_1$ and $f_{z2} = 1/2\pi(R_1 + R_3)C_3$, respectively. The two gains of the compensation network are $K_1 = R_2/R_1$ and $K_2 = R_2(R_1 + R_3)/R_1 R_3$, respectively. The asymptotic approximated magnitude response is shown in Figure 6.26. As shown, the low-frequency gain below f_{z1} decreases at a rate of −20 dB/decade due to the pole at the origin. The gain is constant between the two zero frequencies. After f_{z2}, the magnitude response starts to increase at a rate of +20 dB/decade until f_{p1}. It is flat again between f_{p1} and f_{p2}. After f_{p2}, the magnitude response decreases at a rate of −20 dB/decade. This compensation network is used primarily for a switching converter with no output capacitor ESR. The slope of the open-loop magnitude response at the unity-gain crossover frequency of such switching converter is −40 dB/decade. In order to yield a −20 dB/decade slope at the unity-gain crossover frequency, the magnitude response of the compensation network must have a slope of +20 dB/decade at the unity-gain crossover frequency. Thus, the unity-gain crossover frequency should occur between f_{z2} and f_{p1} where the magnitude response increases at a rate of +20 dB/decade. Figure 6.27 shows the magnitude response of the compensated network with $C_1 = 0.16\,\mu F$, $C_2 = 532\,pF$, $C_3 = 14.3\,nF$, $R_1 = 10\,k\Omega$, $R_2 = 10\,k\Omega$, and $R_3 = 1.1\,k\Omega$. The

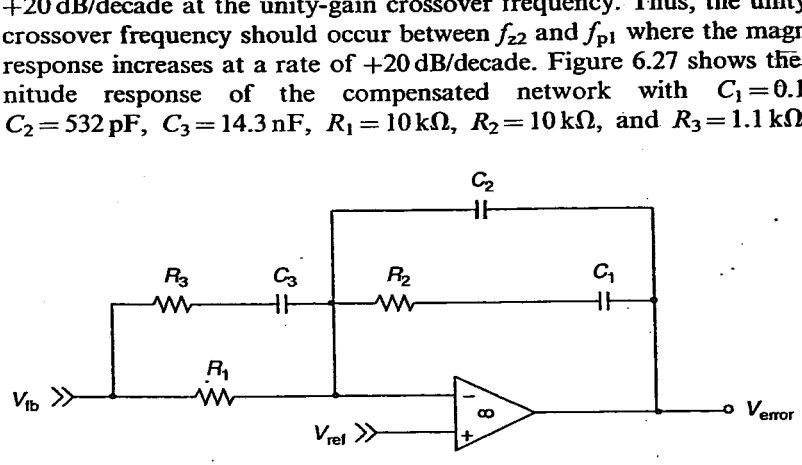

Figure 6.25 Compensation network with three poles and two zeroes.

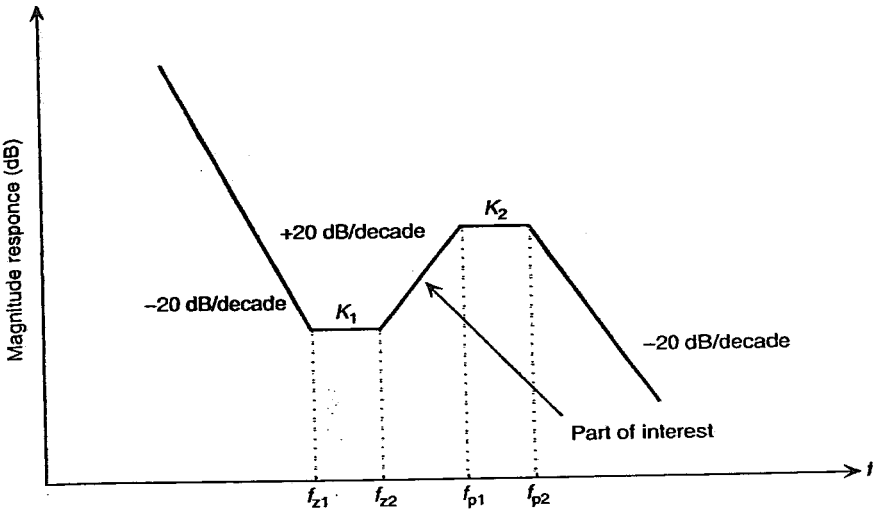

Figure 6.26 Asymptotic approximated magnitude response of the compensation network shown in Figure 6.25.

two zeros are at 100 Hz and 1 kHz, respectively. The two poles are at 10 and 25 kHz, respectively. It should be noted that the gains between the zeros and poles are not constant, as depicted in Figure 6.26. Figure 6.28 shows the phase response of the compensation network. As can be seen, a phase boost occurs between f_{z1} and f_{p2}. The wider the separation between the poles and zeros, the larger is the phase margin. As such, this compensation network yields a very good transient response.

To simplify the design process, the two zeros in the compensation network shown in Figure 6.25 are usually chosen to be equal to each other (i.e., $f_{z1}=f_{z2}=f_{zd}$) such that

$$\frac{1}{2\pi R_2 C_1}=\frac{1}{2\pi(R_1+R_3)C_3} \tag{6.55}$$

or

$$R_2C_1=(R_1+R_3)C_3. \tag{6.56}$$

The phase boost at the double zeros, θ_{zd}, is

$$\theta_{zd}=2\tan^{-1}\left(\frac{f_1}{f_{zd}}\right) \tag{6.57}$$

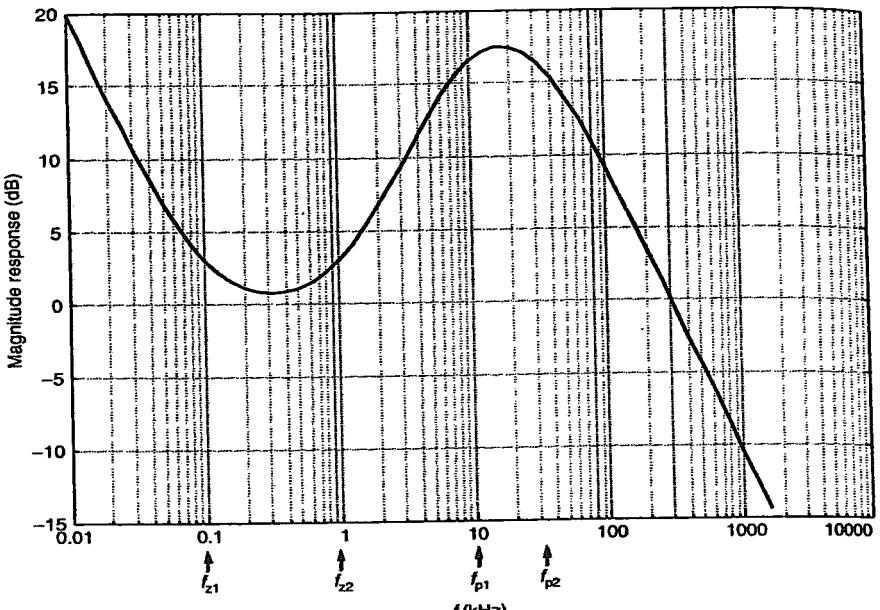

Figure 6.27 Frequency response of the compensation network shown in Figure 6.25.

since there are two zeros at f_{zd}. To simplify the design process, the two high-frequency poles are usually chosen to be equal to each other such that

$$\frac{1}{2\pi R_3 C_3} = \frac{(C_1 + C_2)}{2\pi R_2 C_1 C_2} \tag{6.58}$$

or

$$\frac{R_3}{R_2} C_3 = \frac{C_1 C_2}{C_1 + C_2}. \tag{6.59}$$

The asymptotic approximated magnitude response of the compensation network shown in Figure 6.25 with a 2-zero and 2-pole is displayed in Figure 6.29. The phase lag due to the double pole, θ_{pd}, is approximately

$$\theta_{pd} = 2\tan^{-1}\left(\frac{f_1}{f_{pd}}\right). \tag{6.60}$$

The total phase lag introduced by the compensation network and the error amplifier at the unity-gain crossover frequency is

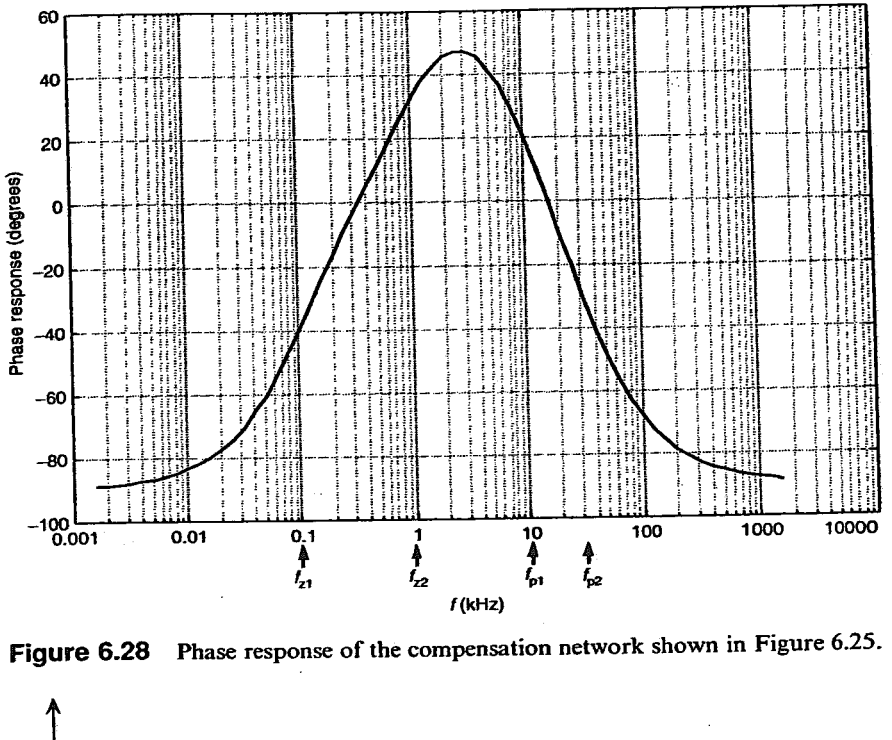

Figure 6.28 Phase response of the compensation network shown in Figure 6.25.

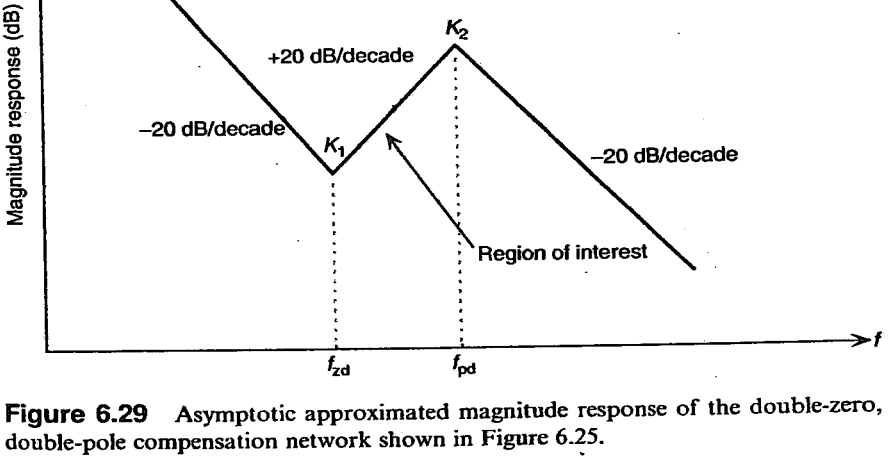

Figure 6.29 Asymptotic approximated magnitude response of the double-zero, double-pole compensation network shown in Figure 6.25.

$$\theta_{lag} = 270° - 2\tan^{-1}\left(\frac{f_1}{f_{zd}}\right) + 2\tan^{-1}\left(\frac{f_1}{f_{pd}}\right). \tag{6.61}$$

Again, the 270° phase lag is due to phase inversion introduced by the inverting amplifier and the pole at the origin of the compensation network.

Example 6.5. The compensation network shown in Figure 6.22 has the following component values: $C_1 = 6.8\,\text{nF}$, $C_2 = 270\,\text{pF}$, $R_1 = 10\,\text{k}\Omega$, and $R_2 = 27\,\text{k}\Omega$. Determine (a) the zero introduced by the compensation network, (b) the high-frequency pole introduced by the compensation network, and (c) the phase lag introduced by the compensation network at 5 kHz.

Solution.

(a) The zero frequency is

$$f_z = \frac{1}{2\pi R_2 C_1} = \frac{1}{2\pi(27 \times 10^3)6.8 \times 10^{-9}} = 854.3\,\text{Hz}.$$

(b) The pole frequency is

$$f_p = \frac{1}{2\pi R_2 C_2} = \frac{1}{2\pi(10 \times 10^3)270 \times 10^{-12}} = 21{,}832\,\text{Hz}.$$

(c) The phase lag contribution from the compensation network at 5 kHz is

$$90° + \tan^{-1}\left(\frac{f_1}{f_p}\right) - \tan^{-1}\left(\frac{f_1}{f_z}\right) = 22.59°.$$

6.2.4 Feedback Compensation in a Buck Converter with Output Capacitor ESR

A closed-loop buck converter is shown in Figure 6.30. In this converter, the average output voltage is specified to be 5 V with an input voltage of 12 V and a load resistance, R_L, of 5 Ω. The objective of the feedback compensation is to shape the closed-loop magnitude response of the switching converter to achieve a −20 dB/decade roll-off rate at the unity-gain crossover frequency with a sufficient phase margin for stability.

The sampling network, R_3 and R_4, contributes attenuation according to its sampling ratio of $R_4/(R_3 + R_4)$. Since the average output voltage of the buck converter is 5 V and the sampled voltage is chosen to be 2.5 V, the gain attenuation of the sampling network is $20[\log_{10}(2.5/5)] = -6\,\text{dB}$. The PWM modulator gain is the gain from the error amplifier output to the average

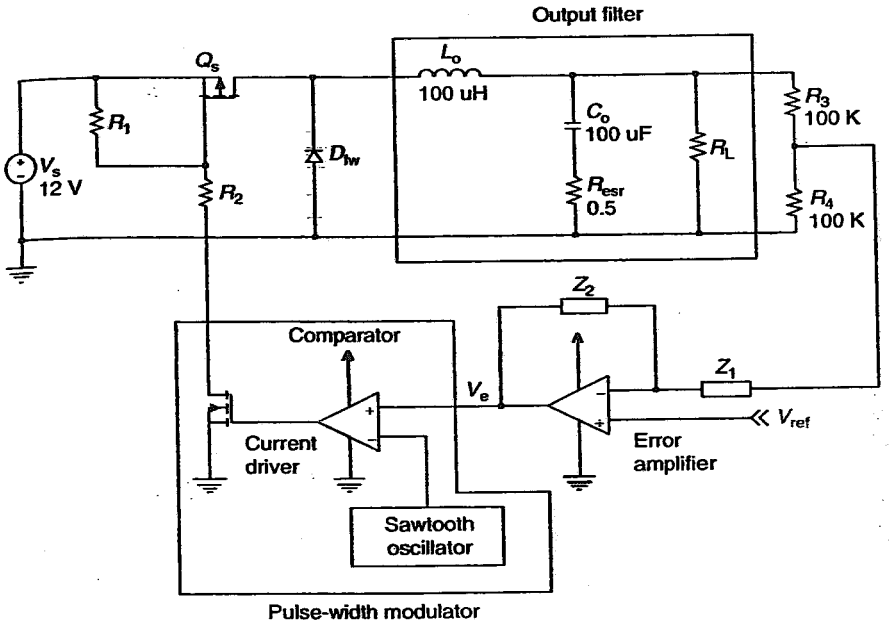

Figure 6.30 Circuit schematic of a closed-loop buck converter.

voltage at the input end of the output inductor. When the output of the error amplifier is at its peak value of 3.5 V, the duty cycle is 100% and the average voltage at the input end of the output inductor is 12 V. Thus, the PWM contributes a gain of $20\log_{10}(V_s/V_p)$ or 10.7 dB, where V_p is the peak amplitude of the sawtooth voltage (3.5 V). The low-frequency gain of the open-loop buck converter is +4.7 dB. The natural frequency of the output filter, f_o, is

$$f_o = \frac{\sqrt{R_o/L_oC_o(R_o + R_{esr})}}{2\pi} = \frac{\sqrt{5/(100 \times 10^{-6})(100 \times 10^{-6})(5 + 0.5)}}{2\pi}$$
$$= 1.517\,\text{kHz} \tag{6.62}$$

while the ESR break frequency, f_{ESR}, is

$$f_{ESR} = \frac{1}{2\pi(0.5)100 \times 10^{-6}} = 3.18\,\text{kHz}. \tag{6.63}$$

The unity-gain crossover frequency, f_1, is chosen to be one fifth of the switching frequency of 25 kHz (i.e., $f_1 = 5$ kHz). The loop magnitude

response of the uncompensated buck converter, excluding the compensation network and the error amplifier, is shown in Figure 6.31 as ABCD. From Figure 6.31, the attenuation at the unity-gain crossover frequency is −14.5 dB. Hence, the gain of the error amplifier should be chosen to be +14.5 dB so that the gain at the unity-gain crossover frequency is 0 dB. This is achieved by selecting the ratio R_2/R_1 such that a 14.5 dB gain is attained by the error amplifier. Thus, if R_1 is chosen to be 47 kΩ, then R_2 is about 250 kΩ. The locations of the pole and zero of the compensation network are then determined to yield the desired phase margin of 45°. The total phase shift at the unity-gain crossover frequency should be 360°−45° = 315°. Since the output filter contributes a phase lag of

$$\theta_{LC} = \tan^{-1}\left(\frac{2\zeta(f/f_o)}{1-(f/f_o)^2}\right) - \tan^{-1}\left(\frac{f}{f_{ESR}}\right) = 109.9°. \tag{6.64}$$

Then, the phase lag contribution from the compensation network and the error amplifier is

$$\theta_{ea} = 315° - 109.9° = 205.1° \tag{6.65}$$

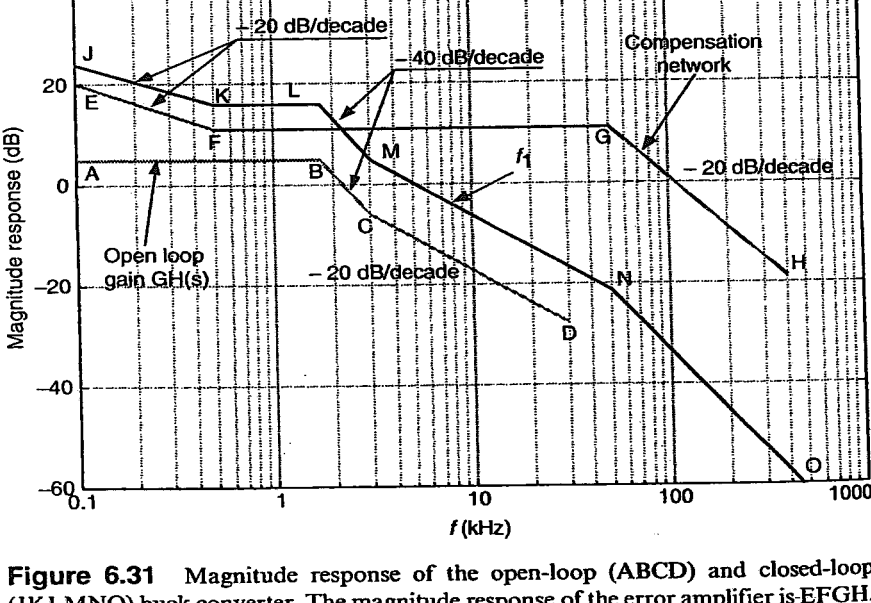

Figure 6.31 Magnitude response of the open-loop (ABCD) and closed-loop (JKLMNO) buck converter. The magnitude response of the error amplifier is EFGH.

From Equation (6.53), the phase lag contribution from the compensation network is thus

$$\tan^{-1}\left(\frac{5}{f_z}\right) - \tan^{-1}\left(\frac{5}{f_p}\right) = 64.9°. \tag{6.66}$$

Assuming that the pole and zero are equidistant from the unity-gain crossover frequency,[3] then

$$\tan^{-1} f'' - \tan^{-1}\left(\frac{1}{f''}\right) = 64.9°. \tag{6.67}$$

Solving iteratively for f'' yields a value of 4.5 to achieve a phase lag of 64.9°. Hence, the high-frequency pole should be located at 4.5 times the unity-gain crossover frequency, or 22.5 kHz, while the low-frequency zero should be located at 1/4.5 of the unity-gain crossover frequency or 1.11 kHz. The magnitude response of the error amplifier is shown in Figure 6.31 as EFGH. The components of the compensation network can be determined now. The capacitor C_1 is

$$C_1 = \frac{1}{2\pi R_2 f_z} = 573\,\text{pF} \tag{6.68}$$

and the capacitor C_2 is

$$C_2 = \frac{1}{2\pi R_2 f_p} = 28\,\text{pF}. \tag{6.69}$$

The overall loop magnitude response of the feedback compensated switching converter is shown in Figure 6.31 as JKLMNO. Notice that the loop gain at the unity-gain crossover frequency in the overall magnitude response of the feedback compensated switching converter is 0 dB. Above the high-frequency pole, f_p, the loop gain attenuates at −40 dB/decade. Thus high-frequency switching noise is suppressed. If high-frequency noise is a problem, then the location of the high-frequency pole can be made to be less at the expense of a more sluggish transient response. If f_p is chosen to be at 12.5 kHz, then f_z is 0.288 kHz according to Equation (6.66).

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[3] This is an approximation to simplify the calculations. An exact solution would satisfy magnitude and phase constraints simultaneously. The exact solution is used in the design examples of Chapters 9 and 10.

6.2.5 Feedback Compensation in a Buck Converter with no Output Capacitor ESR

The output ripple voltage of a buck converter depends largely on the magnitude of the ESR in the output capacitor. Thus, it is necessary to choose an output capacitor with a low ESR to reduce the output ripple voltage. A different compensation network from that considered in Section 6.2.4 must be employed, as the capacitor manufacturers strive to manufacture aluminum electrolytic capacitors with essentially zero ESR. Consider the buck converter shown in Figure 6.30 but with no output capacitor ESR. The corner frequency of the output filter, f_o, was found to be 1.59 kHz. Curve ABC in Figure 6.32 shows the magnitude response of the open-loop buck converter. The unity-gain crossover frequency is again chosen to be 5 kHz, which is one fifth of the switching frequency. Since the slope of the magnitude response at the unity-gain crossover frequency is −40 dB/decade, the compensation network shown in Figure 6.25 is chosen. From the open-loop magnitude response of the buck converter shown in curve ABC of Figure 6.32, the attenuation at the unity-gain crossover frequency is −16 dB. Hence, the gain of the error amplifier at the unity-gain crossover

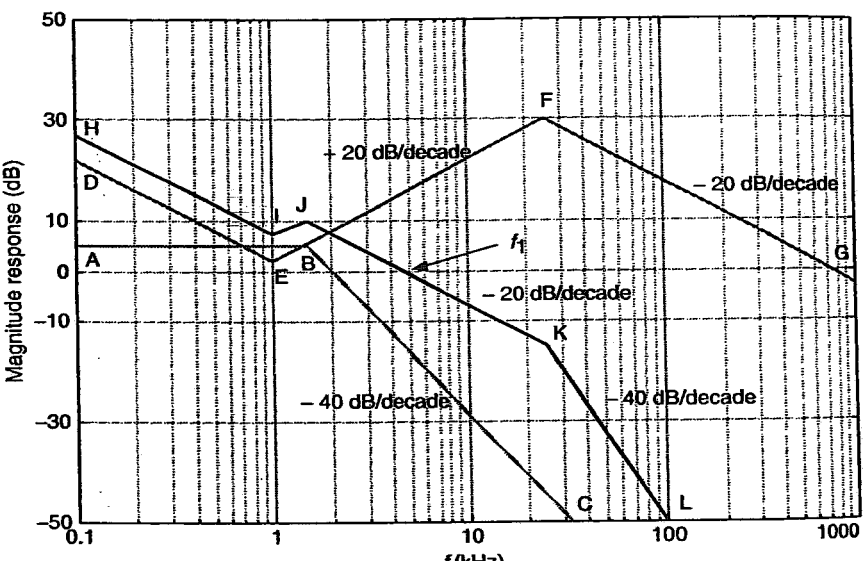


Figure 6.32 Magnitude response of the open-loop (ABC) and closed-loop (HIJKL) buck converter. The magnitude response of the error amplifier is DEFG.

frequency is chosen to be +16 dB in order to yield a 0 dB at the unity-gain crossover frequency.

The locations of the double-pole and double-zero of the compensation network are chosen to yield the desired phase margin of 45°. The total phase shift at the unity-gain crossover frequency is 360° − 45° or 315°. Since the output filter contributes a phase lag of approximately 180°, the allowable phase lag contribution from the compensation network and the error amplifier is 135°. Hence, from Equation (6.61), the phase lag contribution from the compensation network is

$$2\tan^{-1}\left(\frac{f_1}{f_{zd}}\right) - 2\tan^{-1}\left(\frac{f_1}{f_{pd}}\right) = 270° - 135° = 135°. \tag{6.70}$$

Assuming that the double-pole and double-zero are equidistant from the unity-gain crossover frequency, then

$$2\left[\tan^{-1} f'' - \tan^{-1}\left(\frac{1}{f''}\right)\right] = 135°. \tag{6.71}$$

Solving iteratively for f'' yields a value of 5 to achieve a phase lag of 135°. Hence, the high-frequency double-pole should be located at five times the unity-gain crossover frequency or 25 kHz, while the low-frequency double-zero should be located at one fifth of the unity-gain crossover frequency or 1 kHz. The magnitude response of the error amplifier is shown in Figure 6.32 as DEFG. The overall magnitude response of the feedback compensated switching converter is shown in Figure 6.32 as HIJKL. Notice that the gain at the unity-gain crossover frequency in the overall magnitude response of the feedback compensated switching converter is 0 dB with a slope of −20 dB/decade. There are six components to be selected for the compensation network. As shown in curve DEFG of Figure 6.32, the gain at the double-zero is 2 dB or 1.26. Assuming an R_1 value of 1000 Ω, then R_2 is 1260 Ω. The gain at the double-pole is measured to be 30 dB or 31.6 from curve DEFG in Figure 6.32. Assuming that $R_1 \gg R_3$, then R_3 is R_2/K_2 or 40 Ω. From $f_{p1} = f_{pd}$, the capacitance value for C_3 is

$$C_3 = \frac{1}{2\pi f_{pd} R_3} = 0.16\,\mu\text{F}. \tag{6.72}$$

From Equation (6.56), the capacitance value for C_1 is

$$C_1 = \frac{(R_1 + R_3)C_3}{R_2} = 0.13\,\mu\text{F}. \tag{6.73}$$

From Equation (6.59), the capacitance value for C_2 is

$$C_2 = \frac{C_1 C_3 (R_3/R_2)}{[C_1 - C_3(R_3/R_2)]} = 5.29\,\text{nF}. \tag{6.74}$$

In practice, commercially available component values are chosen for the capacitors and resistors. It is necessary to check the influence of the time delay on the phase margin. Assuming a time delay of 1 μs, from (6.30), the

$$\text{phase(delay)} = -360° \times 1\,\mu\text{s} \times 5\text{kHz} \tag{6.75}$$

phase(delay) $= -1.8°$ which is not significant in the phase margin.

6.2.6 Linear Model of the Voltage Regulator Including External Perturbances

In the linear model, the nominal load impedance can be modeled as a constant current source I_o at the output of the switching converter. Load variations are represented by a small-signal current source $\hat{i}_o$, as shown in Figure 6.33.

The perturbations of the output voltage may be expressed by the linear terms of its Taylor series expansion as

$$\hat{v}_o = G_{V_{ref}} \hat{v}_{ref} + G_{V_{DC}} \hat{v}_{DC} + G_{i_o} \hat{i}_o, \tag{6.76}$$

where

$$G_{V_{ref}} = \frac{\partial v_o}{\partial v_{ref}}\bigg|_{\substack{\hat{v}_{DC}=0 \\ \hat{i}_o=0}} = \frac{\hat{v}_o}{\hat{v}_{ref}}\bigg|_{\substack{\hat{v}_{DC}=0 \\ \hat{i}_o=0}}, \tag{6.77}$$

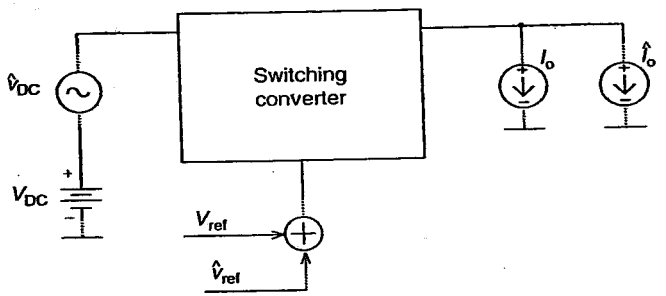


Figure 6.33 Linear model of a voltage regulator including external perturbances

where $G_{V_{ref}}$ is the sensitivity of the output voltage with respect to the reference voltage. There is usually a direct relationship between the output and the reference voltages, meaning that the voltage regulator will not be better than the reference itself. The audio susceptibility, defined as

$$G_{V_{DC}} = \frac{\partial v_o}{\partial v_{DC}}\bigg|_{\substack{\hat{v}_{ref}=0 \\ \hat{i}_o=0}} = \frac{\hat{v}_o}{\hat{v}_{DC}}\bigg|_{\substack{\hat{v}_{ref}=0 \\ \hat{i}_o=0}} \tag{6.78}$$

is a measure of the influence of the variations on the unregulated DC input voltage on the regulated output voltage. The most important variations on V_{DC} are due to fluctuation of the line voltage, the rectified ripple voltage, and voltage drop in the line source impedance. The audio susceptibility models the effects of the variations of the DC input voltage on the output voltage. Usually, V_{DC} is an unregulated voltage derived from a diode bridge and a capacitor filter; thus, it has the same voltage ripple at twice the line frequency (i.e., 100 or 120 Hz). It is desirable that (G_{VDC}) be much less than 1. $G_{V_{DC}}$ is equivalent to the PSSR of an OP AMP circuit.

The output impedance is defined as

$$G_{i_o} = \frac{\partial v_o}{\partial i_o}\bigg|_{\substack{\hat{v}_{ref}=0 \\ \hat{v}_{DC}=0}} = \frac{\hat{v}_o}{\hat{i}_o}\bigg|_{\substack{\hat{v}_{ref}=0 \\ \hat{v}_{DC}=0}} = Z_o. \tag{6.79}$$

It is desirable that the output impedance of the voltage regulator be much smaller than the load impedance. In addition, the bandwidth of the output impedance should be larger than the bandwidth of the load to ensure fast recovery from load transients.

6.2.7 Output Impedance and Stability

The current, I_o represents the nominal load and $\hat{i}_o$ is a source of perturbation to the voltage regulator of Figure 6.33. If $\hat{i}_o$ is a step function, the corresponding v_o is the system step response given by the transfer function, Z_o. The output voltage of a voltage regulator should be bounded within certain limits (e.g., 5 $\pm$ 0.1 V) to avoid damaging sensitive loads. Therefore, the step response should be overdamped or, at the most, critically damped. The phase margin of a second-order system corresponding to a critically damped step response is 45°; therefore, the phase margin for a voltage regulator must be greater than 45°.

According to feedback circuit analysis, the output impedance of the circuit of Figure 6.33 can be calculated as

$$Z_{of} = \frac{Z_{oo}}{1+\beta A}, \tag{6.80}$$

where Z_{oo} is the open-loop output impedance, including the load, calculated from Figure 6.34.

Z_{of} can also be expressed as

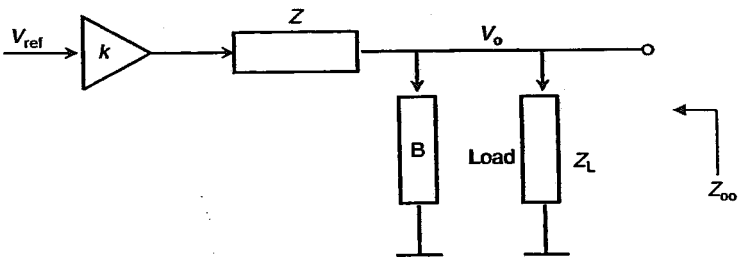
$$\frac{1}{Z_{of}} = \frac{1}{Z_o} + \frac{1}{Z_L}, \tag{6.81}$$

where Z_o is the closed-loop output impedance seen by the load. Then

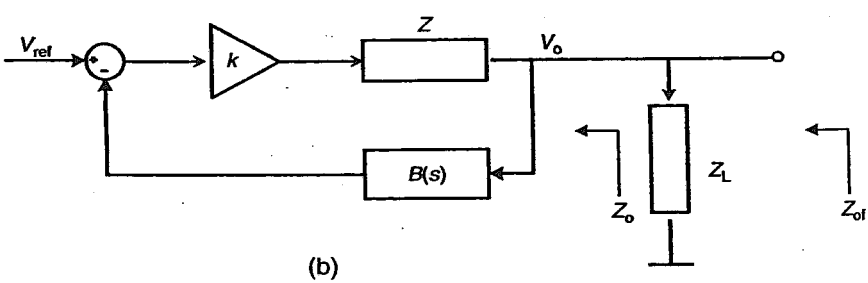
$$Z_o = \left(\frac{1}{Z_{of}} - \frac{1}{Z_L}\right)^{-1} \tag{6.82}$$

if $|\beta A| \gg 1$, then $Z_{of} \ll Z_{oo}$, and if $Z_{of} \ll Z_L$, then $Z_{of} \approx Z_o$ and Z_L will not have much influence on Z_{of} and its stability. This is a desirable condition, but not always possible to achieve.

$Z_{of} = (Z_{oo}/(1 + \beta A))$ has the same poles as the transfer function v_o/v_{ref}, its phase and gain margins can also stabilize the gain and shape its frequency response.



(a)



(b)

Figure 6.34 Output impedance.

6.2.8 State–Space Representation of Switching Converters

6.2.8.1 Review of Linear System Analysis

Consider the simple linear circuit shown in Figure 6.35. The circuit is a second-order system since it has two storage elements: a capacitor and an inductor. It is also a low-pass filter as the capacitor attenuates or filters the high-frequency signal beyond the corner frequency of the filter. State variables of this second-order low-pass filter are chosen to be the current flowing through the inductor, x_1, and the voltage across the capacitor, x_2. The source variable is designated as u_1. Applying Kirchoff's voltage law, the source variable, u_1, is equal to the sum of the voltage drop across the inductor and the voltage across the capacitor

$$u_1 = L\dot{x}_1 + x_2, \tag{6.83}$$

where

$$\dot{x}_1 = \frac{dx_1}{dt} \tag{6.84}$$

and is equal to the time rate of change of the inductor current, x_1. Applying Kirchoff's current law, the inductor current, x_1, is equal to the sum of currents flowing through the capacitor, C, and the resistor, R:

$$\dot{x}_1 = C\dot{x}_2 + \frac{x_2}{R}, \tag{6.85}$$

where

$$\dot{x}_2 = \frac{dx_2}{dt} \tag{6.86}$$

and is equal to the time rate of change of the capacitor voltage, x_2. Equation (6.83) can be rearranged to yield the rate of change of the inductor current, $\dot{x}_1$ as

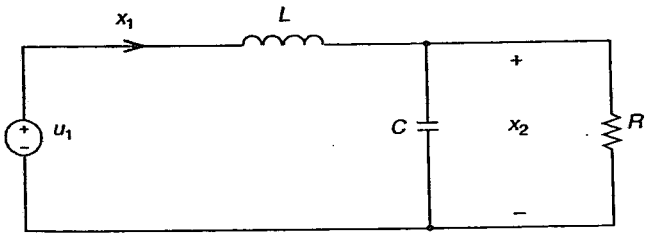


Figure 6.35 A simple second-order low-pass circuit.

$$\dot{x}_1 = -\frac{x_2}{L} + \frac{u_1}{L} \tag{6.87}$$

while Equation (6.85) can be rearranged to yield the time rate of change of the capacitor voltage, $\dot{x}_2$ as

$$\dot{x}_2 = \frac{x_1}{C} + \frac{-x_2}{RC}. \tag{6.88}$$

From the context of linear system analysis, these equations can be written in matrix form as

$$\dot{\boldsymbol{x}} = \boldsymbol{A}\boldsymbol{x} + \boldsymbol{B}\boldsymbol{u}, \tag{6.89}$$

where $\boldsymbol{x}$ is the state vector, $\boldsymbol{A}$ is the state coefficient matrix, $\boldsymbol{u}$ is the source vector, and $\boldsymbol{B}$ is the source coefficient matrix. In our example, these matrices are

$$\boldsymbol{x} = \begin{bmatrix} x_1 \\ x_2 \end{bmatrix}, \tag{6.90}$$

$$\boldsymbol{A} = \begin{bmatrix} 0 & -\frac{1}{L} \\ \frac{1}{C} & -\frac{1}{RC} \end{bmatrix}, \tag{6.91}$$

$$\boldsymbol{u} = [u_1], \tag{6.92}$$

and

$$\boldsymbol{B} = \begin{bmatrix} \frac{1}{L} \\ 0 \end{bmatrix}. \tag{6.93}$$

If either $\boldsymbol{A}$ or $\boldsymbol{B}$ contains a function of $\boldsymbol{x}$ or $\boldsymbol{u}$, then it is a nonlinear system. For the case of a linear system, the DC solution is obtained by setting Equation (6.89) to zero to yield

$$\boldsymbol{x} = -\boldsymbol{A}^{-1}\boldsymbol{B}\boldsymbol{u}, \tag{6.94}$$

where $\boldsymbol{A}^{-1}$ is the inverse of the state coefficient matrix. The inverse of a matrix is the adjoint matrix divided by its determinant. It should be noted that the determinant of $\boldsymbol{A}$ must be nonzero for a valid DC solution. Taking the Laplace transform of Equation (6.89), gives

$$s\boldsymbol{X}(s) = \boldsymbol{A}\boldsymbol{X}(s) + \boldsymbol{B}\boldsymbol{U}(s) \tag{6.95}$$

or

$$\boldsymbol{X}(s) = (s\boldsymbol{I} - \boldsymbol{A})^{-1}\boldsymbol{B}\boldsymbol{U}(s), \tag{6.96}$$

where I is the identity matrix having the same dimension as A. For our simple second-order example, we have

$$\begin{bmatrix} X_1(s) \\ X_2(s) \end{bmatrix} = \frac{\begin{bmatrix} s+\frac{1}{RC} & -\frac{1}{L} \\ \frac{1}{C} & s \end{bmatrix} \begin{bmatrix} \frac{1}{L} \\ 0 \end{bmatrix} U(s)}{s^2 + \frac{s}{RC} + \frac{1}{LC}}. \tag{6.97}$$

Equation (6.97) yields two transfer functions. The transfer function relating the inductor current, x_1, to the input voltage, u_1, $X_1(s)/U_1(s)$, is

$$\frac{X_1(s)}{U_1(s)} = \frac{(1/L)(s+(1/RC))}{(s^2+(s/RC)+(1/LC))} \tag{6.98}$$

while the transfer function relating the capacitor voltage, x_2, to the input voltage, u_1, $X_2(s)/U_1(s)$, is

$$\frac{X_2(s)}{U_1(s)} = \frac{1/LC}{(s^2+(s/RC)+(1/LC))}. \tag{6.99}$$

It can be seen that the linear system analysis lends itself readily to computer simulations.

6.2.9 State–Space Averaging

State–space averaging is an approximation technique that *approximates the switching converter as a continuous linear system* [4]. State–space averaging requires that the effective output filter corner frequency, f_c, to be much smaller than the switching frequency, f_s or $f_c/f_s \ll 1$. This is similar to the requirement for a low output-switching ripple. Final results of the state–space averaging can be either a mathematical or equivalent circuit model. The mathematical model permits the designer to determine voltages, currents, and small-signal transfer functions of the switching converter. However, this model does not enable the designer to physically visualize electrical processes occurring in the switching converter. The equivalent circuit model provides the designer with a better understanding of the physical operation of the switching converter. In general, both the mathematical and equivalent circuit models are necessary and recommended in the design of practical switching converters. There are two drawbacks of the state–space averaging technique. The major one is that it does not result in a general linearized model of a switching converter (a model that is independent of the switching converter configuration, operating mode, and control variable). The other drawback is that it requires extensions and modifications if the control

variable is other than the duty cycle [16]. The major advantages of this method are the establishment of a complete converter model with both steady-state (DC) and dynamic (AC) quantities, and the mathematical rigor with which it can be carried out [17].

Procedures for state–space averaging are as follows:

Step 1. Identify switched models over a switching cycle. Draw the linear switched circuit model for each state of the switching converter (e.g., currents through inductors and voltages across capacitors).

Step 2. Identify state variables of the switching converter. Write state equations for each switched circuit model using Kirchoff's voltage and current laws.

Step 3. Perform state–space averaging using the duty cycle as a weighting factor and combine state equations into a single averaged state equation. The state-space averaged equation is

$$\dot{x} = [A_1 d + A_2(1-d)]x + [B_1 d + B_2(1-d)]u. \tag{6.100}$$

This results in a set of nonlinear continuous equations. A nonlinear continuous equivalent circuit can be drawn from this set of nonlinear equations.

Step 4. Perturb the averaged state equation to yield steady-state (DC) and dynamic (AC) terms and eliminate the product of any AC terms.

Step 5. Draw the linearized equivalent circuit model.

Step 6. Perform hybrid modeling using a DC transformer, if desired.

We will make use of the above procedures to obtain state–space averaged models for (a) an ideal buck converter operating in the continuous mode, (b) an ideal buck converter operating in the discontinuous mode, (c) a continuous-mode buck converter with an output capacitor containing an equivalent-series-resistance (ESR), and (d) an ideal boost converter.

6.2.9.1 State–Space Averaged Model for an Ideal Buck Converter

We now illustrate the state–space averaging method for an ideal buck converter shown in Figure 6.36 operating in the continuous mode. State variables for this buck converter are chosen as the inductor current, x_1, and the capacitor voltage, x_2. With the assumption of ideal switching devices, two switched models are shown in Figure 6.37(a) and (b), respectively. Using Kirchoff's voltage law in Figure 6.37(a), the state equation is

$$u_1 = L\dot{x}_1 + x_2 \tag{6.101}$$

and using Kirchoff's current law, the state equation is

$$x_1 = C\dot{x}_2 + \frac{x_2}{R} \tag{6.102}$$

for the interval when the switching transistor is switched on, i.e., dT. Similarly, applying Kirchoff's voltage law to the switched model shown in Figure 6.37(b), the state equation is

$$0 = L\dot{x}_1 + x_2 \tag{6.103}$$

and applying Kirchoff's current law, the state equation is

$$x_1 = C\dot{x}_2 + \frac{x_2}{R} \tag{6.104}$$

for the interval when the switching transistor is switched off, i.e., $(1 - d)T$. Equations (6.101) to (6.104) can be written in matrix form as

$$\begin{bmatrix} \dot{x}_1 \\ \dot{x}_2 \end{bmatrix} = \begin{bmatrix} 0 & -(1/L) \\ 1/C & -(1/RC) \end{bmatrix} \begin{bmatrix} x_1 \\ x_2 \end{bmatrix} + \begin{bmatrix} 1/L \\ 0 \end{bmatrix} [u_1] \tag{6.105}$$

for the dT interval and

$$\begin{bmatrix} \dot{x}_1 \\ \dot{x}_2 \end{bmatrix} = \begin{bmatrix} 0 & -(1/L) \\ 1/C & -(1/RC) \end{bmatrix} \begin{bmatrix} x_1 \\ x_2 \end{bmatrix} + \begin{bmatrix} 0 \\ 0 \end{bmatrix} [u_1] \tag{6.106}$$

for the $(1 - d)T$ interval, respectively. The state-space averaged state coefficient matrix is

$$\bar{A} = \begin{bmatrix} 0 & -(1/L) \\ 1/C & -(1/RC) \end{bmatrix} d + \begin{bmatrix} 0 & -(1/L) \\ 1/C & -(1/RC) \end{bmatrix} (1 - d) \tag{6.107}$$

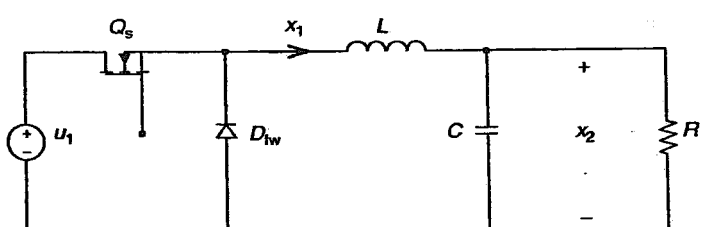


Figure 6.36 Circuit schematic of an ideal buck converter with the state and source variables indicated.

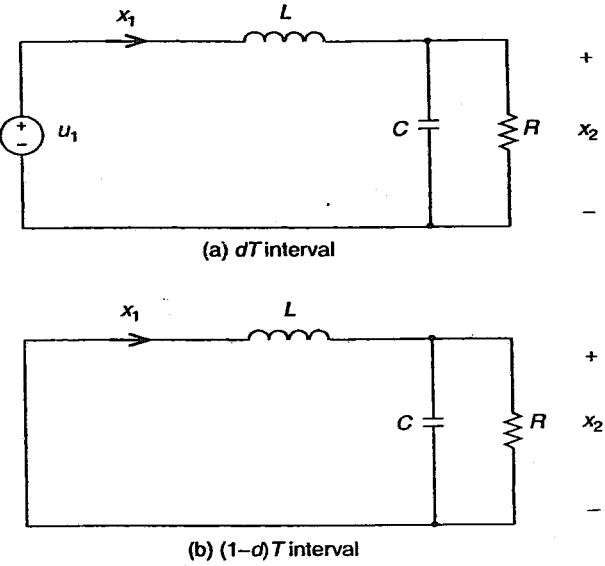


Figure 6.37 Switched models for the ideal buck converter.

or

$$\bar{A} = \begin{bmatrix} 0 & -(1/L) \\ 1/C & -(1/RC) \end{bmatrix}. \tag{6.108}$$

The state–space averaged source coefficient matrix is

$$\bar{B} = \begin{bmatrix} 1/L \\ 0 \end{bmatrix} d + \begin{bmatrix} 0 \\ 0 \end{bmatrix} (1-d) = \begin{bmatrix} d/L \\ 0 \end{bmatrix}. \tag{6.109}$$

State–space averaged equations for the buck converter in matrix form are

$$\begin{bmatrix} \dot{x}_1 \\ \dot{x}_2 \end{bmatrix} = \begin{bmatrix} 0 & -(1/L) \\ 1/C & -(1/RC) \end{bmatrix} \begin{bmatrix} x_1 \\ x_2 \end{bmatrix} + \begin{bmatrix} d/L \\ 0 \end{bmatrix} [u_1]. \tag{6.110}$$

From Equation (6.110), two nonlinear equations describing the state–space averaged model of the buck converter are

$$\dot{x}_1 = -\frac{x_2}{L} + \frac{d}{L} u_1 \tag{6.111}$$

and

$$\dot{x}_2 = \frac{1}{C}x_1 - \frac{1}{RC}x_2. \tag{6.112}$$

These equations are nonlinear because the duty cycle, d, is a function of u_1. Equations (6.111) and (6.112) can be rearranged to yield

$$u_1 d = L\dot{x}_1 + x_2 \tag{6.113}$$

and

$$x_1 = C\dot{x}_2 + \frac{x_2}{R}. \tag{6.114}$$

A nonlinear continuous equivalent circuit can be drawn based on Equations (6.113) and (6.114). This is shown in Figure 6.38. In this figure, $u_1 d$ represents a pulsed voltage source. The next step is to linearize the state–space averaged equation. It should be noted that any nonlinear continuous system can be approximated as a linear system within a small neighborhood about its DC operating point. Each of the state and source variables is assumed to comprise of a steady-state (DC) term and a dynamic (AC) term as shown below:

$$x_1 = x_{10} + \hat{x}_1, \tag{6.115}$$

$$x_2 = x_{20} + \hat{x}_2, \tag{6.116}$$

$$u_1 = u_{10} + \hat{u}_1, \tag{6.117}$$

and

$$d = D + \hat{d}. \tag{6.118}$$

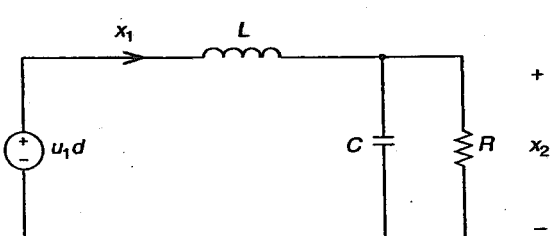


Figure 6.38 A nonlinear continuous equivalent circuit of the ideal buck converter.

In the above equations, the AC terms are identified by the "hat" notation. The amplitudes of the AC terms are assumed to be small so that the product of any AC terms is negligible. Substituting these variables into state–space averaged Equations (6.111) and (6.112), the perturbed state–space averaged equations are

$$\frac{d\hat{x}_1}{dt} = -\frac{1}{L}\left(x_{20} + \hat{x}_2\right) + \frac{1}{L}\left(D + \hat{d}\right)\left(u_{10} + \hat{u}_1\right) \tag{6.119}$$

and

$$\frac{d\hat{x}_2}{dt} = \frac{1}{C}(x_{10} + \hat{x}_1) - \frac{1}{RC}(x_{20} + \hat{x}_2). \tag{6.120}$$

Neglecting the AC product term of $\hat{d}\hat{u}_1$, Equations (6.119) and (6.120) can be simplified to yield

$$\dot{x}_1 = \frac{1}{L}(-x_{20} + Du_{10}) + \frac{1}{L}(-\hat{x}_2 + D\hat{u}_1 + \hat{d}u_{10}) \tag{6.121}$$

and

$$\dot{x}_2 = \frac{1}{C}\left(x_{10} - \frac{x_{20}}{R}\right) + \frac{1}{C}\left(\hat{x}_1 - \frac{\hat{x}_2}{R}\right). \tag{6.122}$$

From Equation (6.31), the DC solution is

$$0 = \frac{1}{L}(-x_{20} + Du_{10}) \tag{6.123}$$

or

$$\frac{x_{20}}{u_{10}} = D. \tag{6.124}$$

This is the steady-state voltage conversion ratio for an ideal buck converter operating in the continuous mode. The AC term from Equation (6.121) is

$$\frac{d\hat{x}_1}{dt} = \frac{1}{L}(-\hat{x}_2 + D\hat{u}_1 + \hat{d}u_{10}) \tag{6.125}$$

or

$$\hat{x}_2 = D_{\hat{u}_1} + \hat{d}_{u_{10}} - L\frac{d\hat{x}_1}{dt}. \tag{6.126}$$

Equation (6.126) reveals that the output voltage modulation is due primarily to changes in the input voltage, $\hat{u}_1$, the modulation in the duty cycle, $\hat{d}$, and the modulation in the inductor current, $\hat{x}_1$. From Equation (6.122), the steady-state or DC solution is

$$0 = \frac{1}{C}\left(x_{10} - \frac{x_{20}}{R}\right) \tag{6.127}$$

or

$$x_{10} = \frac{x_{20}}{R}. \tag{6.128}$$

Equation (6.128) reveals that the steady-state input current is equal to the steady-state output voltage, x_{20}, divided by the output resistance, R. The AC solution from Equation (6.122) is

$$\frac{d\hat{x}_2}{dt} = \frac{1}{C}\left(\hat{x}_1 - \frac{\hat{x}_2}{R}\right) \tag{6.129}$$

or

$$\hat{x}_1 = C\frac{d\hat{x}_2}{dt} + \frac{\hat{x}_2}{R}. \tag{6.130}$$

Equation (6.130) shows that the current modulation in the inductor is the sum of the current modulation due to the charging or discharging of the capacitor and the output current modulation due to modulation in the output voltage across the load. Equation (6.121) can be rearranged to yield

$$x_{20} + \hat{x}_2 = -L\dot{x}_1 + D(u_{10} + \hat{u}_1) + \hat{d}u_{10}. \tag{6.131}$$

or

$$x_2 = Du_1 + \hat{d}u_{10} - L\dot{x}_1 \tag{6.132}$$

The above equation shows that the output voltage, x_2, is equal to the sum of a steady-state input, Du_1, and a modulated dependent voltage source of $\hat{d}u_{10}$ minus the voltage drop across the output inductor, $L\dot{x}_1$. Equation (6.122) can be rearranged to yield

$$x_{10} + \hat{x}_1 = C\dot{x}_2 + \frac{x_{20} + \hat{x}_2}{R} \tag{6.133}$$

or

$$x_1 = C\dot{x}_2 + \frac{x_2}{R}. \tag{6.134}$$

The above equation satisfies Kirchoff's current law at the output node. A linear equivalent circuit of the ideal buck converter operating in the continuous mode described by Equations (6.132) and (6.134) is shown in Figure 6.39. The input source, Du_1, is a function of the DC operating point as represented by the steady-state duty cycle, D. The dependent voltage source $\hat{d}u_{10}$ is a consequence of the modulation in the duty cycle.

The linearized equivalent circuit in Figure 6.39 does not actually represent the buck converter since the input source is represented by a modulated voltage source of Du_1. As mentioned previously, the linearized equivalent circuit shown in Figure 6.39 is not unique. It can be manipulated to yield either a source- or a load-reflected equivalent circuit [17]. The source circuitry comprises of the input voltage source, u_1, while the load circuitry consists of the output capacitor (C_2), output inductor (L), and load resistor (R). To draw a source-reflected linearized equivalent circuit for the ideal buck converter, Equations (6.132) and (6.134) can be manipulated to preserve u_1. From Equation (6.132),

$$u_1 + \frac{\hat{d}}{D}u_{10} = \frac{x_2}{D} + \frac{L}{D^2}\dot{x}_1 D \tag{6.135}$$

and from Equation (6.134)

$$Dx_1 = (D^2C)\frac{\dot{x}_2}{D} + \frac{x_2}{D}\frac{D^2}{R} \tag{6.136}$$

since the output voltage state variable is x_2/D. The source-reflected linearized equivalent circuit for the ideal buck converter is shown in Figure 6.40. Figure 6.39 is already in the form of a load-reflected equivalent circuit since the load variables x_2, L, C, and R are "preserved" [17]. The hybrid modeling technique introduced by Middlebrook and Cûk [4] can be used to combine the source-reflected and the load-reflected linearized equivalent circuits into

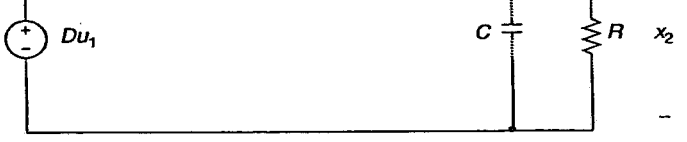


Figure 6.39 A linear equivalent circuit of the ideal buck converter.

a single equivalent circuit using a pseudo-element called a "DC transformer." This element was introduced only as a convenient modeling tool in the state–space averaging technique [4]; so it cannot be realized physically. The linearized equivalent circuit of the ideal buck converter using the DC transformer is shown in Figure 6.41. The turn-ratio of the DC transformer is D, which corresponds to the duty cycle of the buck converter. It should be noted that both input and output variables are preserved in this equivalent circuit. As such, the linearized equivalent circuit using the DC transformer is a very convenient model for the simulation of the switching converter as a component in a complex power electronic system.

6.2.9.2 State–Space Averaged Model for the Discontinuous-Mode Buck Converter

There are three switched models for the buck converter operating in the discontinuous mode as shown in Figure 6.42. Since there are three intervals in one switching period, the state–space averaged coefficient matrices are

$$\bar{A} = A_1 d_1 + A_2 d_2 + A_3(1 - d_1 - d_2) \tag{6.137}$$

and

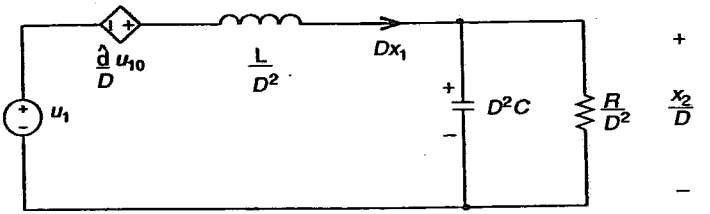


Figure 6.40 A source-reflected linearized equivalent circuit of the ideal buck converter.

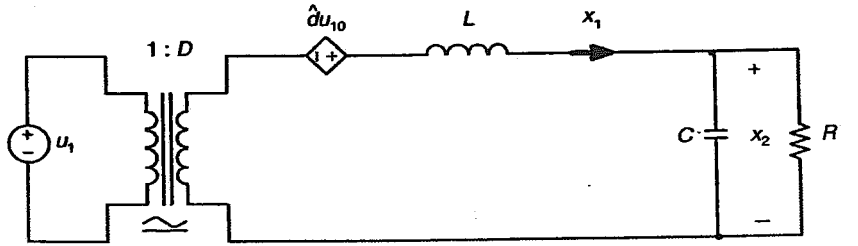


Figure 6.41 A linearized equivalent circuit of the ideal buck converter using a DC transformer.

$$\bar{B} = B_1 d_1 + B_2 d_2 + B_3(1 - d_1 - d_2). \tag{6.138}$$

Equations (6.101) to (6.104) now apply for the $d_1 T$ and $d_2 T$ intervals. During the $(1 - d_1 - d_2)T$ interval, Kirchoff's voltage law yields

$$\dot{x}_1 = 0 \tag{6.139}$$

and Kirchoff's current law gives

$$C\dot{x}_2 + \frac{x_2}{R} = 0. \tag{6.140}$$

The state and source coefficient matrices during this interval are

$$A_3 = \begin{bmatrix} 0 & 0 \\ 0 & -\frac{1}{RC} \end{bmatrix} \tag{6.141}$$

and

$$B_3 = \begin{bmatrix} 0 \\ 0 \end{bmatrix}. \tag{6.142}$$

State–space averaging using Equations (6.137) and (6.138) yields

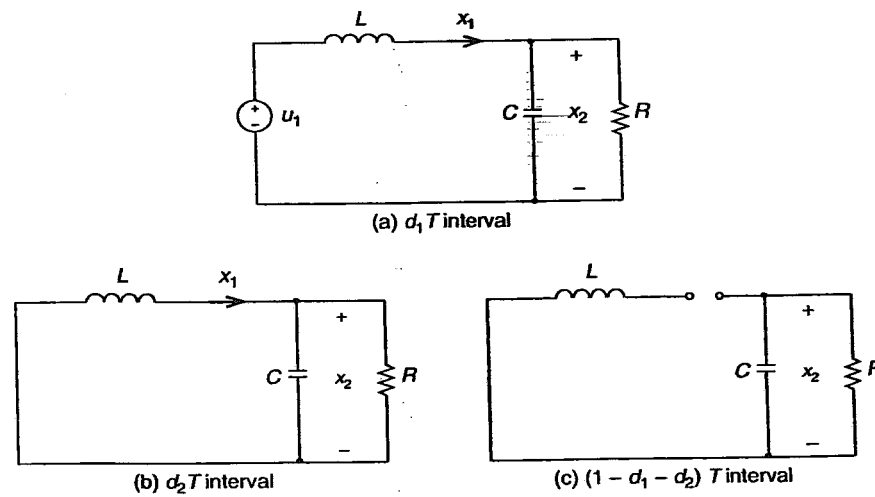


Figure 6.42 Switched models for the buck converter operating in the discontinuous mode.

$$\bar{A} = \begin{bmatrix} 0 & \dfrac{(d_1 + d_2)}{L} \\ \dfrac{d_1 + d_2}{C} & -\dfrac{1}{RC} \end{bmatrix} \tag{6.143}$$

and

$$B = \begin{bmatrix} \dfrac{d_1}{L} \\ 0 \end{bmatrix}. \tag{6.144}$$

State–space averaged equations in matrix form for the discontinuous-mode ideal buck converter are

$$\begin{bmatrix} \dot{x}_1 \\ \dot{x}_2 \end{bmatrix} = \begin{bmatrix} 0 & -\dfrac{(d_1 + d_2)}{L} \\ \dfrac{d_1 + d_2}{C} & -\dfrac{1}{RC} \end{bmatrix} \begin{bmatrix} x_1 \\ x_2 \end{bmatrix} + \begin{bmatrix} \dfrac{d_1}{L} \\ 0 \end{bmatrix} u_1 \tag{6.145}$$

which gives

$$\dot{x}_1 = -\frac{(d_1 + d_2)}{L} x_2 + \frac{d_1}{L} u_1 \tag{6.146}$$

or

$$u_1 d_1 = (d_1 + d_2) x_2 \tag{6.147}$$

since $\dot{x}_1 = 0$ from Equation (6.43), and

$$\dot{x}_2 = \frac{(d_1 + d_2)}{C} x_1 - \frac{x_2}{RC}. \tag{6.148}$$

A nonlinear continuous equivalent circuit derived from Equations (6.147) and (6.148) is shown in Figure 6.43. It can be seen that the state–space averaged discontinuous mode buck converter is a first-order system. The disappearance of the output inductor is a direct consequence of the constraint that $\dot{x}_1 = 0$. In the discontinuous mode,

$$x_1(0) = x_1(T) = 0. \tag{6.149}$$

This implies that the inductor current starts at zero and resets to zero with no net increase in one switching period. Thus, x_1 no longer qualifies as a state variable in the discontinuous mode of operation since it has lost its dynamic properties. However, an input voltage perturbation does cause a perturb-

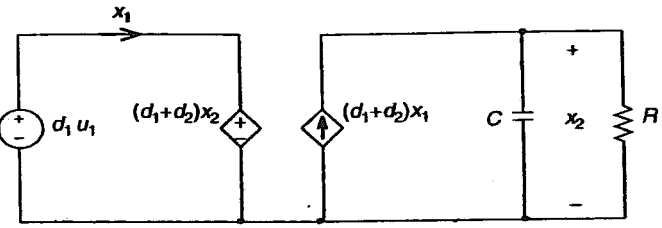


Figure 6.43 A nonlinear continuous equivalent circuit for the discontinuous-mode buck converter.

ation of the instantaneous inductor current from its steady-state value, which in turn results in a corresponding perturbation of the steady-state output voltage. The "average inductor current" is the quantity, which reflects the effect of this perturbation [4]. Thus, the average inductor current is introduced as a substitute for the "lost" state-variable.

The instantaneous inductor current, x_1, can be expressed in terms of u_1 and x_2. The instantaneous inductor current, x_1, in the steady state is

$$x_1 = \frac{I_{Lp}}{2}, \tag{6.150}$$

where I_{Lp} is the peak inductor current. The voltage across the inductor during the d_1T interval can be expressed as

$$u_1 - x_2 = L\frac{I_{Lp} f_s}{d_1}. \tag{6.151}$$

Combining Equations (6.150) and (6.151), the instantaneous inductor current, x_1, can be written as

$$x_1 = (u_1 - x_2)\frac{d_1}{2Lf_s}. \tag{6.152}$$

Equations (6.147), (6.148), and (6.152) are perturbed to yield

$$(u_{10} + \hat{u}_1)(D_1 + \hat{d}_1) = (D_1 + \hat{d}_1 + D_2 + \hat{d}_2)(x_{20} - \hat{x}_2), \tag{6.153}$$

$$\frac{d\hat{x}_2}{dt} = \frac{(D_1 + \hat{d}_1 + D_2 + \hat{d}_2)}{C}(x_{10} + \hat{x}_1) - \frac{(x_{20} + \hat{x}_2)}{RC}, \tag{6.154}$$

and

$$x_{10} + \hat{x}_1 = (u_{10} + \hat{u}_1 - x_{20} - \hat{x}_2)\frac{(D_1 + \hat{d}_1)}{2Lf_s}. \tag{6.155}$$

Steady-state or DC terms are:

$$0 = -(D_1 + D_2)x_{20} + D_1 u_{10}, \tag{6.156}$$

$$0 = (D_1 + D_2)x_{10} - \frac{x_{20}}{R}, \tag{6.157}$$

and

$$x_{10} = (u_{10} - x_{20})\frac{D_1}{2Lf_s}. \tag{6.158}$$

Dynamic or AC terms are:

$$0 = -(D_1 + D_2)\hat{x}_2 + (u_{10} - x_{20})\hat{d}_1 - x_{20}\hat{d}_2 + D_1\hat{u}_1, \tag{6.159}$$

$$C\frac{d\hat{x}_2}{dt} = (D_1 + D_2)\hat{x}_1 - \frac{\hat{x}_2}{R} + x_{10}(\hat{d}_1 + \hat{d}_2), \tag{6.160}$$

and

$$\hat{x}_1 = \frac{1}{2Lf_s}\left[D_1(\hat{u}_1 - \hat{x}_2) + (u_{10} - x_{20})\hat{d}_1\right]. \tag{6.161}$$

Equations (6.156) to (6.158) can be manipulated to yield the DC voltage conversion ratio for the discontinuous-mode buck converter. Equating Equations (6.157) and (6.158) to eliminate x_{10} yields

$$\frac{x_{20}}{R(D_1 + D_2)} = \frac{(u_{10} - x_{20})D_1}{2Lf_s}. \tag{6.162}$$

A quadratic equation results after substituting $(D_1 + D_2) = (D_1 u_{10}/x_{20})$ from Equation (6.156) into Equation (6.162)

$$\frac{2Lf_s}{RD_1^2}x_{20}^2 + x_{20}u_{10} - u_{10}^2 = 0. \tag{6.163}$$

The DC voltage conversion ratio, M, is

$$M = \frac{x_{20}}{u_{10}} = \frac{2}{1 + \sqrt{1 + (8Lf_s/RD_1^2)}}, \tag{6.164}$$

which is similar to Equation (2.39) after substituting R from Equation (2.31). From Equation (6.164),

$$M + M\sqrt{\frac{8Lf_s}{RD_1^2} + 1} = 2. \tag{6.165}$$

Solving for D_1 yields

$$D_1 = M\sqrt{\frac{2Lf_s}{R(1-M)}}. \tag{6.166}$$

Then, from Equation (6.156)

$$D_1 + D_2 = \frac{u_{10}}{x_{20}}D_1 = \frac{1}{M}M\sqrt{\frac{2Lf_s}{R(1-M)}} = \sqrt{\frac{2Lf_s}{R(1-M)}}. \tag{6.167}$$

The DC inductor current, x_{10}, is found by substituting the voltage conversion ratio, M, and D_1 into Equation (6.158) to yield

$$\begin{aligned} x_{10} &= x_{20}\left(\frac{u_{10}}{x_{20}} - 1\right)\frac{M\sqrt{2Lf_s/R(1-M)}}{2Lf_s} \\ &= x_{20}\left(\frac{1}{M} - 1\right)\frac{M}{\sqrt{2Lf_sR(1-M)}} \end{aligned} \tag{6.168}$$

or

$$x_{10} = x_{20}\sqrt{\frac{1-M}{2Lf_sR}}. \tag{6.169}$$

Substituting the DC voltage conversion ratio M, D_1, and $(D_1 + D_2)$ into Equation (6.159) yields

$$0 = -\sqrt{\frac{2Lf_s}{R(1-M)}}\hat{x}_2 + x_{20}\left(\frac{u_{10}}{x_{20}} - 1\right)\hat{d}_1 - x_{20}\hat{d}_2 + M\sqrt{\frac{2Lf_s}{R(1-M)}}\hat{u}_1 \tag{6.170}$$

or

$$0 = -\sqrt{\frac{2Lf_s}{R(1-M)}}\hat{x}_2 + x_{20}\frac{1-M}{M}\hat{d}_1 - x_{20}\hat{d}_2 + M\sqrt{\frac{2Lf_s}{R(1-M)}}\hat{u}_1. \tag{6.171}$$

Solving for $\hat{d}_2$

$$\hat{d}_2 = \left(-\frac{1}{x_{20}}\right)\sqrt{\frac{2Lf_s}{R(1-M)}}\hat{x}_2 + \frac{(1-M)}{M}\hat{d}_1 + \frac{M}{x_{20}}\sqrt{\frac{2Lf_s}{R(1-M)}}\hat{u}_1. \tag{6.172}$$

Substituting D_1 and M into Equation (6.161) yields

$$\hat{x}_1 = \frac{1}{2Lf_s}\left[M\sqrt{\frac{2Lf_s}{R(1-M)}}(\hat{u}_1 - \hat{x}_2) + x_{20}\left(\frac{u_{10}}{x_{20}} - 1\right)\hat{d}_1\right] \tag{6.173}$$

or

$$\hat{x}_1 = \frac{M}{\sqrt{2Lf_sR(1-M)}}(\hat{u}_1 - \hat{x}_2) + \frac{x_{20}}{2Lf_s}\left(\frac{1}{M} - 1\right)\hat{d}_1 \tag{6.174}$$

or

$$\hat{x}_1 = -\frac{M}{\sqrt{2Lf_sR(1-M)}}\hat{x}_2 + \frac{x_{20}}{2Lf_s}\frac{1-M}{M}\hat{d}_1 + \frac{M}{\sqrt{2Lf_sR(1-M)}}\hat{u}_1. \tag{6.175}$$

Substituting $(D_1 + D_2)$ and $\hat{x}_1$ into Equation (6.160) yields

$$C\frac{d\hat{x}_2}{dt} = \sqrt{\frac{2Lf_s}{R(1-M)}}\left[\frac{M}{\sqrt{2Lf_sR(1-M)}}(\hat{u}_1 - \hat{x}_2) + \frac{x_{20}}{2Lf_s}\left(\frac{1}{M} - 1\right)\hat{d}_1\right] - \frac{1}{R}\hat{x}_2 + x_{20}(\hat{d}_1 + \hat{d}_2) \tag{6.176}$$

or

$$C\frac{d\hat{x}_2}{dt} = \frac{M}{R(1-M)}(\hat{u}_1 - \hat{x}_2) + \frac{x_{20}}{M}\sqrt{\frac{1-M}{2Lf_sR}}\hat{d}_1 - \frac{1}{R}\hat{x}_2 + x_{20}\sqrt{\frac{1-M}{2Lf_sR}}(\hat{d}_1 + \hat{d}_2), \tag{6.177}$$

or

$$C\frac{d\hat{x}_2}{dt}=\frac{1}{R(M-1)}\hat{x}_2+\frac{x_{20}}{M}\sqrt{\frac{1-M}{2Lf_sR}}(1+M)\hat{d}_1$$
$$+\frac{M}{R(1-M)}\hat{u}_1+x_{20}\sqrt{\frac{1-M}{2Lf_sR}}\hat{d}_2. \tag{6.178}$$

Because

$$x_{20}\sqrt{\frac{1-M}{2Lf_sR}}\hat{d}_2=x_{20}\sqrt{\frac{1-M}{2Lf_sR}}\left[-\left(\frac{1}{x_{20}}\right)\sqrt{\frac{2Lf_s}{R(1-M)}}\hat{x}_2+\frac{1-M}{M}\hat{d}_1\right.$$
$$\left.+\frac{M}{x_{20}}\sqrt{\frac{2Lf_s}{R(1-M)}}\hat{u}_1\right] \tag{6.179}$$

or

$$x_{20}\sqrt{\frac{1-M}{2Lf_sR}}\hat{d}_2=-\left(\frac{1}{R}\right)\hat{x}_2+\frac{x_{20}}{M}\sqrt{\frac{1-M}{2Lf_sR}}(1-M)\hat{d}_1+\frac{M}{R}\hat{u}_1, \tag{6.180}$$

then,

$$C\frac{d\hat{x}_2}{dt}=\left[\frac{1}{R(M-1)}-\frac{1}{R}\right]\hat{x}_2+\frac{x_{20}}{M}\sqrt{\frac{1-M}{2Lf_sR}}[(1+M)$$
$$+(1-M)]\hat{d}_1+\left[\frac{M}{R(1-M)}+\frac{M}{R}\right]\hat{u}_1 \tag{6.181}$$

or

$$C\frac{d\hat{x}_2}{dt}=\frac{1}{R}\frac{2-M}{M-1}\hat{x}_2+\frac{2x_{20}}{M}\sqrt{\frac{1-M}{2Lf_sR}}\hat{d}_1+\frac{M}{R}\frac{2-M}{1-M}\hat{u}_1. \tag{6.182}$$

Eliminating x_{10} and $\hat{x}_1$ in Equation (6.160) and taking the Laplace transform yields

$$\hat{u}_1(s)=\left[\frac{sRC(1-M)}{M(2-M)}+\frac{1}{M}\right]\hat{x}_2(s)$$
$$-\left[\frac{2x_{20}}{M^2(2-M)}\sqrt{\frac{R(1-M)^3}{2Lf_s}}\right]\hat{d}_1(s). \tag{6.183}$$

Equation (6.183) can be used to draw a linearized equivalent circuit for the discontinuous mode buck converter. Let [18]

$$j_1 = 2x_{20}\sqrt{\frac{1-M}{2Lf_sR}}, \tag{6.184}$$

$$j_2 = \frac{2x_{20}}{M}\sqrt{\frac{1-M}{2Lf_sR}}, \tag{6.185}$$

$$r_1 = R\frac{(1-M)}{M^2}, \tag{6.186}$$

$$r_2 = R(1-M), \tag{6.187}$$

$$g_1 = \frac{1}{R}\frac{M^2}{(1-M)}, \tag{6.188}$$

and

$$g_2 = \frac{M}{R}\frac{(2-M)}{(1-M)}. \tag{6.189}$$

Using the above parameters, a linearized equivalent circuit for the discontinuous mode buck converter is shown in Figure 6.44.

6.2.9.3 *State–Space Averaged Model for a Buck Converter with a Capacitor ESR*

Figure 6.45 shows a buck converter with an output filter capacitor that has an equivalent series resistance of R_{esr}. With the assumption of ideal elements except for the output filter capacitor, two switched models are shown in Figure 6.46(a) and (b), respectively. Using Kirchoff's voltage law in Figure 6.46(a), the state equation is

$$u_1 = L\dot{x}_1 + x_2 + R_{esr}C\dot{x}_2 \tag{6.190}$$

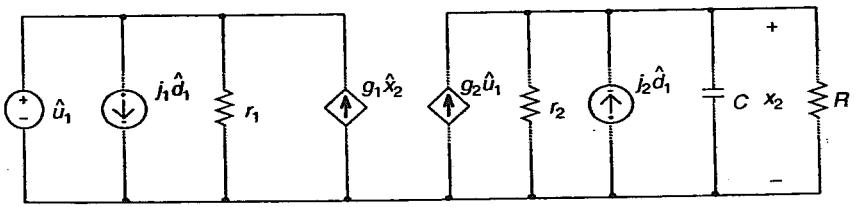


Figure 6.44 A linearized equivalent circuit for the discontinuous-mode buck converter.

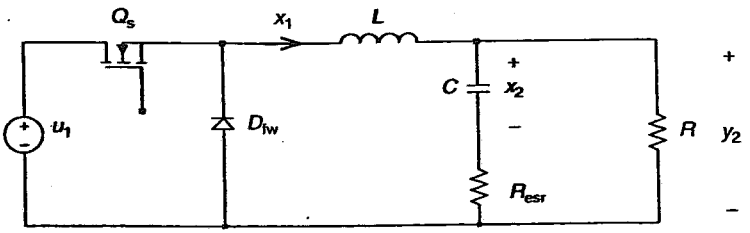
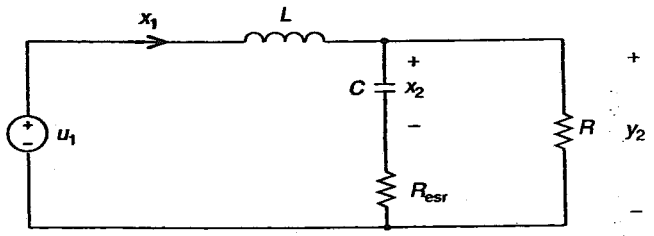
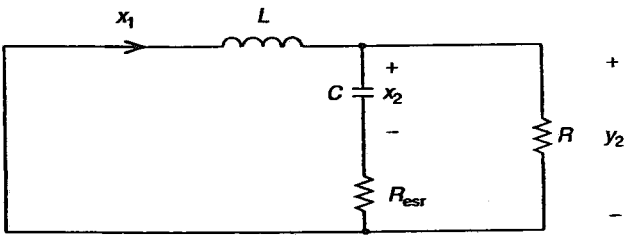


Figure 6.45 Circuit schematic of a buck converter with a R_{esr}.



(a) dT interval



(b) $(1-d)T$ interval

Figure 6.46 Switched models for the buck converter with a R_{esr}.

and using Kirchoff's current law, the state equation is

$$x_1 = C\dot{x}_2 + \frac{x_2 + R_{esr}C\dot{x}_2}{R} \tag{6.191}$$

for the interval when the switching transistor is switched on. Solving for $\dot{x}_2$ in Equation (6.191),

$$\dot{x}_2 = \frac{R}{C(R_{esr}+R)}x_1 - \frac{1}{C(R_{esr}+R)}x_2. \tag{6.192}$$

Substituting $\dot{x}_2$ from Equation (6.192) into Equation (6.190) and solving for $\dot{x}_1$ yields

$$\dot{x}_1 = -\frac{R_{esr}R}{L(R_{esr}+R)}x_1 - \frac{R}{L(R_{esr}+R)}x_2 + \frac{u_1}{L}. \tag{6.193}$$

Equations (6.192) and (6.193) can be written in matrix form as

$$\begin{bmatrix}\dot{x}_1\\ \dot{x}_2\end{bmatrix} = \begin{bmatrix}\dfrac{-R_{esr}R}{L(R_{esr}+R)} & \dfrac{-R}{L(R_{esr}+R)}\\ \dfrac{R}{C(R_{esr}+R)} & \dfrac{-1}{C(R_{esr}+R)}\end{bmatrix}\begin{bmatrix}x_1\\ x_2\end{bmatrix} + \begin{bmatrix}1/L\\ 0\end{bmatrix}[u_1]. \tag{6.194}$$

Similarly, applying Kirchoff's voltage law to Figure 6.46(b), the state equation is

$$0 = L\dot{x}_1 + x_2 + R_{esr}C\dot{x}_2. \tag{6.195}$$

Using Kirchoff's current law, the state equation is

$$x_1 = C\dot{x}_2 + \frac{x_2 + R_{esr}C\dot{x}_2}{R} \tag{6.196}$$

for the interval when the switching transistor is switched off. Equation (6.196) can be solved for $\dot{x}_2$ to give

$$\dot{x}_2 = \frac{R}{C(R_{esr}+R)}x_2 - \frac{1}{C(R_{esr}+R)}x_2. \tag{6.197}$$

Substituting $\dot{x}_2$ from Equation (6.197) into Equation (6.195) and solving for $\dot{x}_2$ yields

$$\dot{x}_1 = \frac{-R_{esr}R}{L(R_{esr}+R)}x_1 - \frac{R}{L(R_{esr}+R)}x_2. \tag{6.198}$$

Equations (6.197) and (6.198) can be written in matrix form as

$$\begin{bmatrix}\dot{x}_1\\ \dot{x}_2\end{bmatrix} = \begin{bmatrix}\dfrac{-RR_{esr}}{L(R_{esr}+R)} & \dfrac{-R}{L(R_{esr}+R)}\\ \dfrac{R}{C(R_{esr}+R)} & \dfrac{-1}{C(R_{esr}+R)}\end{bmatrix}\begin{bmatrix}x_1\\ x_2\end{bmatrix} + \begin{bmatrix}0\\ 0\end{bmatrix}[u_1]. \tag{6.199}$$

The state–space averaged state coefficient matrix is

$$\bar{A} = A_1 d + A_2(1-d) = A_1 = A_2 = \begin{bmatrix} \frac{-R_{esr}R}{L(R_{esr}+R)} & \frac{-R}{L(R_{esr}+R)} \\ \frac{R}{C(R_{esr}+R)} & \frac{-1}{C(R_{esr}+R)} \end{bmatrix}. \quad (6.200)$$

The state–space averaged source coefficient matrix is

$$\bar{B} = B_1 d + B_2(1-d) = \begin{bmatrix} \frac{d}{L} \\ 0 \end{bmatrix}. \quad (6.201)$$

State–space averaged equations for the buck converter with an output capacitor R_{esr} in matrix form are

$$\begin{bmatrix} \dot{x}_1 \\ \dot{x}_2 \end{bmatrix} = \begin{bmatrix} \frac{-R_{esr}R}{L(R_{esr}+R)} & \frac{-R}{L(R_{esr}+R)} \\ \frac{R}{C(R_{esr}+R)} & \frac{-1}{C(R_{esr}+R)} \end{bmatrix} \begin{bmatrix} x_1 \\ x_2 \end{bmatrix} + \begin{bmatrix} d/L \\ 0 \end{bmatrix} [u_1] \quad (6.202)$$

which yield

$$\dot{x}_1 = \frac{-R_{esr}R}{L(R_{esr}+R)} x_1 - \frac{R}{L(R_{esr}+R)} x_2 + \frac{d}{L} u_1, \quad (6.203)$$

and

$$\dot{x}_2 = \frac{R}{C(R_{esr}+R)} x_1 - \frac{x_2}{C(R_{esr}+R)}. \quad (6.204)$$

Equation (6.203) can be rearranged to yield

$$\mathrm{d}u_1 = L\dot{x}_1 + \frac{R_{esr}R}{(R_{esr}+R)} x_1 + \frac{R}{(R_{esr}+R)} x_2 \quad (6.205)$$

or

$$\mathrm{d}u_1 = L\dot{x}_1 + y_2, \quad (6.206)$$

where

$$y_2 = \frac{R_{esr}Rx_1}{(R_{esr}+R)} + \frac{Rx_2}{(R_{esr}+R)} = (R_{esr}//R)x_1 + \frac{Rx_2}{(R_{esr}+R)} \quad (6.207)$$

is the voltage across the load resistor, R. Equation (6.204) can be rearranged to give

$$x_1 = C\dot{x}_2 + \frac{(x_2 + R_{esr}C\dot{x}_2)}{R}. \tag{6.208}$$

Equation (6.206) is a consequence of the Kirchoff's voltage law while Equation (6.208) is a consequence of the Kirchoff's current law. A nonlinear continuous equivalent circuit can be drawn based on Equations (6.206) and (6.208). This is shown in Figure 6.47. The next step is to linearize the state–space averaged equations given in Equations (6.203) and (6.204). The perturbed state–space averaged equations are

$$\frac{d\hat{x}_2}{dt} = \frac{-R_{esr}R(x_{10} + \hat{x}_1)}{L(R_{esr} + R)} - \frac{R(x_{20} + \hat{x}_2)}{L(R_{esr} + R)} + \frac{(D + \hat{d})(u_{10} + \hat{u}_1)}{L} \tag{6.209}$$

and

$$\frac{d\hat{x}_2}{dt} = \frac{R(x_{10} + \hat{x}_1)}{C(R_{esr} + R)} - \frac{(x_{20} + \hat{x}_2)}{C(R_{esr} + R)}. \tag{6.210}$$

The DC or steady-state terms are

$$0 = \frac{-R_{esr}R}{L(R_{esr} + R)}x_{10} - \frac{R}{L(R_{esr} + R)}x_{20} + \frac{Du_{10}}{L} \tag{6.211}$$

and

$$0 = \frac{R}{C(R_{esr} + R)}x_{10} - \frac{x_{20}}{C(R_{esr} + R)}. \tag{6.212}$$

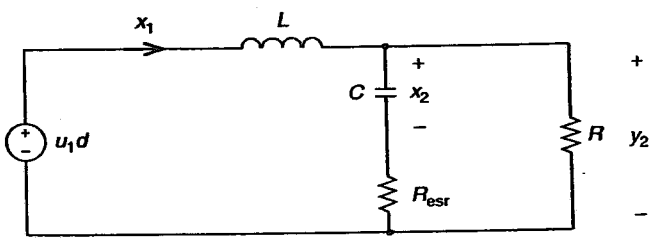


Figure 6.47 A nonlinear continuous equivalent circuit for the buck converter with a R_{esr}.

The dynamic or AC terms are

$$\frac{d\hat{x}_1}{dt} = \frac{-R_{esr}R}{L(R_{esr}+R)}\hat{x}_1 - \frac{R}{L(R_{esr}+R)}\hat{x}_2 + \frac{D\hat{u}_1}{L} + \frac{\hat{d}u_{10}}{L} \tag{6.213}$$

and

$$\frac{d\hat{x}_2}{dt} = \frac{R}{C(R_{esr}+R)}\hat{x}_1 - \frac{\hat{x}_2}{C(R_{esr}+R)}. \tag{6.214}$$

From Equation (6.211),

$$Du_{10} = \frac{R_{esr}R}{(R_{esr}+R)}x_{10} + \frac{R}{(R_{esr}+R)}x_{20} = y_2 \tag{6.215}$$

which yields the output voltage across the load resistor. From Equation (6.212),

$$x_{20} = Rx_{10} \tag{6.216}$$

which indicates that the DC voltage across the capacitor is equal to the product of the DC current and the load resistor. Equation (6.209) can be rearranged to yield

$$Du_1 + \hat{d}u_{10} = L\dot{\hat{x}}_1 + (R_{esr}//R)x_1 + \frac{Rx_2}{(R_{esr}+R)} = L\dot{\hat{x}}_1 + y_2 \tag{6.217}$$

while Equation (6.210) can be rearranged to give

$$C\dot{x}_2 = \frac{R}{R_{esr}+R}x_1 - \frac{1}{R_{esr}+R}x_2. \tag{6.218}$$

A linearized continuous equivalent circuit for the buck converter with an output capacitor R_{esr} can be drawn using Equations (6.217) and (6.218). This is shown in Figure 6.48. This linearized continuous equivalent circuit is similar to the linearized continuous circuit for the ideal buck converter shown in Figure 6.41, except that the output capacitor is replaced by an ideal capacitor in series with an equivalent series resistance, R_{esr}. Figure 6.49 shows the linearized equivalent circuit using a DC transformer with a turns-ratio of D.

6.2.9.4 State–Space Averaged Model for an Ideal Boost Converter

Figure 6.50 shows an ideal boost converter with a source variable u_2 to simulate the load current modulation. With the assumption of ideal circuit

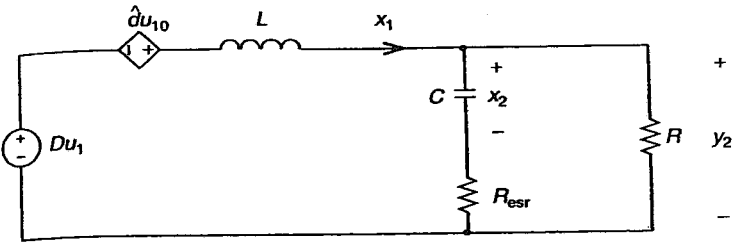


Figure 6.48 A linearized continuous equivalent circuit for the buck converter with a R_{esr}.

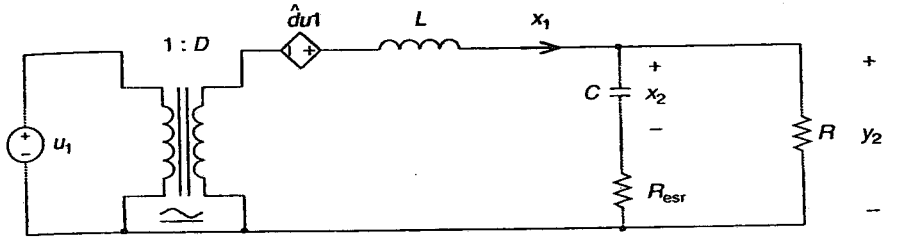


Figure 6.49 A linearized equivalent circuit using DC transformer with a turns-ratio of D.

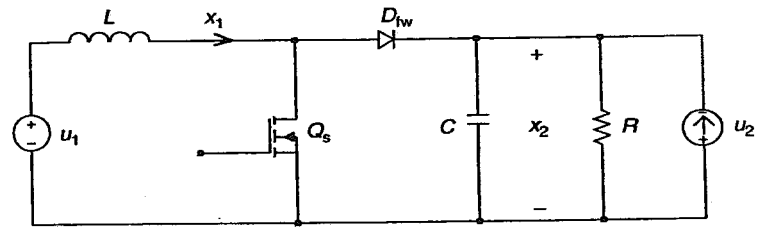


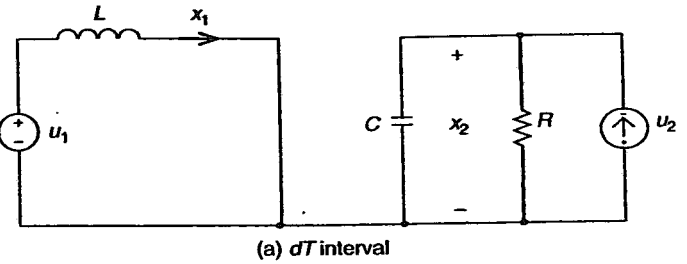
Figure 6.50 Circuit schematic of an ideal boost converter.

elements, two switched models are shown in Figure 6.51. The state variables for this boost converter are chosen as the inductor current, x_1, and the capacitor voltage, x_2. In the dT interval, state equations are

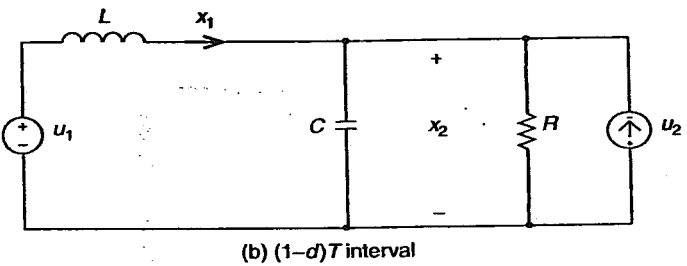
$$u_1 = L\dot{x}_1 \tag{6.219}$$

according to Kirchoff's voltage law and

$$u_2 = C\dot{x}_2 + \frac{x_2}{R} \tag{6.220}$$



(a) dT interval



(b) $(1-d)T$ interval

Figure 6.51 Switched models for the ideal boost converter.

according to Kirchoff's current law. The state equations in matrix form are

$$\begin{bmatrix} \dot{x}_1 \\ \dot{x}_2 \end{bmatrix} = \begin{bmatrix} 0 & 0 \\ 0 & -(1/RC) \end{bmatrix} \begin{bmatrix} x_1 \\ x_2 \end{bmatrix} + \begin{bmatrix} 1/L & 0 \\ 0 & 1/C \end{bmatrix} \begin{bmatrix} u_1 \\ u_2 \end{bmatrix}. \tag{6.221}$$

During the $(1-d)T$ interval, the state equation using Kirchoff's voltage law is

$$u_1 = L\dot{x}_1 + x_2 \tag{6.222}$$

and the state equation using Kirchoff's current law is

$$x_1 + u_2 = C\dot{x}_2 + \frac{x_2}{R}. \tag{6.223}$$

These state equations can be expressed in matrix form as

$$\begin{bmatrix} \dot{x}_1 \\ \dot{x}_2 \end{bmatrix} = \begin{bmatrix} 0 & -(1/L) \\ 1/C & -(1/RC) \end{bmatrix} \begin{bmatrix} x_1 \\ x_2 \end{bmatrix} + \begin{bmatrix} 1/L & 0 \\ 0 & 1/C \end{bmatrix} \begin{bmatrix} u_1 \\ u_2 \end{bmatrix}. \tag{6.224}$$

Applying state–space averaging, the state coefficient matrix, A, is

$$\bar{A} = A_1 d + A_2(1-d) = \begin{bmatrix} 0 & 0 \\ 0 & -\frac{1}{RC} \end{bmatrix} d + \begin{bmatrix} 0 & -\frac{1}{L} \\ \frac{1}{C} & -\frac{1}{RC} \end{bmatrix} (1-d) \tag{6.225}$$

or

$$\bar{A} = \begin{bmatrix} 0 & -\frac{(1-d)}{L} \\ \frac{(1-d)}{C} & -\frac{1}{RC} \end{bmatrix}. \tag{6.226}$$

The averaged source coefficient matrix is

$$\bar{B} = B_1 d + B_2(1-d) = \begin{bmatrix} \frac{1}{L} & 0 \\ 0 & \frac{1}{C} \end{bmatrix} d + \begin{bmatrix} \frac{1}{L} & 0 \\ 0 & \frac{1}{C} \end{bmatrix} (1-d) \tag{6.227}$$

or

$$\bar{B} = \begin{bmatrix} \frac{1}{L} & 0 \\ 0 & \frac{1}{C} \end{bmatrix}. \tag{6.228}$$

State–space averaged equations in matrix form are

$$\begin{bmatrix} \dot{x}_1 \\ \dot{x}_2 \end{bmatrix} = \begin{bmatrix} 0 & -(1-d)/L \\ (1-d)/C & -(1/RC) \end{bmatrix} \begin{bmatrix} x_1 \\ x_2 \end{bmatrix} + \begin{bmatrix} 1/L & 0 \\ 0 & 1/C \end{bmatrix} \begin{bmatrix} u_1 \\ u_2 \end{bmatrix} \tag{6.229}$$

or

$$\begin{bmatrix} \dot{x}_1 \\ \dot{x}_2 \end{bmatrix} = \begin{bmatrix} \frac{-(1-d)x_2}{L} \\ \frac{(1-d)x_1}{C} - \frac{x_2}{RC} \end{bmatrix} + \begin{bmatrix} \frac{u_1}{L} \\ \frac{u_2}{C} \end{bmatrix}. \tag{6.230}$$

From Equation (6.230), the two nonlinear state–space averaged equations are

$$\dot{x}_1 = \frac{-(1-d)x_2}{L} + \frac{1}{L} u_1 \tag{6.231}$$

or

$$\frac{u_1}{(1-d)} = \frac{L}{(1-d)} \dot{x}_1 + x_2 \tag{6.232}$$

and

$$\dot{x}_2 = \frac{(1-d)x_1}{C} - \frac{x_2}{RC} + \frac{u_2}{C} \tag{6.233}$$

or

$$\frac{u_2}{(1-d)} + x_1 = \frac{C}{(1-d)}\dot{x}_2 + \frac{x_2}{R(1-d)}. \tag{6.234}$$

From Equations (6.232) and (6.234), a nonlinear continuous equivalent circuit can be drawn, as shown in Figure 6.52. The next step is to linearize the nonlinear continuous Equations of (6.231) and (6.233) into a set of linear continuous equations. Applying small-signal approximation to Equations (6.231) and (6.233) yield

$$\frac{d\hat{x}_1}{dt} = \frac{-(1-D-\hat{d})}{L}(x_{20}+\hat{x}_2) + \frac{1}{L}(u_{10}+\hat{u}_1) \tag{6.235}$$

and

$$\frac{d\hat{x}_2}{dt} = \frac{(1-D-\hat{d})}{C}(x_{10}+\hat{x}_1) - \frac{1}{RC}(x_{20}+\hat{x}_2) + \frac{1}{C}\hat{u}_2, \tag{6.236}$$

assuming that $\hat{u}_2$ consists of only the modulation term. Neglecting AC cross-product terms, the above equations can be simplified to

$$\frac{d\hat{x}_1}{dt} = \frac{-(1-D)}{L}\hat{x}_2 + \frac{\hat{d}}{L}x_{20} + \frac{1}{L}\hat{u} - \frac{1-D}{L}x_{20} + \frac{1}{L}u_{10} \tag{6.237}$$

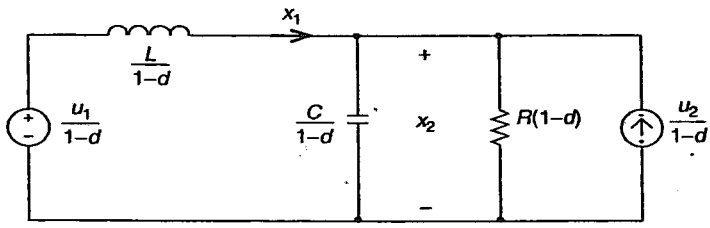


Figure 6.52 Nonlinear continuous equivalent circuit of the ideal boost converter.

and

$$\frac{d\hat{x}_2}{dt} = \frac{(1-D)}{C}\hat{x}_1 - \frac{\hat{d}}{C}x_{10} - \frac{1}{RC}\hat{x}_2 + \frac{1}{C}\hat{u}_2 + \frac{(1-D)}{C}x_{10} - \frac{1}{RC}x_{20}. \tag{6.238}$$

The steady-state or DC solutions are

$$0 = -\frac{(1-D)}{L}x_{20} + \frac{u_{10}}{L} \tag{6.239}$$

and

$$0 = \frac{(1-D)}{C}x_{10} - \frac{x_{20}}{RC}. \tag{6.240}$$

Equation (6.239) can be simplified to yield

$$\frac{x_{10}}{u_{20}} = \frac{1}{(1-D)} \tag{6.241}$$

which is the DC voltage conversion ratio for an ideal boost converter. Equation (6.240) can be rearranged to give

$$x_{10} = \frac{x_{20}/R}{(1-D)} \tag{6.242}$$

or

$$x_{10} = \frac{u_{10}}{R(1-D)^2}, \tag{6.243}$$

which is the DC or average input current of the ideal boost converter. The dynamic or AC solutions are

$$L\frac{d\hat{x}_1}{dt} = -(1-D)\hat{x}_2 + \hat{d}x_{20} + \hat{u}_1 \tag{6.244}$$

and

$$C\frac{d\hat{x}_2}{dt} = (1-D)\hat{x}_1 - x_{10}\hat{d} - \frac{\hat{x}_2}{R} + \hat{u}_2. \tag{6.245}$$

The small-signal averaged state–space equation for the continuous-conduction mode boost converter is

$$\dot{\hat{x}} = \begin{bmatrix} 0 & -\dfrac{(1-D)}{L} \\ \dfrac{(1-D)}{L} & -\dfrac{1}{RC} \end{bmatrix} \hat{x} + \begin{bmatrix} \dfrac{x_{20}}{L} \\ -\dfrac{x_{10}}{C} \end{bmatrix} \hat{d} + \begin{bmatrix} \dfrac{1}{L} & 0 \\ 0 & 1 \end{bmatrix} \begin{bmatrix} \hat{u}_1 \\ \hat{u}_2 \end{bmatrix}. \tag{6.246}$$

Equation (6.246) shows that the system has three inputs. $\hat{u}_1$ and $\hat{u}_2$ represent the perturbations of the input voltage and the output current, respectively. $\hat{d}$ represents the perturbations in the duty cycle; this would be modified by the control variable in a closed-loop system.

A linearized equivalent circuit can be obtained by rearranging Equations (6.237) and (6.238) to give

$$\frac{L}{(1-D)}\dot{\hat{x}}_1 = -x_2 + \frac{x_{20}\hat{d}}{(1-D)} + \frac{1}{(1-D)}u_1 \tag{6.247}$$

and

$$\frac{C}{(1-D)}\dot{\hat{x}}_2 = x_1 - \frac{x_{10}\hat{d}}{(1-D)} - \frac{1}{R(1-D)}x_2 + \frac{1}{(1-D)}u_2. \tag{6.248}$$

A linearized equivalent circuit of the ideal boost converter based on Equations (6.247) and (6.248) is shown in Figure 6.53. The dependent voltage source $x_{20}\hat{d}/(1-D)$ and the dependent current source $x_{10}\hat{d}/(1-D)$ are due to modulation in the duty cycle, i.e., $\hat{d}$.

A linearized source-reflected equivalent circuit for the ideal boost converter can be found by manipulating Equation (6.247) to preserve u_1, x_1, and L. Equation (6.247) becomes

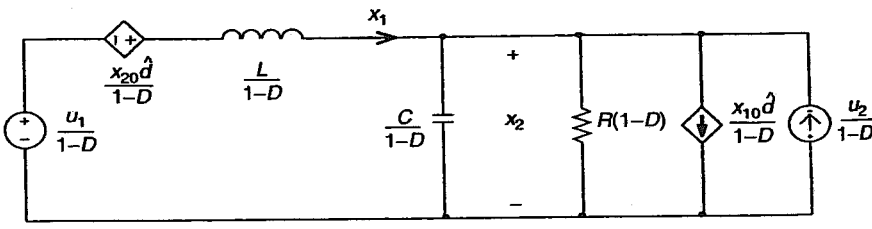


Figure 6.53 Linearized equivalent circuit of the ideal boost converter.

$$L\dot{x}_1 = -x_2(1-D) + x_{20}\hat{d} + u_1. \tag{6.249}$$

Equation (6.248) can be manipulated to yield

$$\frac{C}{(1-D)^2}[\dot{x}_2(1-D)] = x_1 - \frac{x_{10}\hat{d}}{(1-D)} - \frac{[x_2(1-D)]}{R(1-D)^2} + \frac{u_2}{(1-D)}, \tag{6.250}$$

since the output voltage state variable is $x_2(1-D)$. Equation (6.249) represents the Kirchoff's voltage law while Equation (6.250) represents the Kirchoff's current law for the linearized continuous equivalent circuit. Figure 6.54 shows the source-reflected linearized equivalent circuit for the ideal boost converter.

A load-reflected linearized equivalent circuit can be found by manipulating Equation (6.248) to preserve output variables of u_2, x_2, C, and R. This can be attained by multiplying $(1-D)$ to both sides of Equation (6.248)

$$C\dot{x}_2 = x_1(1-D) - \frac{x_2}{R} - x_{10}\hat{d} + u_2. \tag{6.251}$$

It can be seen that the inductor current is now defined as x_1 $(1-D)$ instead of x_1. Thus, Equation (6.247) must be modified to yield

$$\frac{L}{(1-D)^2}\dot{x}_1(1-D) = -x_2 + \frac{u_1}{(1-D)} + \frac{x_{20}\hat{d}}{(1-D)}. \tag{6.252}$$

A load-reflected linearized circuit using Equations (6.251) and (6.252) is shown in Figure 6.55. The source- and load-reflected linearized equivalent circuits can be combined into a single equivalent circuit as shown in Figure 6.56 using a DC transformer with a turns-ratio of $1/(1-D)$.

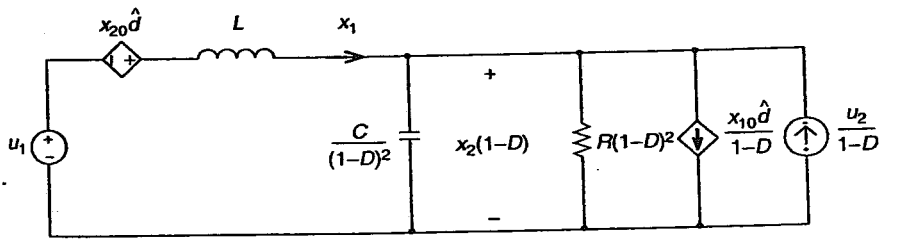


Figure 6.54 Source-reflected linearized equivalent circuit for the ideal boost converter.

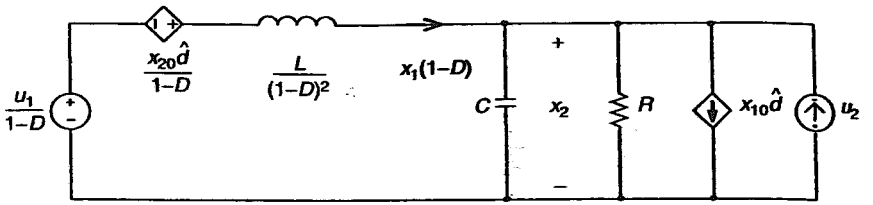


Figure 6.55 Load-reflected linearized circuit for the ideal boost converter.

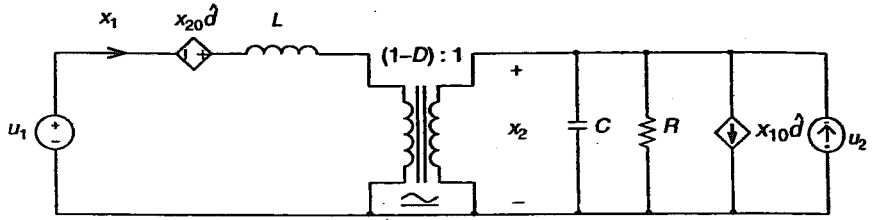


Figure 6.56 DC transformer equivalent circuit for the ideal boost converter.

6.2.10 Switching Converter Transfer Functions

From the results of state–space averaging, transfer functions of the switching converters can be readily obtained using Laplace transformation. Transfer functions are useful for dynamic analysis of the switching converter. The transient response due to input supply perturbation of the switching converter can be found from the input voltage susceptibility transfer function. On the other hand, the transient response due to load modulation can be found from the output impedance of the switching converter. The open-loop transfer function is first used to predict the margin of stability of the switching converter. Loop compensation is then employed to improve the stability of the switching converter.

6.2.10.1 Source-to-State Transfer Functions

From the results of state–space averaging, the perturbed state–space averaged equation can be written as

$$\dot{x} = \bar{A}_0 x + \bar{B}_0 u + E\hat{d} \tag{6.253}$$

where

$$\bar{A}_0 = A_1 D + A_2(1 - D) \tag{6.254}$$

$$\bar{B}_0 = B_1 D + B_2(1 - D) \tag{6.255}$$

and

$$E = (A_1 - A_2)x_0 + (B_1 - B_2)u_0. \tag{6.256}$$

Applying Laplace transform to the perturbed state–space averaged Equation (6.253)

$$sX(s) = \bar{A}_0 X(s) + \bar{B}_0 U(s) + E\hat{d}(s) \tag{6.257}$$

or

$$(sI - \bar{A}_0)X(s) = \bar{B}_0 U(s) + E\hat{d}(s), \tag{6.258}$$

where I is the identity matrix having the same dimension as A_0. Equation (6.258) can be rearranged to yield

$$X(s) = (sI - \bar{A}_0)^{-1}\bar{B}_0 U(s) + (sI - \bar{A}_0)^{-1}E\hat{d}(s). \tag{6.259}$$

In the above equation, $\hat{d}$ is usually a function of x and u. The dependency of $\hat{d}(s)$ on $X(s)$ and $U(s)$ is called the control law. Since $\hat{d}$ is a function of x and u, the control law is usually nonlinear. The linearized control law can be expressed as [19]

$$\hat{d}(s) = F^{\mathrm{T}}(s)X(s) + Q^{\mathrm{T}}(s)U(s), \tag{6.260}$$

where $F^{\mathrm{T}}(s)$ and $Q^{\mathrm{T}}(s)$ are coefficient matrices. Substituting Equation (6.260) into Equation (6.259) yields

$$X(s) = (sI - \bar{A}_0)^{-1}(\bar{B}_0 U(s) + E[F^{\mathrm{T}}(s)X(s) + Q^{\mathrm{T}}(s)U(s)]). \tag{6.261}$$

or

$$X(s) = [sI - \bar{A}_0 - EF^{\mathrm{T}}(s)]^{-1}[\bar{B}_0 + EQ^{\mathrm{T}}(s)]U(s). \tag{6.262}$$

Thus

$$\frac{X(s)}{U(s)} = [sI - \bar{A}_0 - EF^{\mathrm{T}}(s)]^{-1}(\bar{B}_0 + EQ^{\mathrm{T}}(s)) \tag{6.263}$$

is the transfer function matrix relating the state variables to the source variables for a closed-loop switching converter [19]. Derivations of the source-to-state transfer functions for the buck and boost converters are illustrated below.

6.2.10.1.1 Buck converter. The perturbed state–space averaged equations from Equations (6.121) and (6.122) can be rewritten to yield the form of Equation (6.253) as follows:

$$\begin{bmatrix} \dot{x}_1 \\ \dot{x}_2 \end{bmatrix} = \begin{bmatrix} 0 & -(1/L) \\ 1/C & -(1/RC) \end{bmatrix} \begin{bmatrix} x_1 \\ x_2 \end{bmatrix} + \begin{bmatrix} D/L \\ 0 \end{bmatrix} [u_1] + \begin{bmatrix} u_{10}/L \\ 0 \end{bmatrix} \hat{d}. \quad (6.264)$$

The coefficient matrices are

$$\bar{A}_0 = \begin{bmatrix} 0 & -(1/L) \\ 1/C & -(1/RC) \end{bmatrix}, \quad (6.265)$$

$$\bar{B}_0 = \begin{bmatrix} D/L \\ 0 \end{bmatrix}, \quad (6.266)$$

and

$$\bar{E} = \begin{bmatrix} u_{10}/L \\ 0 \end{bmatrix}. \quad (6.267)$$

In a closed-loop converter, the control law describing the voltage-mode PWM controller shown in Figure 5.3(a) is in the form of [19]

$$d(s) = \frac{V_e(s)}{V_p} = \frac{[1 + H(s)]V_R(s) - H(s)X_2(s)}{V_p}, \quad (6.268)$$

where $H(s)$ is the transfer function of the error amplifier and its compensation network, $V_R(s)$ is the transfer function of the reference voltage, and V_p is the peak amplitude of the sawtooth signal. Since the reference voltage is normally a fixed DC value, the modulation in duty cycle can be expressed as

$$\hat{d}(s) = -\frac{H(s)\hat{X}_2(s)}{V_p}. \quad (6.269)$$

The coefficient matrices for the control law are

$$F^T(s) = \begin{bmatrix} 0 & -\dfrac{H(s)}{V_p} \end{bmatrix} \quad (6.270)$$

and

$$Q^{T}(s) = [0 \quad 0]. \tag{6.271}$$

From Equation (6.263), the state variable matrix is

$$\begin{bmatrix} X_1(s) \\ X_2(s) \end{bmatrix} = \begin{bmatrix} s & \frac{1}{L} + \dfrac{u_{10}H(s)}{LV_p} \\ -\frac{1}{C} & s + \dfrac{1}{RC} \end{bmatrix}^{-1} \begin{bmatrix} D/L \\ 0 \end{bmatrix} [U_1(s)] \tag{6.272}$$

or

$$\begin{bmatrix} X_1(s) \\ X_2(s) \end{bmatrix} = \frac{\begin{bmatrix} s+(1/RC) & -((u_{10}H(s)/LV_p)+(1/L)) \\ 1/C & s \end{bmatrix} \begin{bmatrix} D/L \\ 0 \end{bmatrix} [U_1(s)]}{s^2+(s/RC)+(1/LC)+(u_{10}H(s)/LCV_p)}. \tag{6.273}$$

The transfer functions relating the state variables to the source variables for the buck converter are

$$\frac{X_1(s)}{U_1(s)} = \frac{(D/L)[s+(1/RC)]}{s^2+(s/RC)+(1/LC)+(u_{10}H(s)/LCV_p)} \tag{6.274}$$

and

$$\frac{X_2(s)}{U_1(s)} = \frac{(D/LC)}{s^2+(s/RC)+(1/LC)+(u_{10}H(s)/LCV_p)}. \tag{6.275}$$

6.2.10.1.2 Boost converter. The perturbed state–space averaged equations from Equations (6.237) and (6.238) can be rewritten to yield the form of Equation (6.253) as follows:

$$\begin{bmatrix} \dot{x}_1 \\ \dot{x}_2 \end{bmatrix} = \begin{bmatrix} 0 & -((1-D)/L) \\ (1-D)/C & -(1/RC) \end{bmatrix} \begin{bmatrix} x_1 \\ x_2 \end{bmatrix} + \begin{bmatrix} 1/L & 0 \\ 0 & 1/C \end{bmatrix} \begin{bmatrix} u_1 \\ u_2 \end{bmatrix} + \begin{bmatrix} x_{20}/L \\ -(x_{10}/C) \end{bmatrix} \hat{d}. \tag{6.276}$$

From the above equation, the coefficient matrices are

$$\bar{A}_0 = \begin{bmatrix} 0 & -((1-D)/L) \\ (1-D)/C & -(1/RC) \end{bmatrix}, \tag{6.277}$$

$$\bar{B}_0 = \begin{bmatrix} 1/L & 0 \\ 0 & 1/C \end{bmatrix}, \tag{6.278}$$

and

$$\bar{E} = \begin{bmatrix} x_{20}/L \\ -(x_{10}/C) \end{bmatrix}. \tag{6.279}$$

The source-to-state transfer functions for the boost converter can be obtained by substituting Equations (6.270) and (6.271) into Equation (6.262). The state variable matrix is

$$\begin{bmatrix} X_1(s) \\ X_2(s) \end{bmatrix} = \begin{bmatrix} s & \dfrac{1-D}{L} + \dfrac{x_{20}H(s)}{LV_p} \\ -\dfrac{1-D}{C} & \left(s + \dfrac{1}{RC}\right) - \dfrac{x_{10}H(s)}{CV_p} \end{bmatrix}^{-1} \begin{bmatrix} \dfrac{1}{L} & 0 \\ 0 & \dfrac{1}{C} \end{bmatrix} \begin{bmatrix} U_1(s) \\ U_2(s) \end{bmatrix}. \tag{6.280}$$

Taking the inverse matrix,

$$\begin{bmatrix} X_1(s) \\ X_2(s) \end{bmatrix} =$$

$$\frac{\begin{bmatrix} s + \dfrac{1}{RC} - \dfrac{x_{10}H(s)}{CV_p} & -\dfrac{(1-D)}{L} - \dfrac{x_{20}H(s)}{LV_p} \\ \dfrac{1-D}{C} & s \end{bmatrix} \begin{bmatrix} \dfrac{1}{L} & 0 \\ 0 & \dfrac{1}{C} \end{bmatrix} \begin{bmatrix} U_1(s) \\ U_2(s) \end{bmatrix}}{s^2 + \left(\left[s - \left(sx_{10}H(s)R/V_p\right)\right]/RC\right) + \left((1-D)^2/LC\right) + \left(x_{20}H(s)(1-D)/LCV_p\right)}. \tag{6.281}$$

Since the input and output variables of the boost converter are x_1 and x_2, respectively, the transfer function relating the state variable, x_1, to the source variable, u_1, $X_1(s)/U_1(s)$, is the input admittance of the boost converter

$$\frac{X_1(s)}{U_1(s)} =$$

$$\frac{(1/L)[s + (1/RC) - (x_{10}H(s)/CV_p)]}{s^2 + \left(s\left[1 - (x_{10}H(s)R/V_p)\right]/RC\right) + \left((1-D^2)/LC\right) + \left(x_{20}H(s)(1-D)/LCV_p\right)}. \tag{6.282}$$

Substituting $x_{10}=u_{10}/R(1-D)^2$ from Equation (6.243) and $x_{20}=u_{10}/(1-D)$ from Equation (6.241) into the above equation to yield

$$\frac{X_1(s)}{U_1(s)}=$$

$$\frac{(1/L)[s+(1/RC)(1-(u_{10}H(s)/V_p(1-D)^2))]}{s^2+(s/RC)[1-(u_{10}H(s)/V_p(1-D)^2)]+((1-D)^2/LC)[1+(u_{10}H(s)/V_p(1-D)^2)]}. \quad (6.283)$$

The output current susceptibility, $X_1(s)/U_2(s)$, for the boost converter is

$$\frac{X_1(s)}{U_2(s)}=$$

$$\frac{-((1-D)/LC)[1+(u_{10}H(s)/V_p(1-D)^2)]}{s^2+(s/RC)[1-(u_{10}H(s)/V_p(1-D)^2)]+((1-D)^2/LC)[1+(u_{10}H(s)/V_p(1-D)^2)]}. \quad (6.284)$$

The input voltage susceptibility, $X_2(s)/U_1(s)$, is

$$\frac{X_2(s)}{U_1(s)}=$$

$$\frac{((1-D)/LC)}{s^2+(s/RC)[1-(u_{10}H(s)/V_p(1-D)^2)]+((1-D)^2/LC)[1+(u_{10}H(s)/V_p(1-D)^2)]}. \quad (6.285)$$

The output impedance, $X_2(s)/U_2(s)$, is

$$\frac{X_2(s)}{U_2(s)}=$$

$$\frac{(s/C)}{s^2+(s/RC)[1-(u_{10}H(s)/V_p(1-D)^2)]+((1-D)^2/LC)[1+(u_{10}H(s)/V_p(1-D)^2)]}. \quad (6.286)$$

6.2.10.2 *Open-Loop Transfer Functions*

The stability of a linearized switching converter can be evaluated by examining its open-loop transfer function using Bode plots for adequate gain and phase margins. To find the open-loop transfer functions, the feedback loop can be mathematically opened by replacing the transformed

AC state vector, $X(s)$, with an independent test vector, $V(s)$, in the control law given in Equation (6.260) to yield [20]

$$\hat{d}(s) = F^{T} V(s) + Q^{T}(s)U(s). \tag{6.287}$$

The open-loop transfer function matrix, $\frac{X(s)}{V(s)}$, is found by combining the above modified control law equation with Equation (6.257) with $U(s)=0$ to yield

$$\frac{X(s)}{V(s)} = (sI - \bar{A}_o)^{-1} E(s) F^{T}(s). \tag{6.288}$$

For a negative-feedback system with touching feedback loops, the overall open-loop transfer function, $G(s)H(s)$, is the sum of the diagonal elements of the open-loop transfer-function matrix, $-(X_k(s)/V_k(s))$. Thus, the open-loop transfer functions for the buck and boost converters are

$$G(s)H(s) = -\left[\frac{X_1(s)}{V_1(s)} + \frac{X_2(s)}{V_2(s)}\right]. \tag{6.289}$$

6.2.10.2.1 Buck converter. The open-loop transfer-function matrix of the buck converter can be expressed as

$$\begin{bmatrix} X_1(s) \\ X_2(s) \end{bmatrix} = \begin{bmatrix} s & 1/L \\ -(1/C) & s + (1/RC) \end{bmatrix} \begin{bmatrix} 0 & -(u_{10}H(s)/LV_p) \\ 0 & 0 \end{bmatrix} \begin{bmatrix} V_1(s) \\ V_2(s) \end{bmatrix} \tag{6.290}$$

or

$$\begin{bmatrix} X_1(s) \\ X_2(s) \end{bmatrix} = \frac{\begin{bmatrix} s + (1/RC) & -(1/L) \\ 1/C & s \end{bmatrix} \begin{bmatrix} 0 & -(u_{10}H(s)/LV_p) \\ 0 & 0 \end{bmatrix} \begin{bmatrix} V_1(s) \\ V_2(s) \end{bmatrix}}{s^2 + (s/RC) + (1/LC)}. \tag{6.291}$$

Since $X_1(s)/V_1(s) = 0$, then the open-loop transfer function for the buck converter is

$$G(s)H(s) = -\frac{X_2(s)}{V_2(s)}, \tag{6.292}$$

or

$$G(s)H(s) = \frac{u_{10}H(s)/CLV_p}{s^2 + (s/RC) + (1/LC)}. \tag{6.293}$$

6.2.10.2.2 Boost converter. The open-loop transfer-function matrix for the boost converter can be expressed as

$$\begin{bmatrix} X_1(s) \\ X_2(s) \end{bmatrix} = \begin{bmatrix} s & (1-D)/L \\ -((1-D)/C) & s+(1/RC) \end{bmatrix}^{-1} \begin{bmatrix} 0 & -(x_{20}H(s)/LV_p) \\ 0 & x_{10}H(s)/CV_p \end{bmatrix} \begin{bmatrix} V_1(s) \\ V_2(s) \end{bmatrix}, \tag{6.294}$$

or

$$\begin{bmatrix} X_1(s) \\ X_2(s) \end{bmatrix} = \frac{\begin{bmatrix} s+(1/RC) & -((1-D)/L) \\ (1-D)/C & s \end{bmatrix} \begin{bmatrix} 0 & -(x_{20}H(s)/LV_p) \\ 0 & x_{10}H(s)/CV_p \end{bmatrix} \begin{bmatrix} V_1(s) \\ V_2(s) \end{bmatrix}}{s^2+(s/RC)+((1-D)^2/LC)}. \tag{6.295}$$

From Equation (6.289), the open-loop transfer function for the boost converter is

$$G(s)H(s) = \frac{(H(s)u_{10}/CV_pR(1-D)^2)[(R(1-D)^2/L)-s]}{s^2+(s/RC)+((1-D)^2/LC)} \tag{6.296}$$

using the relationships from Equations (6.241) and (6.243). It can be seen that the open-loop transfer function of the boost converter includes a right-half-plane zero. This is because the output current in the boost converter decreases as its duty cycle increases. The right-half-plane zero complicates loop compensation in the boost converter since it introduces an additional 90° phase lag. The loop gain of the compensated boost converter is usually forced to roll off at a relatively low frequency with a concomitant decrease in its unity-gain crossover frequency. Thus, in general, the voltage-mode PWM compensated boost converter has inherently narrow bandwidth, and thereby, relatively poor frequency response.

6.2.10.3 Loop Compensations in Buck Converter

As discussed previously, loop compensation involves the selection of the transfer function of the error amplifier, $H(s)$, to shape the frequency response of the switching converter. In some cases, it is possible to satisfy performance specifications of the switching converter by simply adjusting its open-loop gain-factor. This is also known as gain-factor compensation. Assuming that the transfer function, $H(s)$, is equal to a constant, K. The transfer function of the buck converter with gain-factor compensation or a

proportional control scheme can be found from Equation (6.293) as follows:

$$G(s)H(s) = \frac{u_{10}K/CLV_p}{s^2 + (s/RC) + (1/LC)}. \tag{6.297}$$

Figure 6.57 and Figure 6.58 show the magnitude and phase responses of the buck converter with a 16 mH output inductor and a 100 μF output capacitor for several values of load resistance, R. As shown, the magnitude response has a constant gain of 20 $\log_{10}$ ($u_{10}K/LCV_p$) with a minimal phase shift at low frequencies. Beyond the corner frequency of $1/2\pi\sqrt{LC}$, the magnitude response begins to decrease with a slope of −40 dB/decade and the phase tends toward −180°. The magnitude response is overdamped when $R < \sqrt{L/C}$, underdamped when $R > \sqrt{L/C}$, and critically damped when $R = (1/2)\sqrt{L/C}$. The underdamped open-loop buck converter changes its phase rapidly at the corner frequency as shown in Figure 6.58. A more gradual phase transition is observed for the overdamped open-loop buck converter. Since the open-loop phase lag is close to 180°, any additional phase lag can render the buck converter unstable when the loop is closed.

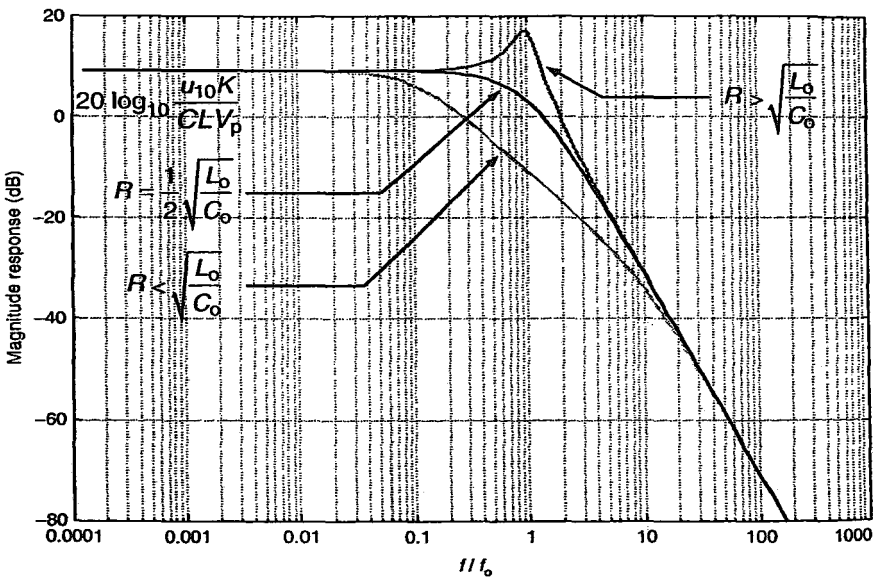


Figure 6.57 Magnitude response of an open-loop buck converter for several values of $\sqrt{L_o/C_o}$.

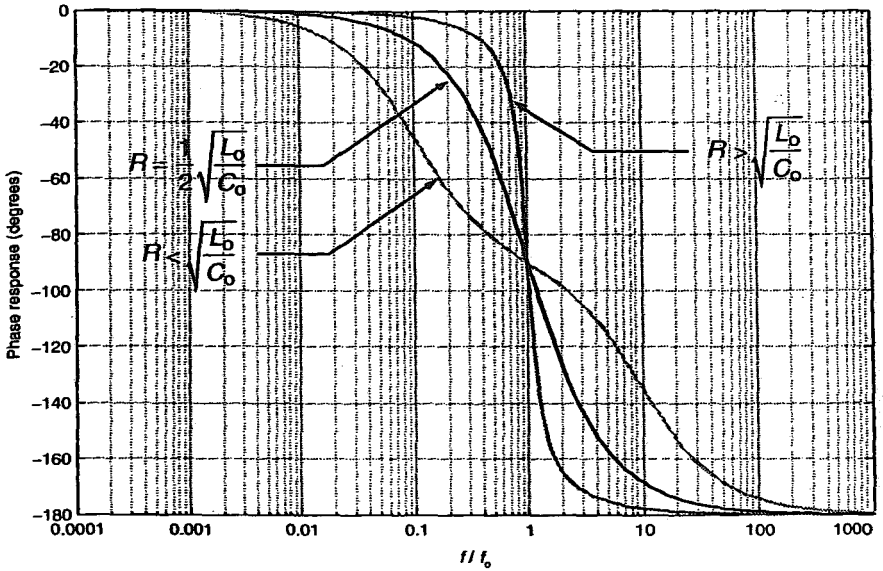


Figure 6.58 Phase response of an open-loop buck converter for several values of $\sqrt{L_o/C_o}$.

The transfer function for a lag-compensator is

$$H_{lag}(s) = \frac{\omega_p K}{s + \omega_p}, \tag{6.298}$$

where ω_p is the pole angular frequency of the lag-compensation network. In general, ω_p must be low enough to achieve a sufficient gain margin. Substituting Equation (6.298) into Equation (6.293) yields the transfer function for a lag-compensated buck converter

$$G(s)H(s) = \frac{K'\omega_p\omega_o^2}{(s^2 + 2\zeta\omega_o s + \omega_o^2)(s + \omega_p)}, \tag{6.299}$$

where $\zeta = 1/(2R\sqrt{C/L})$ is the damping ratio, ω_o is the natural angular frequency, and $K' = Ku_{10}/V_p$. Figure 6.59 and Figure 6.60 show the magnitude and phase responses of the buck converter with a lag-compensator for a pole frequency of $0.01 \times f_o$. As can be seen, a lag-compensated buck converter has a narrower bandwidth compared to that of the open-loop buck converter at the expense of an increase in stability. In practice, the lead-lag compensators shown in Figure 6.15 and Figure 6.25 are employed for loop compensation.

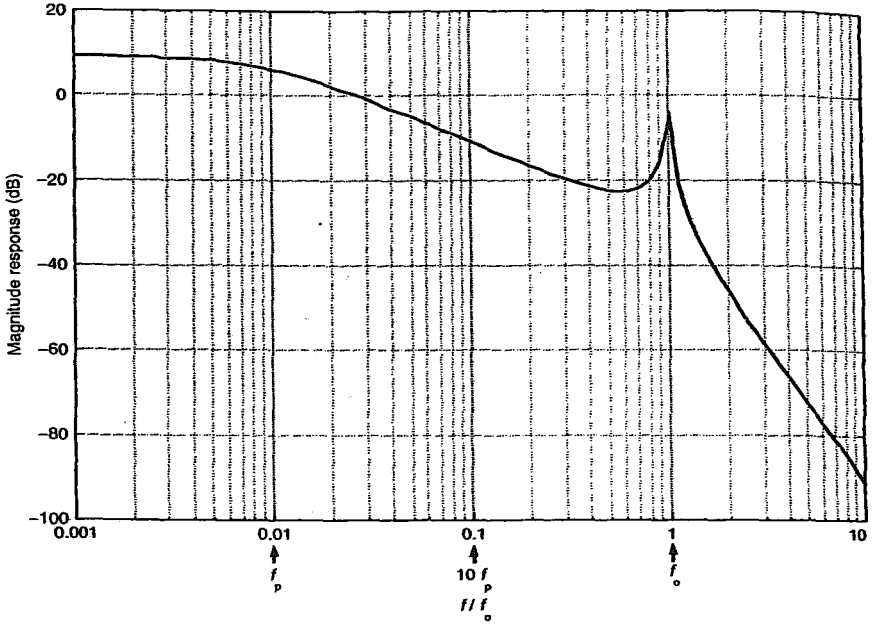


Figure 6.59 Magnitude response of a lag-compensated buck converter with $f_p = 0.01 f_o$.

6.2.11 Complete State Feedback

An important application of the state–space representation is the complete state feedback of the switching converter. All the states of the converter are sensed and multiplied by a feedback gain. This technique allows us to calculate the gains of the feedback vector required to place the closed-loop poles at a desired location.

6.2.11.1 Design of a Control System with Complete State Feedback [9]

Consider a continuous-time linear system, having the following state–space representation:

$$\dot{x} = Ax + Bu. \tag{6.300}$$

A usual control strategy is to generate the error signal as a function of the measurements of the states of the system. In case of a switching converter, the control variable, u, may be chosen proportional to the states as

$$u = -Fx. \tag{6.301}$$

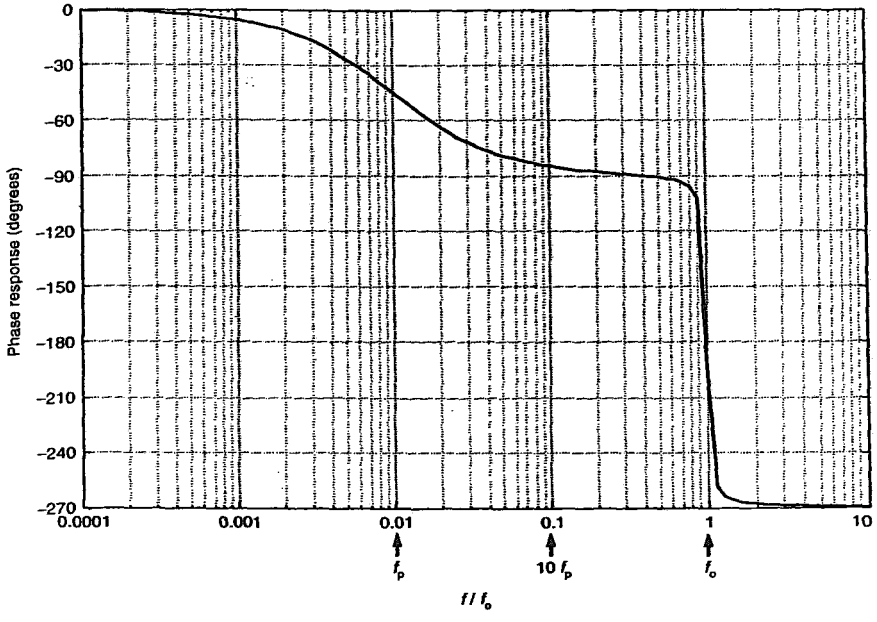


Figure 6.60 Phase response of a lag compensated buck converter with $f_p = 0.01 f_o$.

Then

$$\dot{\boldsymbol{x}} = (\boldsymbol{A} - \boldsymbol{BF})\boldsymbol{x}. \tag{6.302}$$

The closed-loop eigenvalues are found by solving the characteristic equation:

$$\det[s\boldsymbol{I} - \boldsymbol{A} + \boldsymbol{BF}] = 0.$$

Several observations are

- If the state vector has dimension i and the control vector has dimension j, the matrix $\boldsymbol{F}$ will have $i \times j$ elements.
- If the system described by (A,B) is controllable, the choice of the elements of $\boldsymbol{F}$ will control the position of the closed-loop poles on the S plane.
- If the elements of $\boldsymbol{F}$ are real, the closed-loop poles will be real or complex conjugates.
- If the applied control is of scalar type, the resulting $\boldsymbol{F}$ is a row vector, having i elements. The elements of $\boldsymbol{F}$ are unique if the i roots of the characteristic equations are specified.

- The closed-loop poles can be arbitrarily placed by choosing the elements of F.

6.2.11.2 Pole Selection

One way of choosing the closed-loop poles is to select an ith order low-pass Bessel filter for the transfer function, where i is the order of the system that is designed [21]. The step response of a Bessel filter has no overshoot; thus, it is ideal for a voltage regulator. The desired filter can then be selected for a step response that meets a specified settling time. The minimum settling time should be chosen to avoid saturating the control variable. The desired closed-loop poles of the filter,

$$P_s = \{p_1, p_2\} \tag{6.303}$$

can be designed with the aid of the filter toolbox that comes with MATLAB [22] or with any other filter package, like Filter Wiz® [23].

6.2.11.3 Feedback Gains

The values for the elements of the feedback vector F can be obtained by pole placement. The MATLAB command, F=PLACE (A, B, P), can be used to compute the state-feedback matrix F to yield the eigenvalues of ($A - B\,F$) as specified in vector P.

Example 6.6. A buck converter designed to operate in the continuous conduction mode has the following parameters: $R = 4\,\Omega$, $L = 1.330\,\text{mH}$, $C = 94\,\mu\text{F}$, $V_s = 42\,\text{V}$, and $V_a = 12\,\text{V}$. Calculate (a) the open-loop poles, (b) the feedback gains to locate the closed-loop poles at $P = 1000 \times \{-0.3298 + 0.10i\ -0.3298 - 0.10i$, (c) the closed-loop system matrix A_{CL}.

Solution.

(a) The state–space matrices during t_{on} are

$$A_1 = \begin{bmatrix} 1 & -\dfrac{1}{L} \\ \dfrac{1}{C} & -\dfrac{1}{RC} \end{bmatrix}, \quad B_1 = \begin{bmatrix} \dfrac{1}{L} \\ 0 \end{bmatrix}.$$

The state–space matrices during t_{off} are

$$A_2 = \begin{bmatrix} 0 & -\dfrac{1}{L} \\ \dfrac{1}{C} & -\dfrac{1}{RC} \end{bmatrix}, \quad B_2 = \begin{bmatrix} 0 \\ 0 \end{bmatrix}.$$

The state–space averaged model matrices are

$$\bar{A} = A_1 \times D + A_2 \times (1 - D),$$
$$\bar{B} = B_1 \times D + B_2 \times (1 - D).$$

Then

$$\bar{A} = \begin{bmatrix} 0 & -\frac{1}{L} \\ \frac{1}{C} & \frac{1}{RC} \end{bmatrix}, \quad \bar{B} = \begin{bmatrix} \frac{D}{L} \\ 0 \end{bmatrix}.$$

The open-loop poles can be found by the MATLAB command to yield

$$\text{poles}_{\text{OL}} = \text{eig(A) to be poles}_{\text{OL}} = 1000 \times \{-1.3298 + 2.4961i, \\ -1.3298 - 2.4961i\}$$

(b) The equations for the linearized AC small-signal model are

$$\dot{\hat{x}}_1 = \frac{1}{L}(-\hat{x}_2 + D\hat{u} + \hat{d}U),$$
$$\dot{\hat{x}}_1 = \frac{1}{C}\left(\hat{x}_1 - \frac{1}{R}\hat{x}_2\right).$$

Then, the small-signal averaged state–space equations are

$$\dot{\hat{x}} = \begin{bmatrix} 1 & -(1/L) \\ 1/C & -(1/RC) \end{bmatrix} \begin{bmatrix} \hat{x}_1 \\ \hat{x}_2 \end{bmatrix} + \begin{bmatrix} D/L \\ 0 \end{bmatrix} \hat{u} + \begin{bmatrix} U/L \\ 0 \end{bmatrix} \hat{d}.$$

The following MATLAB script can be used to define a state–space model sysOL and plot the step response of the open-loop converter:

```
sysOL = ss(A,B,C,0)
step(sysOL)
```

where A is the system matrix, B is $[D/L\ 0]'$ and $C = [0\ 1]$. Figure 6.61 shows the transient response of the small-signal model of the converter for a step input at $\hat{u}_1$.

To design the control strategy, first assume that the perturbations in the input DC voltage are null, i.e., $\hat{u} = 0$. Then,

$$\dot{\hat{x}} = \bar{A}\hat{x} + E\hat{d}$$

with

$$E = \begin{bmatrix} \frac{U}{L} \\ 0 \end{bmatrix}$$

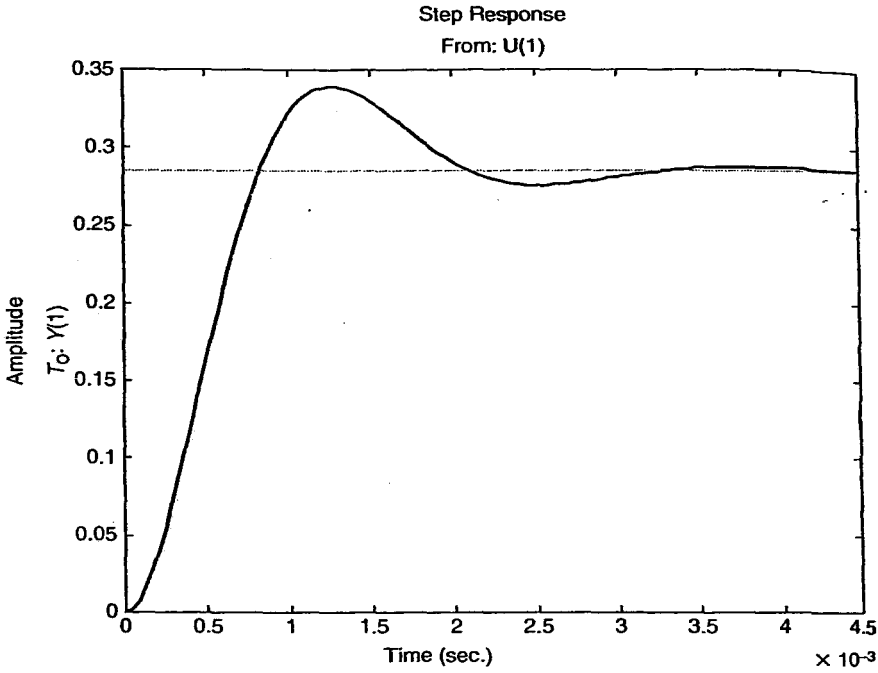


Figure 6.61 Step response of the linearized buck converter.

for voltage-mode control $\hat{d} = (D/V_{\text{ref}})\,\hat{v}_{\text{ref}}$.

If we apply complete state feedback

$$\hat{v}_{\text{ref}} = -\boldsymbol{F}\hat{\boldsymbol{x}}$$

then

$$\dot{\hat{\boldsymbol{x}}} = \bar{\boldsymbol{A}}\hat{\boldsymbol{x}} + \boldsymbol{E}\left(-\frac{D}{V_{\text{ref}}}\boldsymbol{F}\hat{\boldsymbol{x}}\right)$$

or

$$\dot{\hat{\boldsymbol{x}}} = \left(\bar{\boldsymbol{A}} - \boldsymbol{E}\frac{D}{V_{\text{ref}}}\boldsymbol{F}\right)\hat{\boldsymbol{x}}.$$

The closed-loop system matrix is then

$$\bar{\boldsymbol{A}}_{\text{CL}} = \bar{\boldsymbol{A}} - \boldsymbol{E}\frac{D}{V_{\text{ref}}}\boldsymbol{F}.$$

To locate the closed-loop poles at $P=$ 1000* [−0.3298 + 0.10i −0.3298 − 0.10i]', we calculate the feedback gains as

$$P = 1000 \times [-0.3298 + 0.10\text{i} - 0.3298 - 0.10\text{i}]'$$

$$F = \text{place}\left(A, E\frac{D}{V_{\text{ref}}}, P\right).$$

Then, $F=\{-2.6600\ -0.3202\}$.

(c) The closed-loop matrix is

$$\bar{A}_{\text{CL}} = \bar{A} - E\frac{D}{V_{\text{ref}}}F,$$

$$\bar{A}_{\text{CL}} = 1\text{e}4\begin{bmatrix} 0.2000 & -0.0511 \\ 1.0638 & -0.2660 \end{bmatrix}$$

we can check the locations of the closed-loop poles with eig(A_{CL}); which gives

$$\text{ans} = 1\text{e}+2 \times [-3.2980 + 1.0000\text{i} - 3.2980 - 1.0000\text{i}]$$

Figure 6.62 displays the schematic circuit of the closed-loop buck converter used for the simulations. The parameter *loop* changes from 0 to 1 in the

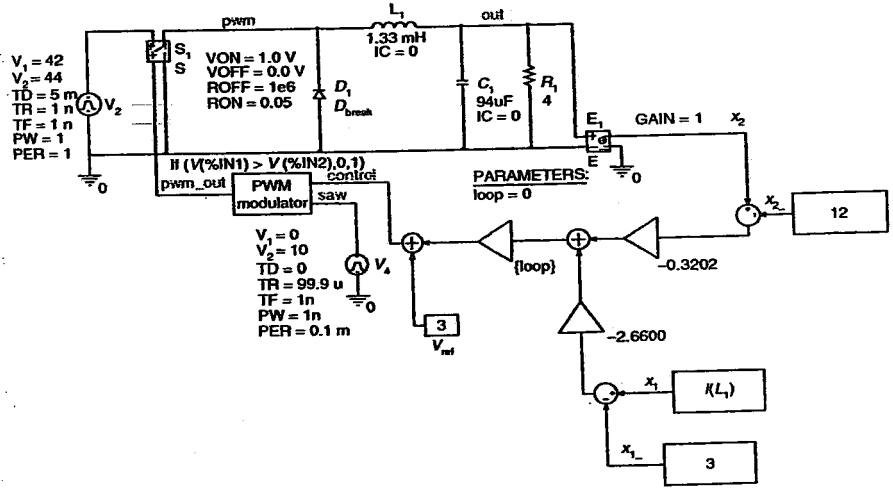


Figure 6.62 PSpice schematic of the switching converter under study.

parametric simulation to obtain the open-loop and the closed-loop responses, respectively. The turn-on transient of the switching converter is shown in Figure 6.63 for the open-loop and the closed-loop converters. Notice that the open-loop response overshoots the steady-state output voltage, while the closed-loop response shows the behavior of a second order system with real poles. The dynamic of the turn-on transient does not necessarily correspond to our previous calculations because this is a large signal swing not modeled by the linear small-signal approximation.

A small perturbation is added to the input voltage source at 5 ms; at that time, the input voltage changes from 42 to 44 V to simulate a line transient. Figure 6.63 shows that the open-loop system evolves to a new steady-state voltage after overshooting. The perturbation in the output voltage of the closed-loop switching converter is hardly noticed. Figure 6.64 displays an expanded view of the output voltage transient at 5 ms. The closed-loop switching converter follows the calculated dynamic response for the small-signal model.

6.2.12 Input EMI Filters

Switching converters, in particular buck or buck–boost converters, have a notorious reputation as one of the worst electromagnetic interference (EMI) generators due to its pulsating input current waveform and switching actions of its semiconductor switches. Electromagnetic interference is the

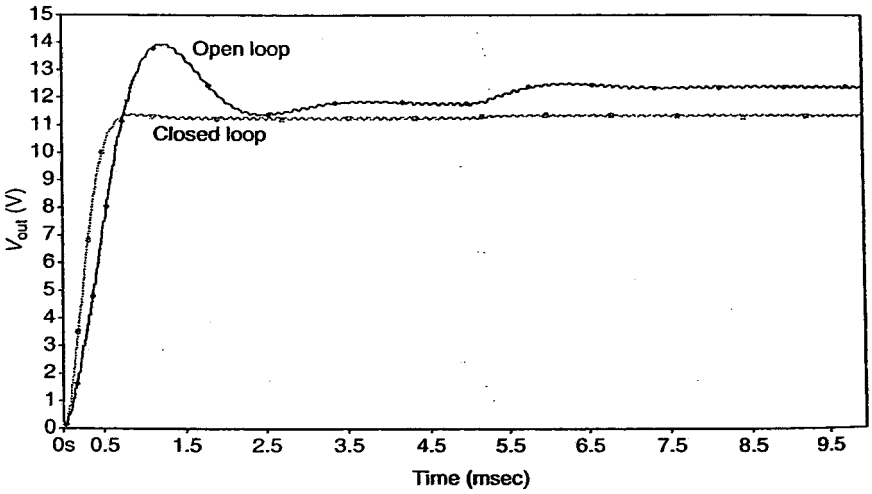


Figure 6.63 Transient response of the open-loop and closed-loop converters.

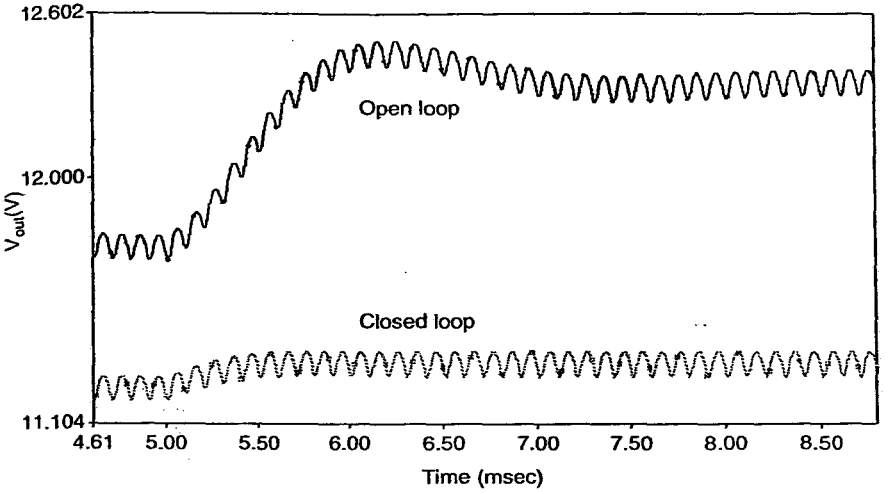


Figure 6.64 Expanded view of the transient at 5 msec.

unintentional generation of conducted or radiated energy. To preserve the integrity of the power source, an input EMI filter placed between the power source and the switching converter is often required. The major purpose of the input EMI filter is to prevent the input current waveform of the switching converter from interfering with the power source. As such, the major role of the input EMI filter is to optimize the mismatch between the power source and switching converter impedances [24].

There are two conduction modes of EMI: common and differential. Common mode EMI is that component of noise current which exists on any or all supply or output lines with respect to a common ground plane such as chassis or ground return bus. The capacitance of the switching transistor insulator mounted on the chassis or ground plane is known to be a "culprit" for the common mode-coupling path. Differential mode EMI, also known as longitudinal mode EMI, occurs between any two supply or output lines. A principal source of the differential mode emission is the impedance of the input EMI filter capacitor. Another source of differential mode emission is the switching devices. The magnitude and spectral content of the EMI are often dictated by the reverse recovery characteristics of these switching devices.

6.2.12.1 Stability Considerations

Figure 6.65 shows a circuit model for a buck converter with a second-order input EMI filter. As shown, the DC transformerized equivalent circuit

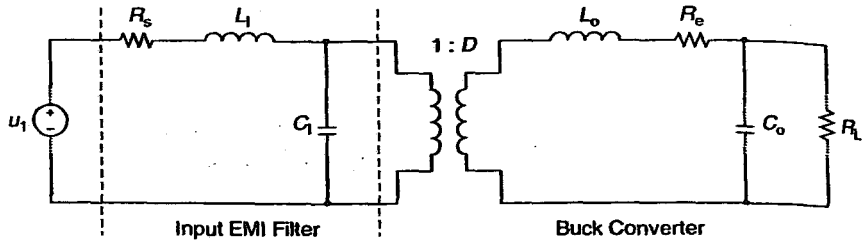


Figure 6.65 Circuit model of a buck converter with an input EMI filter.

of the buck converter shown in Figure 6.41 is used. The input EMI filter consists of an input EMI filter inductance, L_I, and an input EMI filter capacitance, C_I. For simplicity, the total effective impedance of the source, u_1, is modeled as a single effective source resistance, R_s. The effective source resistance, R_s, consists of the source impedance and the series resistance of the input EMI filter inductor. In general, the values for L_I and C_I are large enough to dominate the reactive impedance of the source. The output impedance of the second-order input EMI filter is given by

$$Z_{EMI} = \frac{R_s + j\omega L_I}{(1 - \omega^2 C_I L_I) + j\omega R_s C_I}. \tag{6.304}$$

By choosing L_I and C_I sufficiently large, the interfering signals at the switching frequency and its higher harmonics of the switching converter can be adequately attenuated.

The stability of a closed-loop switching converter with an input EMI filter can be found by comparing the output impedance of the input EMI filter to the input impedance of the switching converter. For a given load resistance, R_L, the controller adjusts the duty cycle to maintain a constant output voltage, and hence, a constant output power. Thus, if the input voltage increases, the input current must decrease to yield a constant input power. Consequently, the closed-loop switching converter exhibits a negative input impedance. The effective secondary-side impedance of the buck converter is

$$Z_b = R_L // \frac{1}{j\omega C_o} + j\omega L_o + R_e, \tag{6.305}$$

where R_e is an effective resistance that accounts for the series resistances in the output filter inductor and other components, and a "modulation" resistance that arises from the modulation of the switching transistor storage time [25]. It is a complicated function of these component resistances and

also of the duty cycle. From Figure 6.65, the input impedance of the closed-loop buck converter is the negative of the effective secondary-side impedance reflected through the DC transformer to its input at low frequencies. The input impedance of the buck converter is

$$Z_{in} = -\frac{[R_L//(1/j\omega C_o) + j\omega L_o + R_e]}{D^2}, \tag{6.306}$$

or

$$Z_{in} = -\frac{1}{D^2}\left(\left[\frac{R_L}{1+(\omega R_L C_o)^2} + R_e\right] + j\omega\left[L_o - \frac{R_L^2 C_o}{1+(\omega R_L C_o)^2}\right]\right), \tag{6.307}$$

where D is the duty cycle of the buck converter. At low frequencies, the input impedance is dominated by the output load resistance, R_L, and is given by

$$Z_{in} = -\frac{(R_L + R_e)}{D^2}. \tag{6.308}$$

At the resonant frequency of $1/2\pi\sqrt{L_o C_o}$, the input impedance is at its minimum and is given by

$$Z_{in} = -\frac{R_e}{D^2}. \tag{6.309}$$

Above the resonant frequency, the input impedance increases inductively as

$$Z_{in} = -\frac{j\omega L}{D^2}. \tag{6.310}$$

The input impedance of the buck converter versus frequency is illustrated in Figure 6.66. The switching converter negative input impedance in combination with the input EMI filter can under certain conditions constitute a negative resistance oscillator, and is the origin of the system potential instability. The input EMI filter output impedance is a small positive resistance at DC and low frequencies, but in the neighborhood of the filter resonant frequency its output impedance may be many times the associated Ohmic resistances, and if the magnitude of Z_{EMI} increases sufficiently that the net circuit resistance becomes negative, oscillation will occur [25]. As such, the maximum output impedance of the input EMI filter, $Z_{EMI,max}$, must be less than the magnitude of the input impedance of the switching converter to avoid instability [26]. Hence,

$$Z_{in} \gg Z_{EMI,max}. \tag{6.311}$$

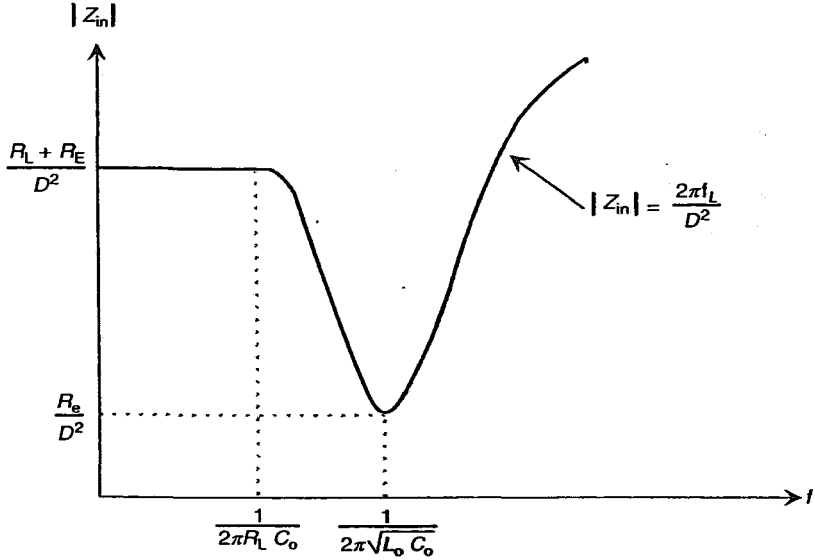


Figure 6.66 Input impedance versus frequency for a buck converter.

To ensure stability, however, the poles of $Z_{in}//Z_{EMI}$ should lie in the left-hand plane. The above stability condition is only valid if the input EMI filter resonant frequency is below the frequency at which the input impedance of the switching converter begins to deviate from its low-frequency values. Thus, instability tends to occur at the resonant frequency of the switching converter since the input impedance of the switching converter is at its minimum. Also, the worst case for stability is at low input voltage since it requires a larger duty cycle that decreases the input impedance of the switching converter.

The average power demand through the input EMI filter is practically constant for a constant switching converter load. Thus, the switching converter can be modeled as a continuous constant power element for low-frequency stability considerations [27], in accordance with the concept of state–space averaging as shown in Figure 6.67. The state variables are chosen as x_1 for the current flowing through the input EMI filter inductor and x_2 as the voltage across the input EMI filter capacitor. The state equations are

$$u_1 = R_s x_1 + L_1 \dot{x}_1 + x_2, \tag{6.312}$$

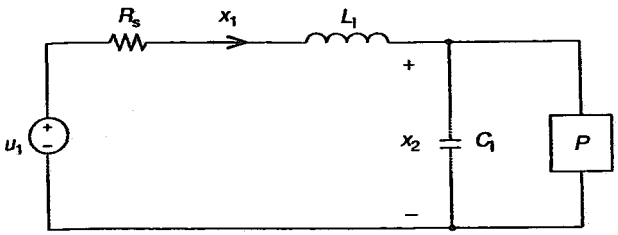


Figure 6.67 Circuit model of switching converter with an input EMI filter.

and

$$x_1 = C_1\dot{x}_2 + \frac{P}{x_2}. \tag{6.313}$$

Substituting x_1 from Equation (6.313) into Equation (6.312), we have

$$u_1 = R_s\left[C_1\frac{dx_2}{dt} + \frac{P}{x_2}\right] + L_1\left[C_1\frac{d^2x_2}{dt^2} - \frac{P}{x_2^2}\frac{dx_2}{dt}\right] + x_2. \tag{6.314}$$

or

$$\frac{u_1}{L_1C_1} = \frac{d^2x_2}{dt^2} + \left(\frac{R_s}{L_1} - \frac{P}{C_1x_2^2}\right)\frac{dx_2}{dt} + \frac{x_2}{L_1C_1}. \tag{6.315}$$

The term, $-(P/C_1x_2^2)$, is due to the negative input impedance of the constant power load of the switching converter. Routh–Hurwitz stability criterion can be used to determine the necessary and sufficient condition for stability from the sign and magnitude of the coefficients of the characteristic equation. From Routh–Hurwitz stability criterion, it requires that

$$R_s > \frac{PL_1}{C_1x_{2(\min)}^2}. \tag{6.316}$$

It is clear that the input EMI filter inductance should be much smaller than the input EMI filter capacitance. A resistance in series with the input EMI filter inductor can be added to improve stability. However, it is undesirable to increase the series resistance of the input EMI filter to improve stability since it increases conduction losses. The series resistance is normally chosen to be three to five times the characteristic impedance of the filter, $\sqrt{L_1/C_1}$. However, the quality factor, Q, of the input EMI filter increases as the series resistance decreases. Also, the maximum output impedance of the input EMI filter increases as the quality factor increases. In order to avoid

instability, it is necessary to utilize a low Q input EMI filter with the penalty of higher conduction losses.

The nonlinear resistance associated with the constant-power element of the switching converter can be replaced by a negative linear resistance, $-R_L$, defined by $-(x_2^2/P)$. Figure 6.68 shows an equivalent circuit of a switching converter with an input EMI filter. The state equations are

$$u_1 = L_1\dot{x}_1 + R_s x_1 + R_{esr}C_1\dot{x}_2 + x_2, \tag{6.317}$$

and

$$x_1 = C_1\dot{x}_2 + \frac{R_{esr}C_1\dot{x}_2 + x_2}{R_L}. \tag{6.318}$$

Combining, rearranging, and assuming that $R_L \ll R_s$ and $R_L \ll R_{esr}$, the state equations can also be expressed as

$$\dot{x}_1 = -\frac{(R_s + R_{esr})}{L_1}x_1 - \frac{1}{L_1}x_2 + \frac{1}{L_1}u_1, \tag{6.319}$$

and

$$\dot{x}_2 = \frac{1}{C_1}x_1 - \frac{1}{R_L C_1}x_2. \tag{6.320}$$

These state equations can be written in matrix form as

$$\begin{bmatrix}\dot{x}_1\\ \dot{x}_2\end{bmatrix} = \begin{bmatrix}-((R_s + R_{esr})/L_1) & -(1/L_1)\\ 1/C_1 & -(1/R_L C_1)\end{bmatrix}\begin{bmatrix}x_1\\ x_2\end{bmatrix} + \begin{bmatrix}1/L_1\\ 0\end{bmatrix}u_1. \tag{6.321}$$

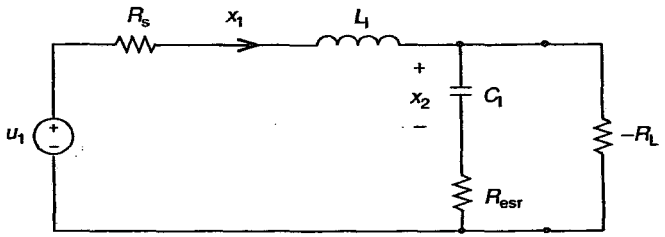


Figure 6.68 Equivalent circuit of a switching converter with an input EMI filter.

Then

$$\begin{bmatrix} x_1(s) \\ x_2(s) \end{bmatrix} = \frac{\begin{bmatrix} s+(1/R_L C_1) & 1/L_1 \\ -(1/C_1 & s+((R_s+R_{esr})/L_1) \end{bmatrix} \begin{bmatrix} 1/L_1 \\ 0 \end{bmatrix} u_1}{s^2+(((R_s+R_{esr})/L_1)+(1/R_L C_1))s+(1/L_1 C_1)}. \quad (6.322)$$

Routh–Hurwitz stability criterion required that

$$\frac{R_s+R_{esr}}{L_1}+\frac{1}{R_L C_1}>0. \quad (6.323)$$

In practice, the input EMI filter with LR reactive damping shown in Figure 6.69 is used to reduce conduction losses. This filter has a −40 dB/decade roll off beyond its resonant frequency at the expense of output impedance higher than its characteristic impedance. The Routh–Hurwitz stability criterion for this filter is [27]

$$\left(\frac{R_d}{L_d}-\frac{1}{R_L C_1}\right)\left(\frac{L_1+L_d}{L_1}-\frac{R_d}{R_L}\right)>\frac{R_1}{L_1}. \quad (6.324)$$

Figure 6.70 shows an input EMI filter with RC reactive damping. The damping capacitor, C_d, is usually chosen to be three times the filter capacitance, C_1, to avoid the filter inductor, L_1, from resonating with the damping capacitor at resonance. The damping resistor, R_d, can be made to be equal to the characteristic impedance of the filter. As such, the RC reactive damped input EMI filter requires the use of a more expensive and bulky damping capacitor compared to the damping inductor of the LR reactive damped filter. However, the output impedance of the RC damped filter is generally lower than the characteristic impedance of the filter. In this configuration

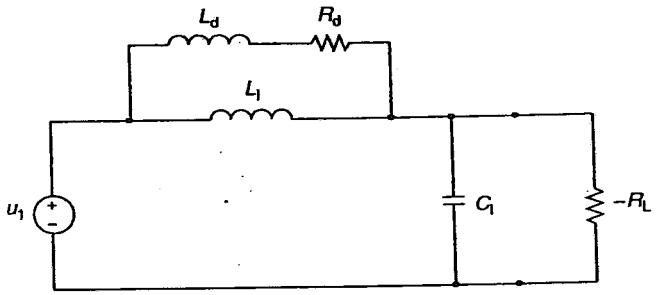


Figure 6.69 Input EMI filter with LR reactive damping.

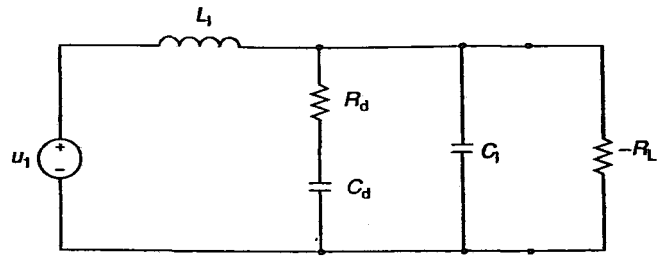


Figure 6.70 Input EMI filter with RC reactive damping.

the capacitor is normally chosen with an ESR equal to R_d. The Routh–Hurwitz stability criterion for this filter is [27]

$$C_d\left(1-\frac{R_d}{R_L}\right)\left(R_dC_d-\frac{L_1}{R_L}\right)>\frac{L_1C_1}{R_L}. \tag{6.325}$$

The second-order input EMI filter may not provide sufficient attenuation and/or roll-off beyond the resonant frequency. A fourth-order filter with LR reactive damping shown in Figure 6.71 may be used to increase attenuation and roll-off beyond its resonant frequency. It is a good design practice to have different resonant frequencies for the two sections of the filter to avoid a sharp maximum in its output impedance and a sharp minimum in its input impedance at the resonant frequency. It should be noted that high-core losses in the input EMI filter inductor is desirable to dissipate the energy at the EMI frequency so as to prevent it from reflecting back to the power source. Otherwise, the EMI current would radiate and/or couple into other circuitry.

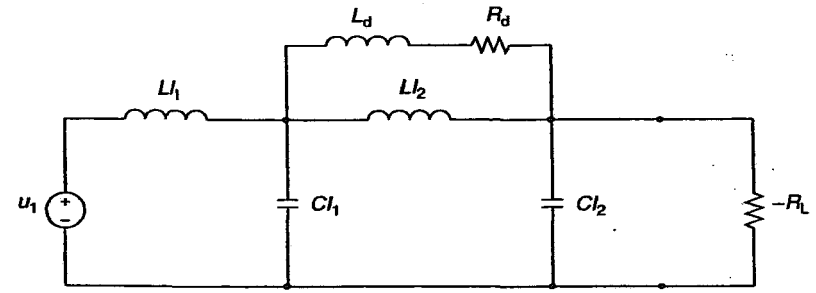


Figure 6.71 A fourth-order input EMI filter with LR reactive damping.

Example 6.7. The parameters for a buck converter are: input voltage = 10 V, average output voltage = 5 V, switching frequency = 1 kHz, $L_o = 1$ mH, $C_o = 100\ \mu$F, $R_e = 0.01\ \Omega$, and $R_L = 5\ \Omega$. The input EMI filter has the following parameters: $L_I = 1$ mH, $C_I = 1000\ \mu$F, and $R_s = 0.001\ \Omega$. Plot the input impedance of the switching converter and the output impedance of the input EMI filter on the same plot. Determine if a potential stability problem exists.

Solution. The magnitude of the input impedance of the buck converter can be expressed as

$$|Z_{in}|(\omega) = \frac{1}{D^2}\sqrt{\left(\frac{R_L}{1+(\omega R_L C_o)^2} + R_e\right)^2 + \omega^2\left(L_o - \frac{R_L^2 C_o}{1+(\omega R_L C_o)^2}\right)^2},$$

and the magnitude of the output impedance of the input EMI filter can be expressed as

$$Z_{EMI}(\omega) = \sqrt{\frac{R_s^2 + (\omega L_I)^2}{(1-\omega^2 C_I L_I)^2 + (\omega R_s C_I)^2}}.$$

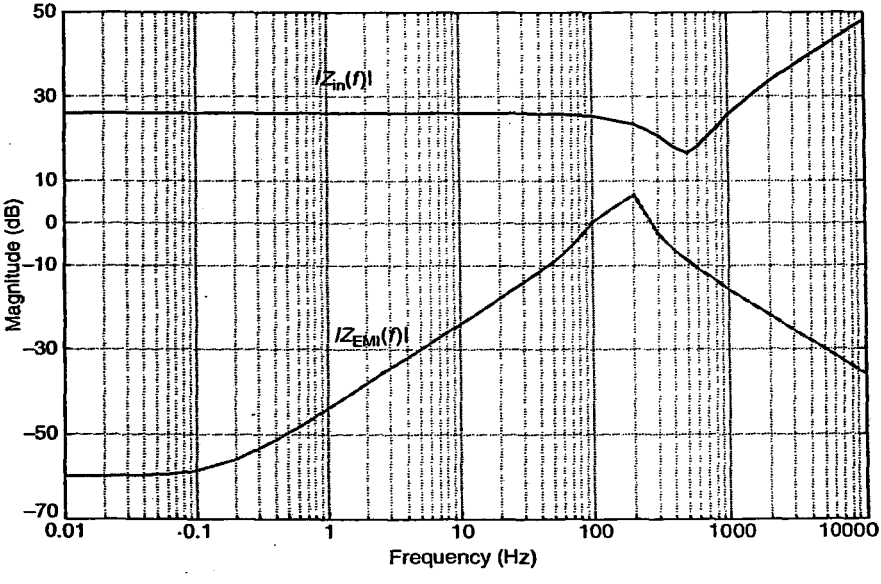


Figure 6.72 Input impedance, $Z_{in}(f)$, of the buck converter and output impedance, $Z_{EMI}(f)$, of the input EMI filter.

Figure 6.72 shows the input impedance of the buck converter and output impedance of the input EMI filter. As shown, the magnitude of the input impedance of the buck converter is always larger than the magnitude of the output impedance of the input EMI filter. Thus, the buck converter with the input EMI filter is stable.

6.3 DISCRETE-TIME MODELS

6.3.1 Introduction

A discrete-time model for a switching converter will be developed based on the continuous-time small-signal model. The discrete-time model is more precise than its continuous-time model and it can be implemented using a digital controller. Both voltage-mode and current-mode control schemes are discussed.

6.3.2 Continuous-Time and Discrete-Time Domains

For the continuous-time system of the form

$$\dot{x} = \bar{A}x(t) + \bar{B}u(t) \tag{6.326}$$

the solution for the differential equation (6.326) in the time domain can be expressed as

$$x(t) = e^{At}x(t_o) + \int_{t_o}^{t} e^{A(t-\tau)}Bu(\tau)d\tau. \tag{6.327}$$

The above equation is an exact representation of the continuous-time system. It implies that the state at the instant t depends only on the state at the time t_o and the convolution of the inputs and the transition matrix, considering the values of the states in between. The evaluation of the integral can be simplified by approximating e^{At} with only the first two terms from its Taylor series:

$$e^{At} = \underbrace{I + At}_{} + A^2t^2 2! + \cdots.$$

Also, assume that $u(t) = u$ is constant over the integration interval and $t_o = 0$, Thus:

$$\int_{t_o}^{t} e^{A(t-\tau)}Bu(\tau)d\tau = \int_{t_o}^{t} e^{At}e^{-A\tau}Bu\, d\tau \Leftrightarrow$$

$$\int_{t_o}^{t} e^{A(t-\tau)}Bu(\tau)d\tau = e^{At}\int_{t_o}^{t} e^{-A\tau}Bu\,d\tau \Leftrightarrow$$

$$\int_{t_o}^{t} e^{A(t-\tau)}Bu(\tau)d\tau = e^{At}Bu\left[A^{-1}\left(-e^{-A\tau}\right)\right]\Big|_{t_o}^{t} \Leftrightarrow$$

$$\int_{t_o}^{t} e^{A(t-\tau)}Bu(\tau)d\tau = e^{At}Bu\left[I - e^{-At}\right]A^{-1}$$

if the matrix A is invertible.

Rearranging the above equation

$$\int_{t_o}^{t} e^{A(t-\tau)}Bu(\tau)d\tau = \left[e^{At} - I\right]A^{-1}Bu.$$

Replacing e^{At} with its approximate value,

$$\int_{t_o}^{t} e^{A(t-\tau)}Bu(\tau)d\tau = [I + At - I]A^{-1}Bu.$$

Then, the solution of the differential Equation (6.326) in the continuous-time domain can be approximated as

$$x(t) \approx e^{At}x(t_o) + tBu(t_o). \tag{6.328}$$

Making $t_o = (n + D)T_s$ and $t = (n + 1 + D)T_s$, results in the discrete-time expression:

$$x[(n+1+D)T_s] = e^{AT_s}x[(n+D)T_s] + T_sBu[(n+D)\cdot T_s]. \tag{6.329}$$

6.3.3 Continuous-Time State–Space Model

Switching converters are nonlinear and time-invariant circuits. Different linear models have been developed to describe the small-signal behavior of the switching converters [1,4–8,16,28]. Suppose that the converter is operating in the continuous-conduction mode with a constant switching frequency $f_s = (1/T_s)$. Let the circuit topology be A_1 during the interval when the main

switch is on (i.e., t_{on}). When the main switch is turned off (i.e., t_{off}), the circuit topology changes to A_2. Writing the circuit equations in matrix form, we obtain the state–space representation of the system:

$$\dot{x}(t) = Ax(t) + Bu(t). \tag{6.330}$$

Because the system has two different topologies during t_{on} and t_{off}, the converter is characterized by two sets of state equations. During t_{on} corresponding to the nth switching period, $nT_s < t < (n + d_n)\,T_s$, the state equation is:[4]

$$\dot{x} = A_1x + B_1u. \tag{6.331}$$

By analogy, during t_{off}, $(n + d_n)\,T_s < t < (n + 1)T_s$, the state equation becomes

$$\dot{x} = A_2x + B_2u, \tag{6.332}$$

where d_n is the *duty cycle*.

A small-signal model of the converter can be found by following the steps described in Brown and Middlebrook [2], where the switching functions in Equations (6.333) and (6.334) help to combine the two sets of equations into one single equation:

$$d(t) = \begin{cases} 1 & \text{if } nT_s < t < (n + d_n)T_s \\ 0 & \text{if } (n + d_n)T_s < t < (n + 1)T_s, \end{cases} \tag{6.333}$$

$$d'(t) = 1 - d(t). \tag{6.334}$$

Then

$$\dot{x} = (d(t)A_1 + d'(t)A_2)x + (d(t)B_1 + d'(t)B_2)u. \tag{6.335}$$

Notice that if the duty cycle d_n is constant, then Equation (6.335) is linear with periodic coefficients. However, if d_n is used as the control variable, Equation (6.335) will be nonlinear because the duty cycle will be a function of the state variables. Nevertheless, it is possible to obtain a linear model if the perturbations on the duty cycle are kept small.

The source variable and duty cycle can be represented by a nominal value (noted in capital letters) plus a perturbation term (noted in lowercase with '^'). Consider the source variable as

---

[4] To simplify the notation, the temporal dependency of the variables will be omitted unless it may lead to confusion. Thus, for example, $\dot{x}(t)$ will be written as $\dot{x}$.

$$u = V_s + \hat{v}_s. \tag{6.336}$$

The duty cycle is

$$d_n = D + \hat{d}_n \tag{6.337}$$

The switching functions can also be described by a steady-state part, $\bar{d}(t)$, plus a perturbation, $\hat{d}(t)$, such that

$$d = \bar{d} + \hat{d} \quad \text{and} \quad d' = 1 - d, \tag{6.338}$$

which are defined as

$$\bar{d}(t) = \begin{cases} 1 & \text{if } nT_s < t < (n+D)T_s \\ 0 & \text{if } (n+D)T_s < t < (n+1)T_s \end{cases} \tag{6.339}$$

and

$$\hat{d}(t) = \begin{cases} \text{sgn}(d_n - D) & \text{if } t \in [(n+D)T_s, (n+d_n)T_s] \\ 0 & \text{otherwise} \end{cases}, \tag{6.340}$$

where sgn() is the sign function. The last two equations model the effect of a perturbation on the duty cycle.

Similarly, the state vector can be represented by a time-variant steady-state part plus a perturbation:

$$x = \bar{x} + \hat{x}. \tag{6.341}$$

Replacing the above equation in the state equation results in an expression describing the steady-state and perturbation responses. Making the perturbations equal to zero, the *steady-state equation* (6.335) is obtained:

$$\dot{\bar{x}} = (\bar{d}A_1 + \bar{d}'A_2)\bar{x} + (\bar{d}B_1 + \bar{d}'B_2)V_s. \tag{6.342}$$

Subtracting the steady-state response from the full response results in the expression for the *perturbation in the state vector*. This expression can be linearized assuming that the perturbations are small enough that the product of perturbations is negligible:

$$\begin{aligned} \dot{\hat{x}} = {} & [\bar{d}A_1 + \bar{d}'A_2]\hat{x} \\ & + [\bar{d}B_1 + \bar{d}'B_2]\hat{v}_s + [(A_1 - A_2)\bar{x} + (B_1 - B_2)V_s]\hat{d}. \end{aligned} \tag{6.343}$$

Finally, the function $\hat{d}(t)$ can be approximated using a string of *delta* functions having the appropriate areas, as shown in Brown and Middlebrook [2]:

$$\hat{d} \simeq \hat{p}(t) = \sum_{n=-\infty}^{\infty} \left(\hat{d}_n T_s\right) \delta[t - (n + D)T_s]. \tag{6.344}$$

6.3.4 Discrete-Time Model of the Switching Converter

In this section, a *discrete model* of the switching converter is obtained by integration of the continuous state-space equation (6.343) over a switching period. The discrete model describes the small-signal behavior of the converter only at *one* time instant during each cycle, saying nothing about what happens in between. Since the starting point of the integration is arbitrary, it is convenient to choose the time when the state vector is used to calculate the duty cycle. This time may depend on the implementation. We choose the instant $(n + D)T_s$ as the starting point of the integration, where the inductor current is at its maximum value. During the interval, $[(n + D)\ T_s, (n + 1)\ T_s]$, the switching functions are $\bar{d} = 0$ and $\bar{d}' = 1$. Thus

$$\dot{\hat{x}} = A_2\hat{x} + B_2\hat{v}_s + K\hat{d}_n T_s \delta[t - (n + D)T_s], \tag{6.345}$$

where

$$K = (A_1 - A_2)\bar{x}[(n + D)T_s] + (B_1 - B_2)V_s. \tag{6.346}$$

Since the δ function is nonzero only at $(n + D)T_s$, the integration yields

$$\hat{x}[(n + 1)T_s] = e^{A_2 D' T_s} e^{A_2 D' T_s} \hat{x}[(n + D)T_s] + e^{A_2 D' T_s} K T_s \hat{d}_n + \int_{(n+D)T_s}^{(n+1)T_s} e^{A_2[(n+1)T_s - \tau]} B_2 \hat{v}_s d\tau. \tag{6.347}$$

Assume that no perturbations are present on the input voltage during the integration interval, then $\hat{v}_s = 0$. Therefore, the last term of Equation (6.347) is also equal to zero. This approximation implies that the input voltage is not considered as a perturbation input; as such, it does not affect the stability analysis.

By analogy, during the interval $[(n + 1)T_s, (n + 1 + D)T_s]$ the state equation is

$$\dot{\hat{x}} = A_1\hat{x}. \tag{6.348}$$

To evaluate the integral over this interval, the value for the state vector at the end of the previous period, $\hat{x}[(n + 1)T_s]$ is used as the initial condition, yielding

$$\hat{x}[(n + 1 + D)T_s] = e^{A_1 DT_s} e^{A_2 D'T_s} \hat{x}[(n + D)T_s] + e^{A_1 DT_s} e^{A_2 D'T_s} K T_s \hat{d}_n. \tag{6.349}$$

Notice that the transition matrix

$$\Phi = e^{A_1 DT_s} e^{A_2 D'T_s} \tag{6.350}$$

depends on the switching frequency.

Equation (6.349) describes the state vector at the instant $(n + 1 + D)\,T_s$ as a function of the initial state $\hat{x}[(n + D)\,T_s]$ and the small-signal perturbation of the duty cycle with duration $\hat{d}_n T_s$.

A discrete model for a general switching converter has been developed. This model allows us to evaluate the behavior of the system for a small-signal variation on the duty cycle $\hat{d}_n$.

Example 6.8. Find the discrete-time model for the synchronous buck converter of Figure 2.10.

Solution. Figure 6.73 and Figure 6.74 represent the two equivalent circuits for the synchronous buck converter during t_{on} and t_{off}, respectively. R_L includes the resistance of the inductor's winding and the current-sensing resistor. R_{on} is the on resistance of the switching devices.

To develop the state–space model, the state variables are selected to be the current flowing through the inductor and the voltage across the capacitor. Then, the state–space model is

$$x = \begin{bmatrix} i_L \\ v_c \end{bmatrix} \tag{6.351}$$

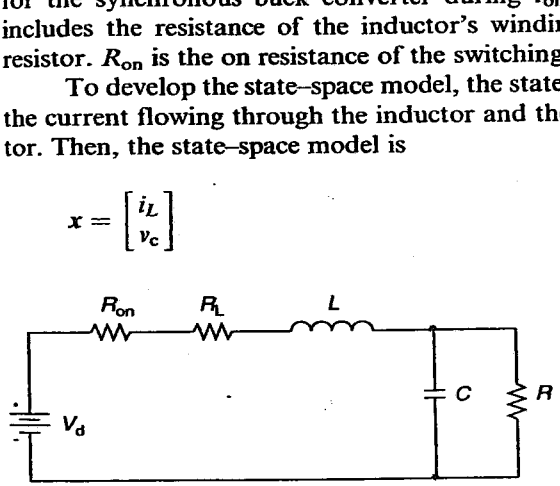


Figure 6.73 Equivalent circuit during t_{on}: A_1.

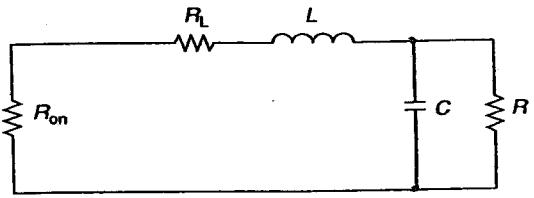


Figure 6.74 Equivalent circuit during t_{off}: A_2.

$$A = \begin{bmatrix} -\dfrac{R_{on}+R_L}{L} & -\dfrac{1}{L} \\ \dfrac{1}{C} & -\dfrac{1}{RC} \end{bmatrix}, \tag{6.352}$$

$$B_1 = \begin{bmatrix} \dfrac{1}{L} \\ 0 \end{bmatrix}, \qquad B_2 = \begin{bmatrix} 0 \\ 0 \end{bmatrix}. \tag{6.353}$$

For a synchronous buck converter, $A_1 = A_2 = A$ then the discrete-time model is

$$\hat{x}[(n+1)T_s] = e^{AT_s}\hat{x}[nT_s] + e^{AT_s}KT_s\hat{d}_n \tag{6.354}$$

and

$$K = B_1 V_s. \tag{6.355}$$

6.3.5 Design of a Discrete Control System with Complete State Feedback

Consider a plant that has been made discrete in time, having the following difference equation:

$$x(n+1) = Ax(n) + Bu(n).$$

The usual technique in control systems consists of generating the control strategies based on measurements of the system states. In case of a voltage regulator, for example, the most commonly used feedback technique is proportional to the state. This can be of the form $u(n) = -Fx(n)$, then:

$$x(n+1) = (A - FB)x(n)$$

For this kind of system, the closed-loop eigenvalues are found by solving the characteristic equation:

$$\det[zI - A + FB] = 0.$$

Notes:

- If the state vector has dimension i and the control has dimension j, the matrix F will have $i \times j$ elements.
- If the system described by (A, B) is controllable, the choice of the elements of F will control the position of the closed-loop poles on the z-plane.
- If the elements of F are real, the closed-loop poles will be real or complex conjugates.
- If the applied control is a scalar such as in a switching converter, the resulting F is a row vector, having i elements. The elements of F are unique if the i roots of the characteristic equations are specified.
- The closed-loop poles can be arbitrarily placed by choosing the elements of F.

6.3.5.1 Pole Selection

One way of choosing the closed-loop poles is to select an ith order low-pass Bessel filter, where i is the order of the system that is designed for the transfer function [21]. The step response of a Bessel filter has no overshoot, thus it is suitable for a voltage regulator. The desired filter can then be selected for a step response that meets a specified settling time. The minimum settling time should be chosen such that the control variable should not saturate.

There are two possibilities in choosing the closed-loop poles; the first is to design an analog filter that meets the continuous-time specifications, and then map the poles into the z-plane. The other possibility is to design a discrete filter with the right specifications. The filters can be designed with the aid of the filter toolbox that comes with MATLAB or with any other filter package, like Filter Wiz.

If the poles are chosen in the s domain, as for example $P_s = \{s_1, s_2\}$, the mapping into the z plane can be performed using $p_z = e^{p_s T_s}$, resulting in $P_z = \{z_1, z_2\}$.

6.3.5.2 Feedback Gains

The values for the elements of the feedback vector L of the discrete model can be obtained by pole placement. The MATLAB command $L = \text{PLACE}(\Phi_d, \Gamma_d, P)$ computes a state-feedback matrix L, such that the eigenvalues of $\Phi_d - \Gamma_d * L$ are those specified in vector P.

6.3.6 Voltage Mode Control

In Equation (6.354), the control input is $\hat{d}_n$. It is necessary to derive an approximate expression for $\hat{d}_n$ as a function of the state variables and the

control variable, $\hat{v}_{ref}$, used in voltage-mode control. This was calculated in Equation (6.3) as

$$\hat{d} = \frac{D}{V_{ref}} \hat{v}_{ref}. \tag{6.356}$$

The discrete-time model for a switching converter is given by Equation (6.349), repeated here for convenience,

$$\hat{x}[(n+1)T_s] = e^{A_1 DT_s} e^{A_2 D'T_s} \hat{x}[nT_s] + e^{A_1 DT_s} e^{A_2 D'T_s} K T_s \hat{d}_n. \tag{6.357}$$

This can be written as:

$$\hat{x}[(n+1)T_s] = \Phi \hat{x}[nT_s] + \Gamma \hat{d}_n, \tag{6.358}$$

where

$$\begin{cases} \Phi = e^{A_1 DT_s} e^{A_2 D'T_s} \\ \Gamma = \Phi K T_s \\ K = (B_1 - B_2) V_s. \end{cases} \tag{6.359}$$

Replacing $\hat{d}_n$ from Equation (6.356) into Equation (6.358), we obtain

$$\hat{x}[(n+1)T_s] = \Phi \hat{x}[nT_s] + \Gamma \frac{D}{V_{ref}} \hat{v}_{ref}. \tag{6.360}$$

If full-state feedback is applied and the system is controllable, then the closed-loop poles can be arbitrarily placed to obtain a desired transient response. The negative feedback proportional to the states on $\hat{v}_{ref}$ is:

$$\hat{v}_{ref} = -F \hat{x}[nT_s]. \tag{6.361}$$

The elements of the vector F are real numbers that weigh the perturbation of each state variable and determine the closed-loop poles of the system. Replacing the expression found for $\hat{v}_{ref}$ in the system model:

$$\hat{x}[(n+1)T_s] = \left[\Phi - \Gamma \frac{D}{V_{ref}} F \right] \hat{x}[nT_s]. \tag{6.362}$$

Then the expression in square bracket in the right-hand side of Equation (6.362) is the closed-loop matrix of the system:

$$\Phi_{CL} = \left[\Phi - \Gamma \frac{D}{V_{ref}} F \right]. \tag{6.363}$$

Then, Equation (6.362) can be written as:

$$\hat{x}[(n+1)T_s] = \Phi_{CL}\hat{x}[nT_s]. \tag{6.364}$$

Thus, the closed-loop poles can be arbitrarily placed by the right choice of the elements of the vector F. Therefore, with this control strategy; it is possible to choose a desired transient response.

6.3.6.1 Extended-State Model for a Tracking Regulator

A voltage regulator for the voltage-mode converter was developed in Section 6.3.6. This controller was calculated under a constant-current load. Our interest is to develop a mechanism that would allow the controller to track load changes and then, update the reference to the new load state; to do so, additional dynamics are added. Figure 6.75 represents a digital tracking system that uses a full-state feedback. The additional dynamics are represented by Φ_a, Γ_a, and L_2 [21].

A state equation for the design model shown in Figure 6.75 can be obtained by defining a composite state vector:

$$x_d[n] = \begin{bmatrix} i_L[n] \\ v_c[n] \\ x_a[n] \end{bmatrix},$$

where x_a is the state vector of the added dynamics. Then, using the formula for the cascade connection of two state–space systems, the state–space description of the design plant is

$$\Phi_d = \begin{bmatrix} \Phi & 0 \\ \Gamma_a c & \Phi_a \end{bmatrix}, \Gamma_d = \begin{bmatrix} \Gamma \\ 0 \end{bmatrix}, \tag{6.366}$$

where c relates the output to the states through $y = cx$.

A regulator for (Φ_d, Γ_d) can be designed and the vector of feedback gains can be partitioned as

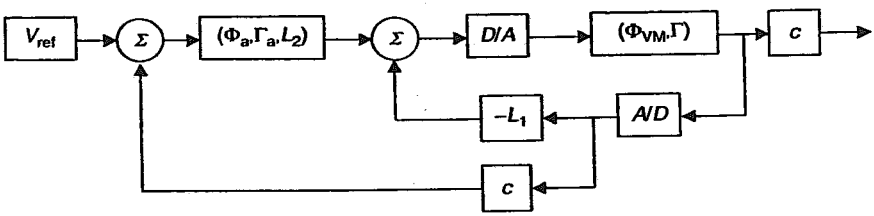


Figure 6.75 Digital tracking system with full-state feedback.

$$L = [L_1 \quad L_2] \tag{6.367}$$

where L_1 consists of the first n_e elements of L, where n_e is the order of the system to be controlled. L_2 is the remainder of L that relates the output to the states through $y_a = L_2 x_a$. L can be found by pole location of the closed-loop regulator. The procedure to find (Φ_a, Γ_a) is covered in detail in Vaccaro [21]. The main advantage of this configuration is that if the actual closed-loop system is stable, the actual system will track the reference input with a zero steady-state error. This is a desired feature in voltage regulators.

A complete design example of a voltage-mode synchronous buck converter with digital control is given in Chapter 10.

6.3.7 Current Mode Control

To apply current-mode control to the synchronous buck converter, $\hat{d}_n$ from Equation (6.354) has to be written as a function of the state variables and the control variable $\hat{I}_p$. This expression was found previously, as Equation (6.6), and re-written here as equation (6.368)

$$\hat{d}_n = \frac{\partial d_n}{\partial x_1}\hat{x}_1 + \frac{\partial d_n}{\partial x_2}\hat{x}_2 + \frac{\partial d_n}{\partial I_p}\hat{I}_p, \tag{6.368}$$

where

$$x_1 = i_L, \quad x_2 = v_C. \tag{6.369}$$

Then

$$\hat{d}_n = \frac{\partial d_n}{\partial i_L}\hat{i}_L + \frac{\partial d_n}{\partial v_c}\hat{v}_c + \frac{\partial d_n}{\partial I_p}\hat{I}_p. \tag{6.370}$$

The sensitivities in Equation (6.370) are given by Equations (6.10), (6.18), and (6.22) as

$$\hat{d}_n = -\frac{L}{(V_d - V_c)T_s}\hat{i}_L, \tag{6.371}$$

$$\hat{d}_n = \frac{D}{V_d - V_c}\hat{v}_c, \tag{6.372}$$

and

$$\hat{d}_n = \frac{L}{(V_d - V_c)T_s}\hat{I}_p. \tag{6.373}$$

Let

$$\omega_1 = \frac{\partial d_n}{\partial x_1},\ \omega_2 = \frac{\partial d_n}{\partial x_2},\ \omega_3 = \frac{\partial d_n}{\partial I_p},\ \text{and}\ \Omega = [\omega_1\ \omega_2]. \tag{6.374}$$

Replacing Equation (6.374) in Equation (6.370) yields:

$$\hat{d}_n = \underbrace{\begin{bmatrix}\omega_1 & \omega_2\end{bmatrix}\begin{bmatrix}\hat{i}_L \\ \hat{v}_c\end{bmatrix}}_{\hat{d}_{CM}} + \underbrace{\omega_3 \hat{I}_p}_{\hat{d}_F}. \tag{6.375}$$

Thus, the perturbation on the duty cycle, $\hat{d}_n$, can be expressed as the sum of a part due to the current-mode and another part due to the feedback:

$$\hat{d}_n = \hat{d}_{CM} + \hat{d}_F. \tag{6.376}$$

The discrete-time model equation for a switching converter was found in Equation (6.358) to be:

$$\hat{x}[(n+1)T_s] = \Phi\hat{x}[nT_s] + \Gamma\hat{d}_n. \tag{6.377}$$

This can be written as

$$\hat{x}[(n+1)T_s] = \Phi\hat{x}[nT_s] + \Gamma\left(\hat{d}_{CM} + \hat{d}_F\right). \tag{6.378}$$

Thus

$$\hat{x}[(n+1)T_s] = \Phi\hat{x}[nT_s] + \Gamma\Omega\hat{x}[nT_s] + \Gamma\omega_3\hat{I}_p. \tag{6.379}$$

By grouping the terms corresponding to the current-mode, the above equation can be written as:

$$\hat{x}[(n+1)T_s] = \Phi_{CM}\hat{x}[nT_s] + \Gamma\omega_3\hat{I}_p. \tag{6.380}$$

Then the system matrix in current-mode is

$$\Phi_{CM} = \Phi + \Gamma\Omega. \tag{6.381}$$

This equation states that when the converter is operating in the current-mode, the dynamic of the system differs from that of the open-loop due to the inherent feedback represented by $\Gamma\Omega$. This contribution may lead to current-mode instability in some switching converters [28,29].

For a lossless synchronous buck converter, the poles of Φ_{CM} lie inside of the unit circle for $D < 0.5$ and outside the unit circle for $D > 0.5$. If full-state feedback is applied and the system is controllable, then the closed-loop poles can be arbitrarily placed to stabilize the system and to obtain a desired transient response. The negative feedback proportional to the states on $\hat{I}_p$ is

$$\hat{I}_p = -F\hat{x}[nT_s]. \tag{6.382}$$

Replacing the expression found for I_p in the system model

$$\hat{x}[(n+1)T_s] = [\Phi_{CM} - \omega_3 \Gamma F]\hat{x}[nT_s]. \tag{6.383}$$

Then the expression in square brackets in the second term is the closed-loop matrix of the system:

$$\Phi_{CL} = [\Phi_{CM} - \omega_3 \Gamma F] \tag{6.384}$$

and

$$\hat{x}[(n+1)T_s] = \Phi_{CL}\hat{x}[nT_s]. \tag{6.385}$$

The closed-loop poles can be arbitrarily placed by a judicial choice of the elements of the vector F. Therefore, with this control strategy, it is possibly to stabilize the current-mode converter under a constant load, even for duty cycles greater than 50%. As was mentioned before, the converter operating with a duty cycle greater than 50% is unstable in the open-loop configuration.

6.3.7.1 Extended-State Model for a Tracking Regulator

A voltage regulator for the current-mode switching converter was developed in Section 6.3.7. This controller was calculated under a constant current load. Our interest is to develop a mechanism that would allow the controller to track load changes and then update the reference to the new load state. To do so, additional dynamics are added, as shown in Figure 6.76, which represents a digital tracking system that uses full-state feedback. The additional dynamics are represented by Φ_a, Γ_a, and L_2. L_2 relates the output of the additional block to its states through $y_a = L_2 x_a$.

A state equation for the design model in Figure 6.76 can be obtained by defining a composite state vector:

$$x_d[n] = \begin{bmatrix} i_L[n] \\ v_c[n] \\ x_a[n] \end{bmatrix}, \tag{6.386}$$

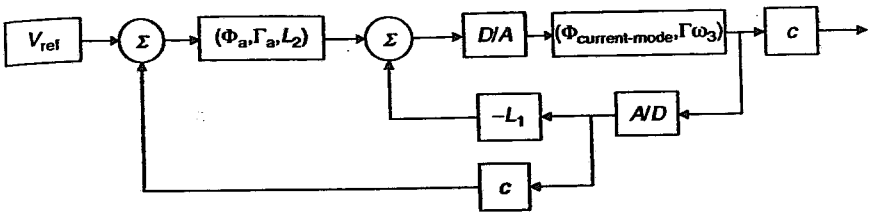


Figure 6.76 Digital tracking system with full-state feedback.

where x_a is the state vector of the added dynamics. Then, using the formula for the cascade connection of two state–space systems, the state–space description of the design plant is

$$\Phi_d = \begin{bmatrix} \Phi_{CM} & 0 \\ \Gamma_a c & \Phi_a \end{bmatrix}, \Gamma_d = \begin{bmatrix} \Gamma \\ 0 \end{bmatrix}, \tag{6.387}$$

where c relates the output to the states through $y = cx$.

A regulator for (Φ_d, Γ_d) can be designed and the vector of feedback gains can be partitioned as

$$L = [L_1 \quad L_2] \tag{6.388}$$

where L_1 consists of the first n_e elements of L, and n_e is the order of the system to be controlled (for a synchronous buck converter $n_e = 2$). L_2 is the remainder of L. L can be found by the pole location of the closed-loop regulator. The procedure to find (Φ_a, Γ_a) is covered in detail in Vaccaro [21]. The main advantage of this configuration is that if the closed-loop system is stable, it will track the reference input with a zero steady-state error. This feature is desirable in the operation of voltage regulators. A complete design example of a synchronous buck converter with digital control is given in Chapter 10.

PROBLEMS

6.1. The output filter shown in Figure 6.13 has a $R_{esr}C_o$ product of 60×10^{-6} Ω-F. The values for the inductor and load resistance are 10 mH and 10 Ω, respectively. Determine (a) the filter corner frequency, f_o, (b) the zero introduced by the equivalent series resistance, R_{esr}, (c) the magnitude in dB at $10f_o$, (d) the phase angle in degrees at $10f_o$, and (e) state whether the output response is critically damped, underdamped, or overdamped.

6.2. The compensation network shown in Figure 6.22 has a zero at 1 kHz and a pole at 5 kHz. The gain of the compensation network at 4 kHz is 4. Determine (a) values for C_1, C_2, R_1, and R_2, (b) the phase lag introduced by the compensation network, and (c) the phase shift introduced by the compensation network and the error amplifier.

6.3. The compensation network shown in Figure 6.25 has a double-zero at 1 kHz, a pole at 10 kHz, and a pole at 30 kHz. The gain at the double zero is 0 dB. Assuming that R_1 is 10,000 Ω, determine: (a) values for C_1, C_2, C_3, R_2, and R_3, and (b) the phase lag introduced by the compensation network.

6.4. The buck converter shown in Figure 6.30 has the following parameters: $V_s = 12$ V, $V_a = 5$ V, $L_o = 100$ μH, $C_o = 100$ μF, $R_{esr} = 0.001$ Ω, $R_3 = 100$ kΩ, $R_4 = 100$ kΩ, and $f_s = 20$ kHz. If the peak amplitude of the sawtooth signal is 3 V and the unity-gain crossover frequency of the closed-loop buck converter is 5 kHz, design the compensation network (i.e., Z_1 and Z_2) for a phase margin of 45°.

6.5. The gain of the error amplifier of a closed-loop buck converter at the unity-gain crossover frequency of 5 kHz is 20 dB. The rate of roll-off of the open-loop magnitude response at the unity-gain crossover frequency is −40 dB/decade. The output filter capacitance and inductance are 1000 μF and 1 mH, respectively. Determine the phase lag required to be contributed by its compensation network and error amplifier.

6.6. Develop a linearized equivalent circuit that preserves the input and output circuits of a Cûk converter.

6.7. Develop a linearized equivalent circuit that preserves the input and output circuits of a buck–boost converter.

6.8. Obtain the output impedance, $X_2(s)/U_2(s)$, for a boost converter having an R_{esr} in the output capacitor.

6.9. Obtain an open-loop transfer function, $G(s)\,H(s)$, for a boost converter that has an R_{esr} in its output capacitor.

6.10. Obtain an open-loop transfer function, $G(s)\,H(s)$, for an ideal buck–boost converter.

6.11. Determine if a potential stability problem exists for the buck converter with an input EMI filter shown in Figure 6.30. The parameters for the buck converters are: input voltage = 10 to 15 V, output voltage = 5 V, switching frequency = 1 kHz, output inductor = 10 mH, output capacitor = 1000 μF, $R_e = 0.005$ Ω, and $R_L = 5$ Ω. The parameters for the second-order input EMI filter are: $L_I = 10$ mH, $C_I = 2000$ μF, and $R_s = 0.005$ Ω.

6.12. Determine if a potential stability problem exists for a buck converter with an input EMI filter shown in Figure 6.30. The parameters for the

second-order input EMI filter are: $L_I = 100\,\mu H$, $C_I = 20{,}000\,\mu F$, $R_{esr} = 0.01\,\Omega$, $R_s = 0.005\,\Omega$. The buck converter has an input voltage range of 20 to 30 V DC. The output of the buck converter is connected to a load resistance of 0.5 Ω. The other parameters for the buck converter are: $C_o = 1000\,\mu F$, $L_o = 10\,mH$, and $f_s = 5\,kHz$.

6.13. A switching converter has an input voltage of 32 V and an input current of 3 A. Assume that the input impedance of the converter is completely resistive. Calculate the input EMI based on Figure 6.70, but do not use C_I; instead, use a big capacitor C_d with a large enough ESR to stabilize the converter. This technique is frequently used in many commercial circuits [30].

6.14. Repeat Problem 6.13, but now model the input impedance of the switching converter as a resistance in parallel with a capacitor, C. Determine a condition for the relative size of the EMI filter capacitor with respect to the converter capacitance that would stabilize the system [30].

6.15. Repeat Problem 6.13, but now use the optimal value of the damping resistor, as discussed in Erickson [31].

6.16. A buck converter has the following parameters: $V_s = 12\,V$, $V_a = 5\,V$, $L_o = 100\,\mu H$, $C_o = 100\,\mu F$, $R_{esr} = 0.001\,\Omega$, $R_L = 5\,\Omega$, and $f_s = 20\,kHz$. The peak amplitude of the sawtooth signal is 3 V. Find the discrete-time model.

6.17. For the converter of Problem 6.16, choose a stable closed-loop pole location and calculate the feedback gains necessary to obtain those closed-loop poles when voltage-mode control is applied.

6.18. For the converter of Problem 6.16, choose a stable closed-loop pole location and calculate the feedback gains necessary to obtain those closed-loop poles when current-mode control is applied.

6.19. For the converter of Problem 6.17, design the additional dynamics to achieve a zero steady-state error.

6.20. For the converter of Problem 6.18, design the additional dynamics to achieve zero steady-state error.

6.21. Calculate the small-signal state–space averaged model for a boost converter operating in the continuous conduction mode. Consider the losses in the switch as R_{on} and the losses in the diode as R_d. There are no other losses in the converter. Show all your work.

6.22. (a) Draw the small-signal model for a voltage-mode buck converter operating in the continuous conduction mode, using the simplified Vorpérian average switch model. (b) Explain how to set up the model parameters. (c) What information can you extract from this circuit?

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7

Interleaved Converters

7.1 INTRODUCTION

Interleaved converters are the result of a parallel connection of switching converters. They usually share the same output filter. Interleaved converters offer several advantages over single power stage converters; a lower current ripple on the input and output capacitors, faster transient response to load changes [1], and improved power handling capabilities at greater than 90% power efficiency. An interleaved converter can be realized by "interleaving" (or driving out of phase) the control signals to each of the paralleled converters, resulting in an effective increase in its switching frequency. They are used in applications where the loads demand low ripple or very tight tolerances. Such requirements are found in the new generation of personal computers, in which core voltages and currents of the central-processing-units (CPUs) are approaching 1 V and 130 A, respectively. [2]. Interleaving converters are also finding applications in switching audio amplifiers by interleaving series or parallel combinations of power inverters [3]. Additionally, interleaving enables the converter to spread its components and the dissipated power over a larger area.

7.2 INTERLEAVED BUCK CONVERTER

A two-stage parallel-interleaved buck converter is shown in Figure 7.1. As shown, the current to charge the output capacitor, C_1, is provided by the two similar output inductors, L_1 and L_2, from each of the paralleled converters. The charging current for each of these inductors comes from the individual converter stage. If the two switches were driven by the same pulse-width modulation (PWM) signal, inductors L_1 and L_2 would effectively be connected in parallel, thus resulting in an equivalent buck converter with a smaller inductor but only a half the total current flowing through each of these switches. However, if the two switches are driven by out-of-phase PWM signals, pwm_1 and pwm_2, with a phase shift equal to $2\pi/n$, where n is the number of paralleled cells (in this case $n = 2$), then the ripple current flowing through the output capacitor would be reduced.

Figure 7.2 shows the PSpice circuit schematic for a two-stage parallel-interleaved buck converter. The voltage and current waveforms of the simulated interleaved buck converter are shown in Figure 7.3. As can be seen, the phase shift between inductor currents, I_{L_1} and I_{L_2}, is 180°, while their current frequency is the same as the switching frequency. The current ripple of both the inductors is about 245 mA. In the steady state, the sum of

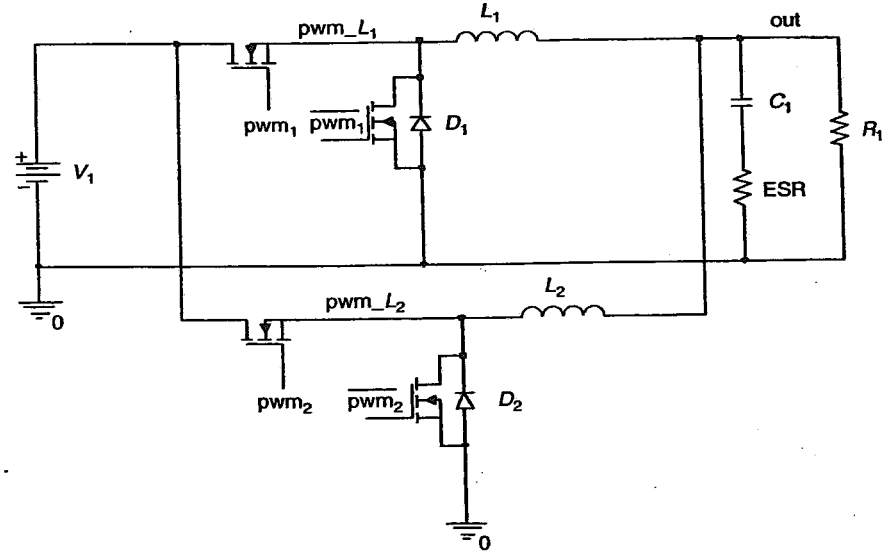

Figure 7.1 Interleaved buck converter.

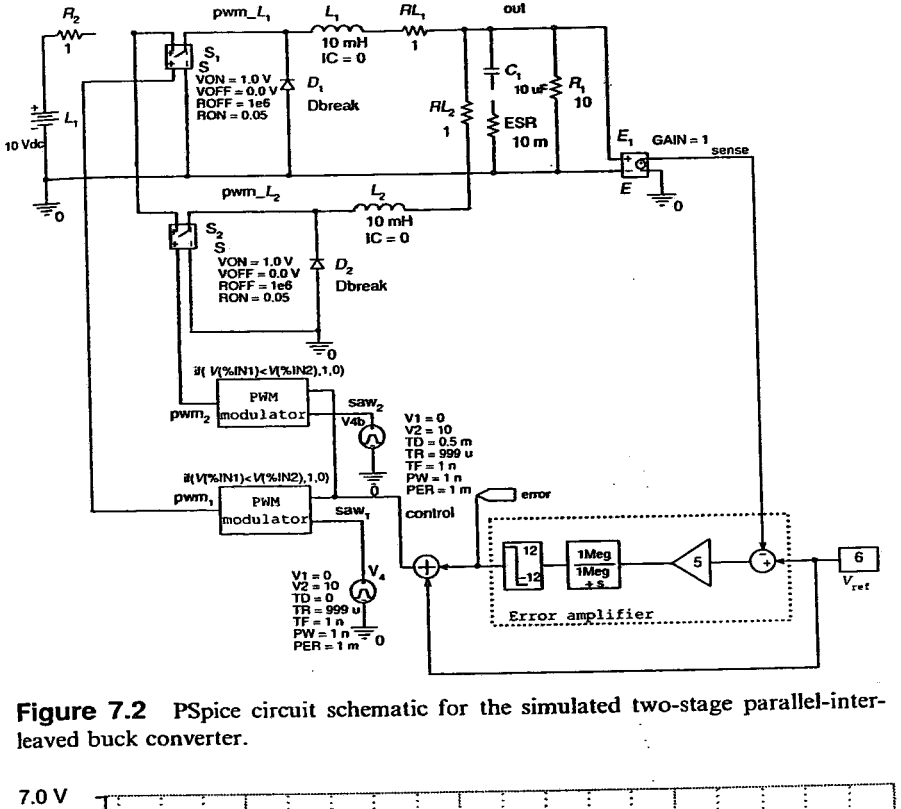

Figure 7.2 PSpice circuit schematic for the simulated two-stage parallel-interleaved buck converter.

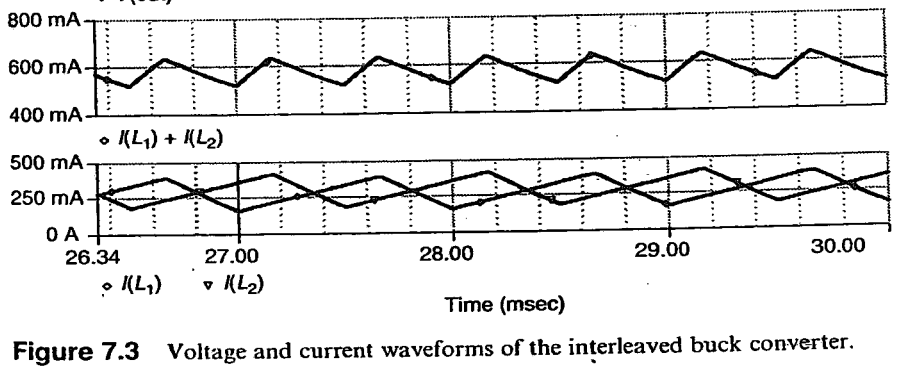

Figure 7.3 Voltage and current waveforms of the interleaved buck converter.

$I_{L_1} + I_{L_2}$ provides the charging current for the output capacitor as well as the average output load current. The amplitude of the current ripple in the combined $I_{L_1} + I_{L_2}$ is 80 mA but its frequency is twice the switching frequency. Since this ripple current determines the capacitor ripple voltage, the latter is reduced as compared to that of a single buck converter. It should be noted that the output ripple voltage also has twice the switching frequency.

The input and output current ripples of a paralleled interleaved converter are always less than or equal to those of the individual converter [4]. Under some special operating conditions, a zero current ripple can be achieved in this interleaved converter. This happens in a two-stage interleaved buck converter when it is operating at a 50% duty cycle. Unfortunately, this condition may only be achieved in the open-loop operation. In the close-loop configuration, the controller automatically adjusts the duty cycle to compensate for load or line fluctuations, thus losing the zero-ripple operation. Nevertheless, it is possible to operate near a zero-ripple point for small variations in the duty cycle.

As shown in Figure 7.2, the control signals, pwm_1 and pwm_2, are generated by comparing the same control signal with two sawtooth generators having a phase shift of 180°. In practice, a shift register or a counter and a decoder can be used to generate the shifted clock pulses [5].

7.2.1 State–Space Averaged Model

Figure 7.4 shows the PWM signals, pwm_1 and pwm_2, for the two switches of the interleaved buck converter shown in Figure 7.2. There are four modes of operation. During mode 1, both the PWM signals, pwm_1 and pwm_2, are high (HI). The duration of mode 1 is d_1. In mode 2, pwm_1 is high (HI) and

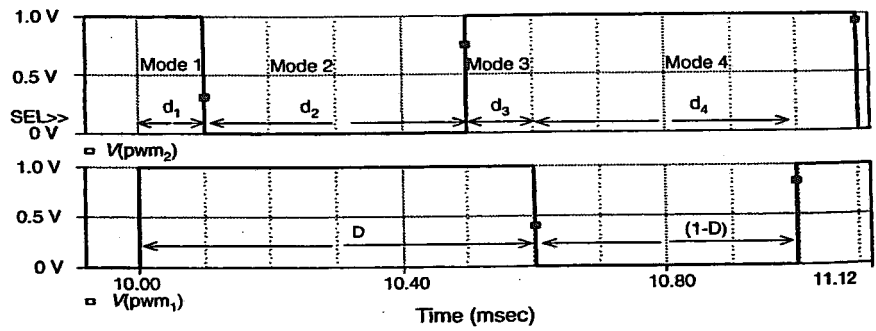

Figure 7.4 Switch driving signals, pwm1 and pwm2.

pwm_2 is low (LO); the duration of this mode is d_2. Mode 3 is similar to mode 1, i.e., both PWM signals, pwm_1 and pwm_2, are high (HI) and its duration is d_3. Finally, during mode 4, pwm_1 is low (LO) and pwm_2 is high (HI). Its duration is d_4.

Due to the circuit symmetry, we have

$$d_1 = d_3, \quad d_2 = d_4, \quad d_1 + d_2 = 0.5. \tag{7.1}$$

Since there are three independent energy-storage elements, the converter can be modeled by a third-order system. The state variables are selected as:

$$x = \begin{bmatrix} i_{L_1} \\ i_{L_2} \\ v_c \end{bmatrix}. \tag{7.2}$$

The state space model is

$$\begin{aligned} \dot{x} &= Ax + BV_s, \\ y &= Cx + D_u V_s, \end{aligned} \tag{7.3}$$

where

$$A = \begin{bmatrix} 0 & 0 & \frac{-1}{L_1} \\ 0 & 0 & \frac{-1}{L_2} \\ \frac{1}{C} & \frac{1}{C} & \frac{-1}{RC} \end{bmatrix}, \quad B = \begin{bmatrix} \frac{2d_1+d_2}{L_1} \\ \frac{2d_1+d_2}{L_2} \\ 0 \end{bmatrix}, \quad C = [0 \;\; 0 \;\; 1], \quad D_u = 0. \tag{7.4}$$

The voltage conversion ratio is given by

$$V_a = V_s D. \tag{7.5}$$

All converter cells are phase shifted and they equally share the current at steady-state operation. The transient response can be improved by the control strategy proposed by Miftakhutdinov [1], where during a load transient all the converter cells switch to the same state simultaneously. Under this condition, the interleaved converter can be considered as a one-cell converter, which has the same input voltage, V_s, as the original interleaved converter and a smaller output inductor $L_{ob} = L_i/n$. Therefore, the corner frequency of the output filter is shifted up in frequency, yielding a faster transient response.

7.3 INTERLEAVED BOOST CONVERTER

Figure 7.5 shows the circuit diagram of a two-cell interleaved boost converter, while Figure 7.6 shows its correspondent PSpice schematic. As shown, both cells share the input voltage, V_s, and the output capacitor, C_1. The PWM signals, pwm_1 and pwm_2, are shifted by 180°, or $2\pi/n$, where $n=2$, as shown in Figure 7.7. The input current is equal to the sum of the inductor currents, $I_{L_1} + I_{L_2}$. Since the inductor currents are 180° out of phase, the resulting input current has a very low ripple. This characteristic, in combination with the continuous input current of the boost converter, makes this circuit ideal for applications in personal computer power supplies and power-factor compensators [6].

7.3.1 State–Space Averaged Model

Similar to the interleaved buck converter, for the continuous conduction mode (CCM) of operation, we have

$$d_1 = d_3, \quad d_2 = d_4, \quad d_1 + d_2 = 0.5. \tag{7.6}$$

Since there are three independent energy-storage elements, the converter can be modeled by a third-order system. The state variables are selected as

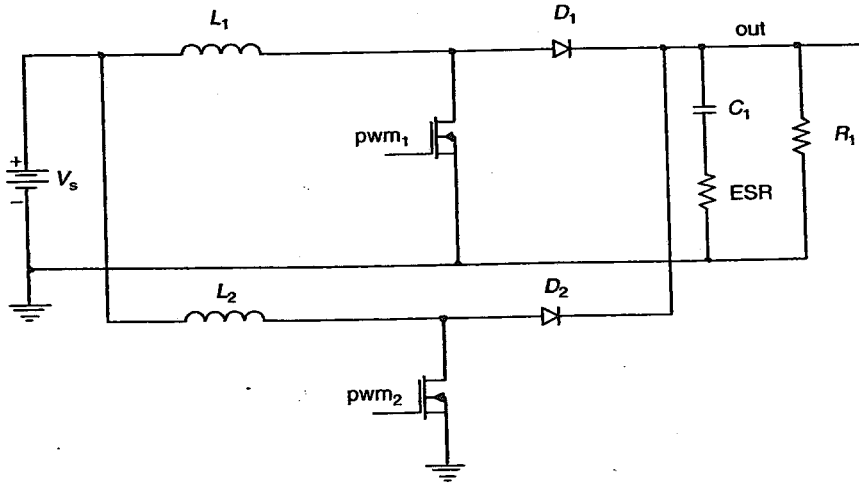

Figure 7.5 Interleaved boost converter.

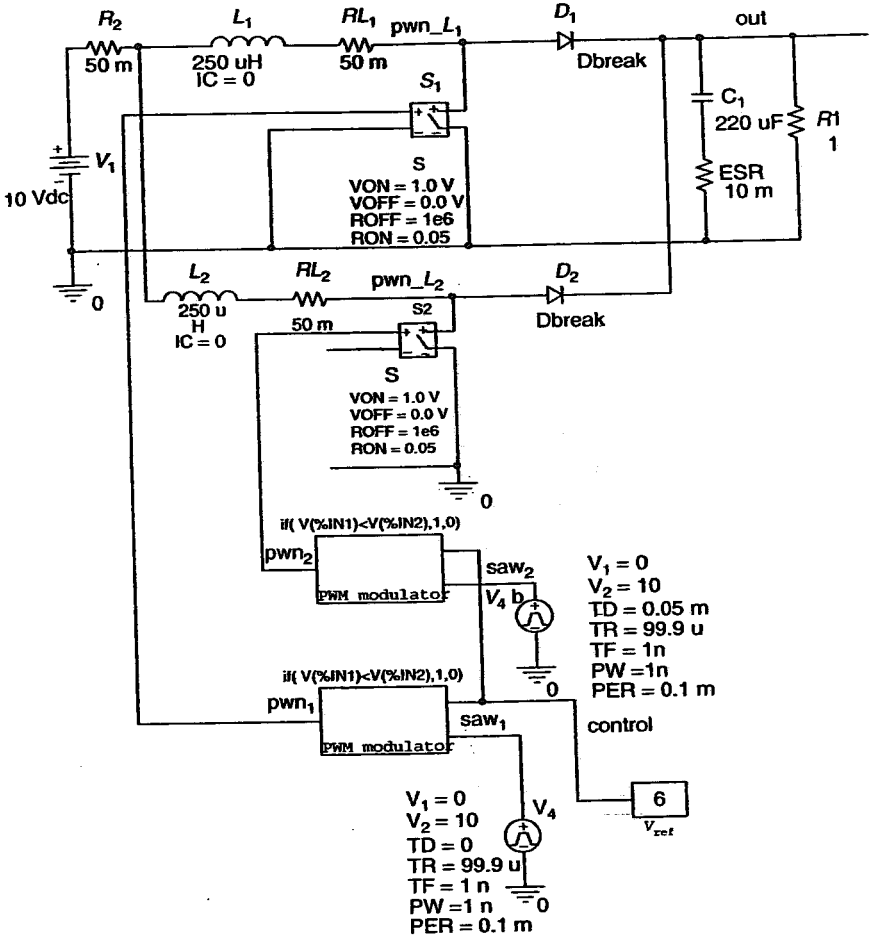

Figure 7.6 PSpice schematic of an interleaved boost converter.

$$x = \begin{bmatrix} i_{L_1} \\ i_{L_2} \\ v_c \end{bmatrix}. \tag{7.7}$$

The state space model is

$$\begin{aligned} \dot{x} &= Ax + BV_s, \\ y &= Cx + D_u V_s, \end{aligned} \tag{7.8}$$

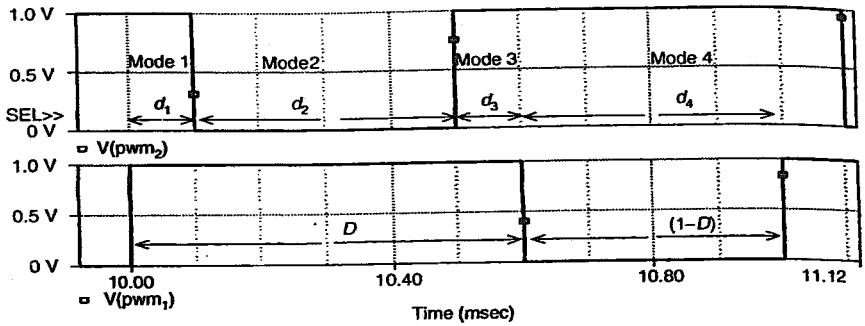

Figure 7.7 PWM and current waveforms of the interleaved boost converter.

where

$$\begin{aligned}
&\bar{A} = A_1 d_1 + A_2 d_2 + A_3 d_3 + A_4 d_4,\\
&\bar{B} = B_1 d_1 + B_2 d_2 + B_3 d_3 + B_4 d_4,\\
&C = [0 \quad 0 \quad 1], \text{ and}\\
&D_u = 0
\end{aligned} \tag{7.9}$$

An expanded view of the input current and the two-inductor currents is shown in Figure 7.8. Since the duty cycle is not 50% (i.e., $D = 0.6$), the ripple of the two inductor currents does not cancel when added. Nevertheless, the input current ripple is 500 mA, while the ripple current of each inductor is 1.5 A. The input ripple current can be further reduced by forcing the operation close to $D = 0.5$ or by increasing the number of paralleled cells.

Figure 7.9 represents the output current and voltage waveforms of the simulated interleaved boost converter. Under the simulated conditions, $P_o = 200\,\text{W}$, $f_s = 10\,\text{kHz}$, and $C_1 = 220\,\mu\text{f}$, the output voltage ripple is close to 1 V. Increasing the switching frequency or the output capacitance reduces the output voltage ripple.

Figure 7.10 shows the equivalent circuits of the operating modes of the CCM interleaved boost converter. The state matrixes for each mode can be calculated as follows:

$$A_1 = A_3 = \begin{bmatrix} 0 & 0 & 0 \\ 0 & 0 & 0 \\ 0 & 0 & \frac{1}{RC} \end{bmatrix}, \quad B_1 = B_3 = \begin{bmatrix} \frac{1}{L_1} \\ \frac{1}{L_2} \\ 0 \end{bmatrix}, \tag{7.10}$$

$$A_2 = \begin{bmatrix} 0 & 0 & 0 \\ 0 & 0 & \frac{-1}{L_2} \\ 0 & \frac{-1}{C} & \frac{-1}{RC} \end{bmatrix}, \quad B_2 = \begin{bmatrix} \frac{1}{L_1} \\ \frac{1}{L_2} \\ 0 \end{bmatrix}, \tag{7.11}$$

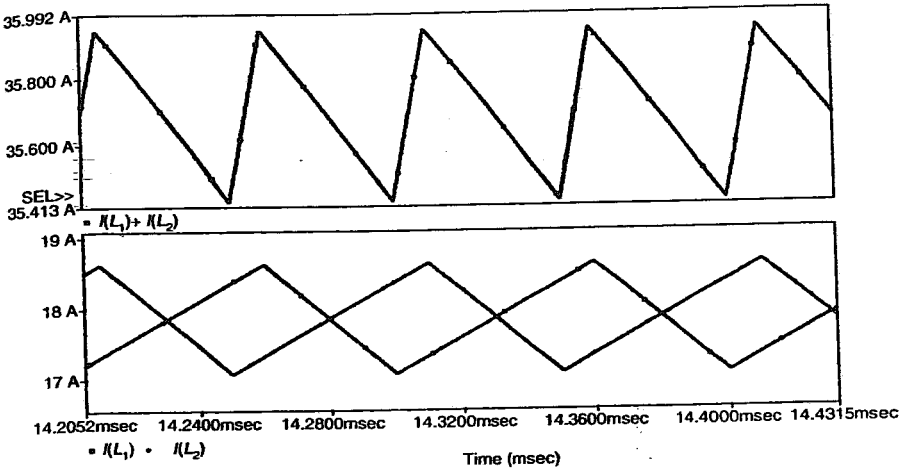

Figure 7.8 Input and inductors currents.

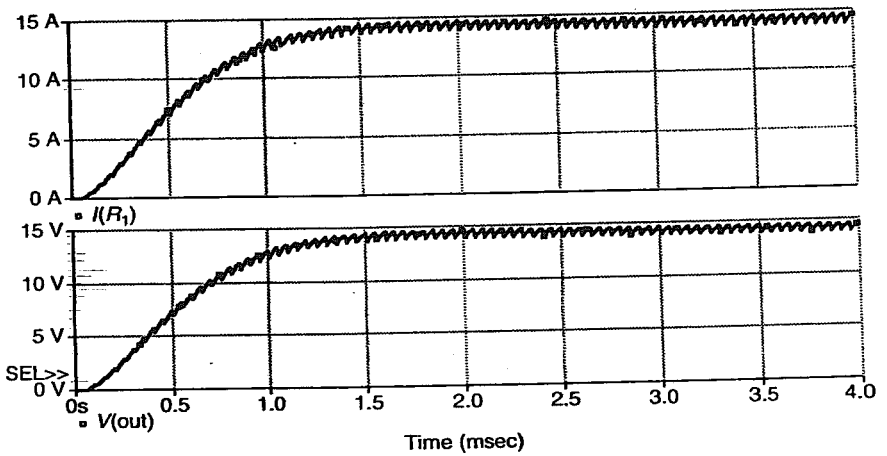

Figure 7.9 Output current and voltage waveforms of the interleaved boost converter.

and

$$A_4 = \begin{bmatrix} 0 & 0 & \frac{-1}{LC} \\ 0 & 0 & 0 \\ \frac{-1}{C} & 0 & \frac{1}{RC} \end{bmatrix}, \quad B_4 = \begin{bmatrix} \frac{1}{L_1} \\ \frac{1}{L_2} \\ 0 \end{bmatrix}. \tag{7.12}$$

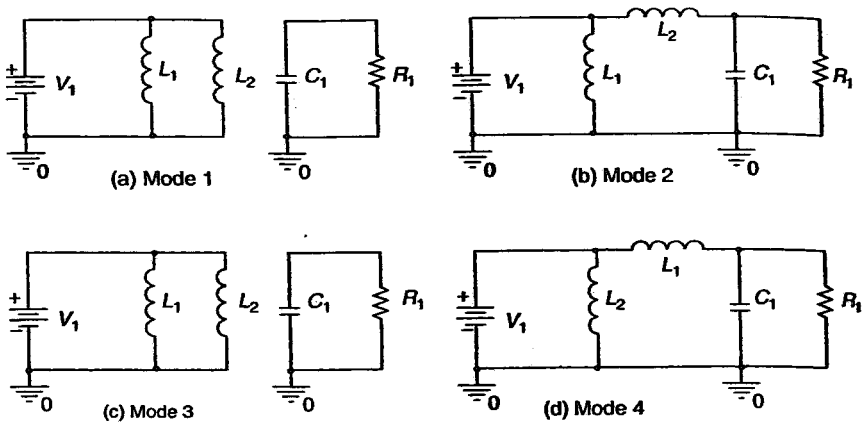

Figure 7.10 Equivalent circuits of the operating modes of the CCM interleaved boost converter.

Finally,

$$\bar{A} = \begin{bmatrix} 0 & 0 & \dfrac{-d_4}{L_2} \\ 0 & 0 & \dfrac{-d_2}{L_2} \\ \dfrac{-d_4}{C} & \dfrac{-d_2}{C} & \dfrac{1}{RC} \end{bmatrix}, \qquad \bar{B} = \begin{bmatrix} \dfrac{1}{L_1} \\ \dfrac{1}{L_2} \\ 0 \end{bmatrix}, \tag{7.13}$$

$$\boldsymbol{C} = [0\ 0\ 1], \quad \boldsymbol{D}_u = 0.$$

The conversion ratio can be calculated by imposing the volt-second balance on the inductor L_1.

$$d_1 V_1 + d_2 V_1 + d_3 V_1 + d_4 (V_1 - v_c) = 0 \tag{7.14}$$

since

$$d_1 + d_2 + d_3 = D \quad \text{and} \quad d_4 = (1 - D) \tag{7.15}$$

then

$$v_c = \frac{V_s}{d_4} = \frac{V_s}{(1 - D)}. \tag{7.16}$$

This is the same expression as for a single-stage or one-cell boost converter operating in the CCM.

7.4 INTERLEAVED CONVERTER OPERATION BASED ON CURRENT-MODE

A family of interleaved converters based on current-mode control (CMC) could be generated by connecting N identical boost converters in parallel, as depicted in Figure 7.11. The CMC using interleaving techniques based on a binary-state transition diagram was proposed in Giral et al. [7]. In a binary-state transition diagram, the status of all the switches is represented by a binary code, a "1" is used when the switch is on and a "0" when the switch is off. From the 2^N possible binary states, one state-transition cyclic sequence is chosen to generate the required phase shift $2\pi/N$ among the converter waveforms. In steady state, all the binary states have the same duration and

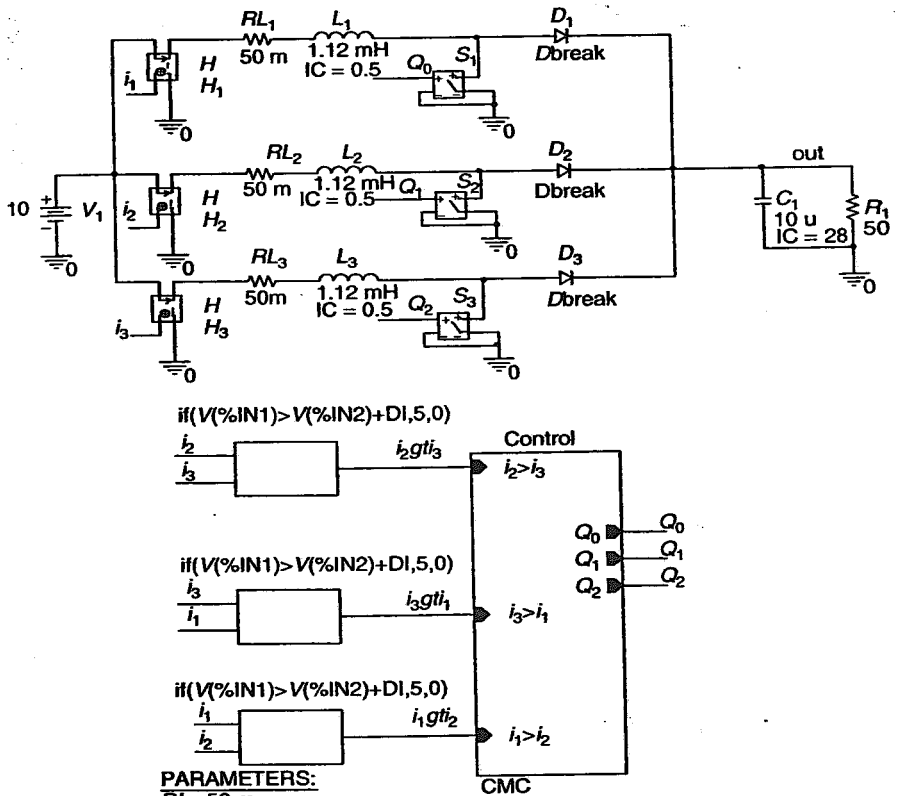

Figure 7.11 Interleaved boost converter with CMC.

the cyclic sequence imposes a complementary duty cycle $1/N$ for each state, resulting in an average output voltage which is N times the input voltage.

An example corresponding to $N=3$ is analyzed. The control is implemented using a comparator with a hysteresis band, Δi, combinational logics, and a shift register. The current-controlled voltage sources H_i are used as current sensors for the PSpice simulation. The comparators are modeled with the ABM1 block using an If() statement.

The corresponding state-transition diagram is illustrated in Figure 7.12. Starting from state 011 ($S_3\ S_2\ S_1$), a condition where $i_2 > i_3 + \Delta i$ forces the change to the next state 110. The converter remains in this state until the condition, $i_3 > i_1 + \Delta i$, causes the transition to state 101. The converter will stay in this state until the condition, $i_1 > i_2 + \Delta i$, is met and a transition to the initial state, 011 is made, starting the cycle all over again.

The switching frequency, f_s, is inversely proportional to the hysteresis width,

$$\begin{aligned} f_s &= \frac{V_g}{L}\frac{D}{(N-1)\,\Delta i} \\ &= \frac{V_g}{L}\frac{N-1}{N}\frac{1}{(N-1)\,\Delta i} \\ &= \frac{V_g}{L}\frac{1}{N\Delta i}, \end{aligned} \tag{7.17}$$

where V_g is the input voltage, D is the steady-state duty cycle, and L is the inductance value of each converter.

7.4.1 Ripple Calculations

One of the main features of interleaved converters is the ripple reduction. In this case, the focus is on the input current ripple, which becomes considerably reduced. Figure 7.13 illustrates the steady-state waveforms of the capacitor current, output voltage, and the different inductor currents for

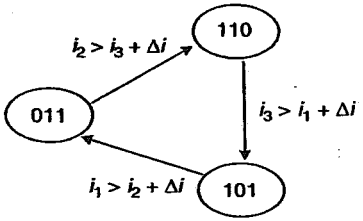

Figure 7.12 Control state diagram.

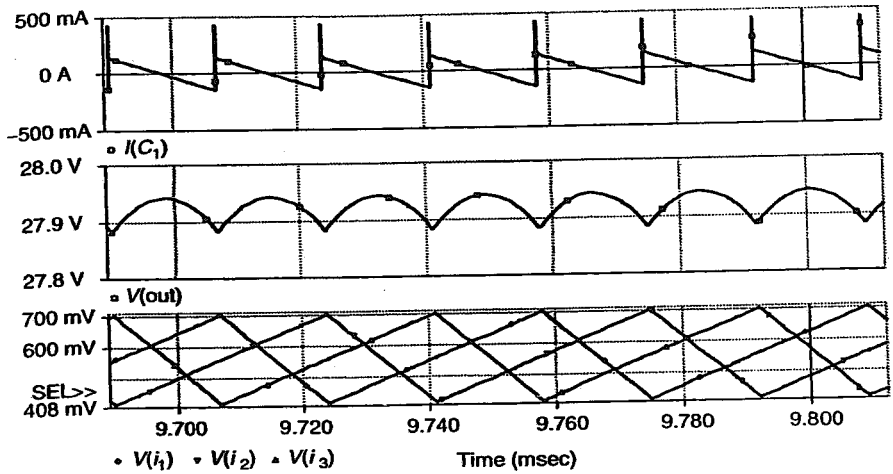

Figure 7.13 Voltage and current waveforms of the interleaved boost converter with CMM.

$N = 3$. As shown in this figure, the ripple in each inductor current, ΔI_l, is exactly two times $(N - 1)$ the hysteresis width of the controller.

The expression of the output voltage ripple is given by

$$\Delta v_o = \frac{1}{C}\frac{1}{2}\frac{\Delta I_l}{2}\frac{D'T}{2} = \frac{(N-1)\,\Delta i D'T}{8C}, \tag{7.18}$$

which depends on the current ripple in one of the inductors. Thus, reducing ΔI_l also reduces the output voltage ripple at the expense of an increased switching frequency. Alternatively, Δv_o can also be reduced by increasing the value of C.

Taking into account that $D' = 1/N$ and $T = 1/f_s$, then

$$\Delta v_o = \frac{L(N-1)\Delta i^2}{8CV_g}. \tag{7.19}$$

It can be seen that there is also an improvement in the output voltage ripple if L is reduced. Considering a constant current ripple, Δv_o will increase if the number of converters is increased.

The amplitude of the input current ripple is given by

$$\Delta I_g = \frac{2}{9\sqrt{3}}\frac{\Delta v_o}{L}D'T = \frac{2}{36\sqrt{3}}\frac{\Delta I_l}{LC}(D'T)^2 = \frac{1}{18\sqrt{3}}\frac{\Delta I_l}{LC}\left(\frac{T}{N}\right)^2. \tag{7.20}$$

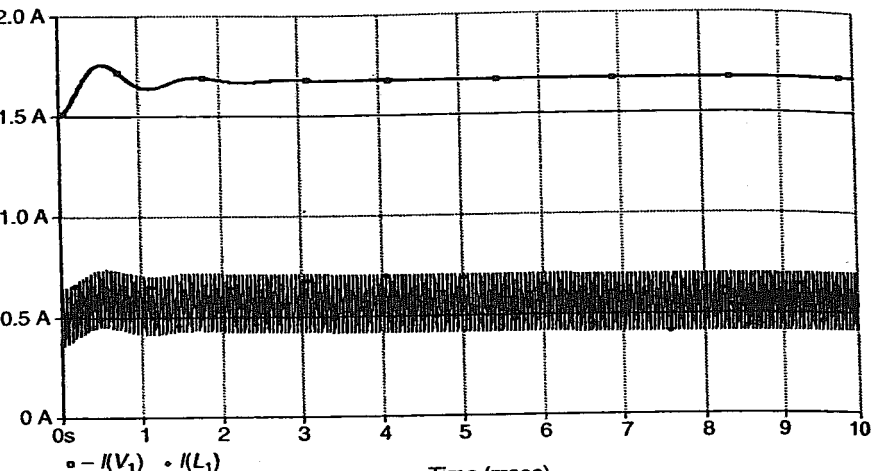

Figure 7.14 Comparison of the input current and the inductor current.

Thus, increasing N reduces the input current ripple. The reduction in the input current ripple achieved by this topology is shown in Figure 7.14, where a comparison of the input current and the current flowing through one of the inductors are illustrated. Figure 7.15 shows an expanded view. The ripple in the input current is 460 μA, while the ripple in each inductor current is 280 mA; this is a 1/600-reduction ratio. This example reveals the main advantage of this topology, which is the possibility of an almost ripple-free input current.

7.4.2 Number of Converters

Although the input and output ripples can be very small, it is not possible to regulate the average values of both input current and output voltage independently. The first criterion to choose N will be derived from the output voltage or input current specifications. Since $D = N/(N - 1)$, increasing N makes the duty cycle closer to its upper bound of 100%. Experimental limits, however, establish $D_{max} = 0.9$, which corresponds to $N_{max} = 10$.

7.5 POWER FACTOR CORRECTION

Nonlinear loads in electronic systems degrade the quality of the utility system by reducing its power factor and injecting unwanted frequencies. As such, electric appliances or electronic systems drawing a sinusoidal current at a

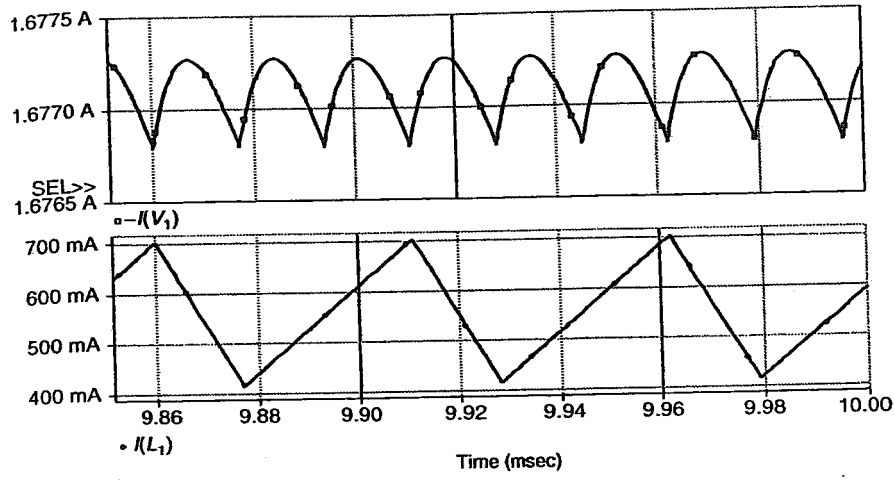

Figure 7.15 Comparison of the input current ripple and the inductor current ripple.

unity power factor, ideally behaving as a resistive load, are desired. Most electric appliances or electronic systems are designed to accept the full range of Japanese, North American, and European utility voltages, which span approximately from 93 to 264 V(AC). Moreover, a typical universal-input topology for power factor correction must satisfy both the IEC 555-2 line harmonic standard and VDE 0871B conducted EMI emissions standard. A typical input converter topology that satisfies all the above requirements is based on the boost converter. The most common topology for single-phase utility interfaces is covered in Mohan et al. [8] where a hysteresis current control forces the input inductor current to follow a full-wave rectified sinusoidal reference current. Miwa et al. [9] proposes the use of interleaving techniques to reduce the switching frequency and associated losses.

An example of such a universal-input AC–DC power supply using interleaving techniques is shown in Figure 7.16. A two-stage interleaved boost converter that outputs twice the input voltage serves as the AC interface. The reference current, I_{ref1}, is proportional to the required input current. The input inductor current, I_{L_1}, is forced to follow I_{ref1} with a hysteresis control, as shown in Figure 7.17. The current flowing through the other input inductor, I_{L_2}, is just a delayed version of I_{L_1}, with a $2\pi/N$ phase shift.

Figure 7.16 shows the input voltage waveform, V(AC), and the resulting total input current, $I(R_s)$. Notice that the input current looks like a

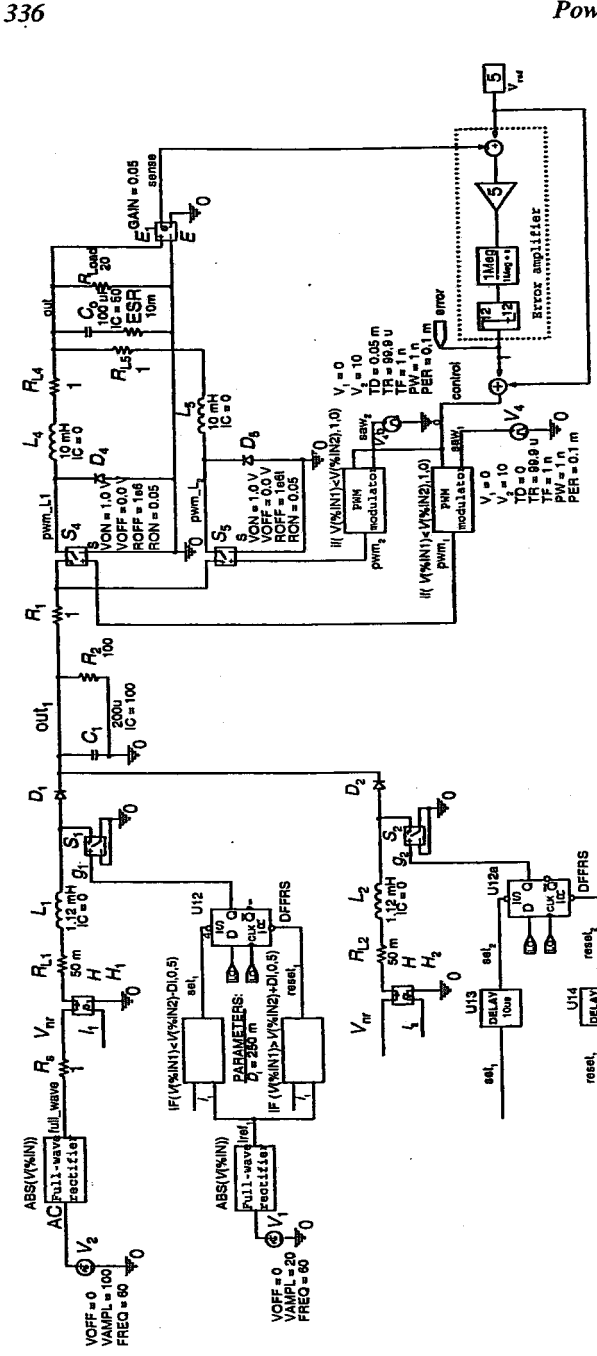

Figure 7.16 Universal-input AC–DC power supply using interleaving techniques.

full-wave rectified sinusoidal current in phase with the input voltage. Thus, this makes the converter behave like a resistive load, with a very low harmonic current distortion. The bottom half of Figure 7.18 displays the output voltage of the boost front-end, *V*(out1), and the DC output voltage,

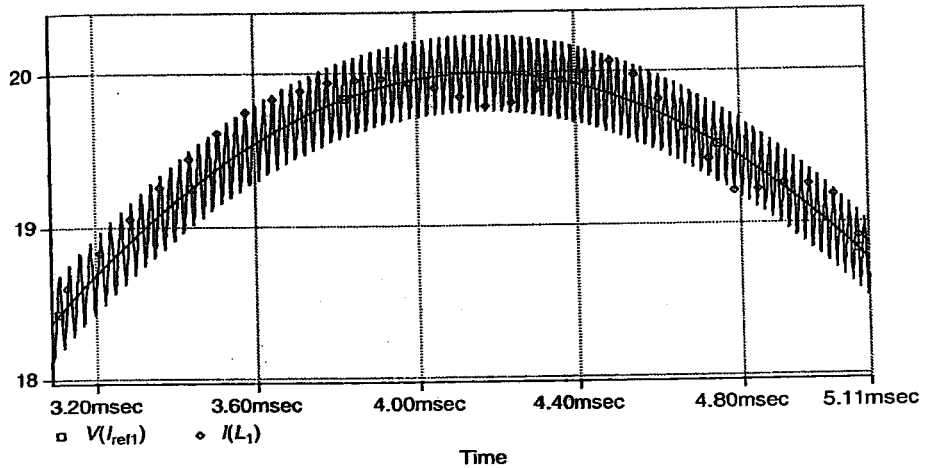

Figure 7.17 Reference and input inductor currents.

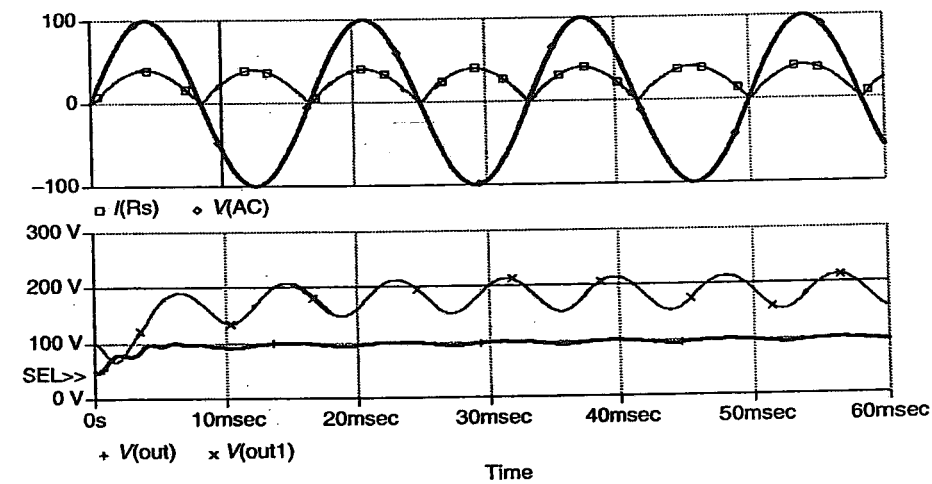

Figure 7.18 Input and output waveforms for the interleaved universal-input AC–DC converter.

V(out). Notice that V(out1) is close to 200 V (twice the input voltage) with a large ripple of 60 V. The second stage is the interleaved buck converter analyzed previously. The reference voltage is set to operate near a zero-ripple operating point ($D = 0.5$ in this case). This guarantees a DC output voltage with a reduced voltage ripple, using a small output capacitor.

PROBLEMS

7.1. Show that the expression of the state-space averaged model of the interleaved buck converter of Figure 7.1 is:

$$\bar{A} = \begin{bmatrix} 0 & 0 & \frac{-1}{L_1} \\ 0 & 0 & \frac{-1}{L_2} \\ \frac{1}{C} & \frac{1}{C} & \frac{-1}{RC} \end{bmatrix}, \quad \bar{B} = \begin{bmatrix} \frac{2d_1 + d_2}{L_1} \\ \frac{2d_1 + d_2}{L_2} \\ 0 \end{bmatrix},$$

$C = [0 \quad 0 \quad 1]$, $D_u = 0$.

7.2. Consider the interleaved buck converter of Figure 7.1. Design a voltage regulator that would output 3 V from a 10-V input source. Measure the simulated output voltage ripple.

7.3. Consider the interleaved buck converter of Figure 7.1 operating with a fixed duty cycle $D = 0.5$. Design a switching converter to be connected between the unregulated DC input voltage and the interleaved converter. This converter should act as a preregulator to develop the necessary input voltage for the interleaved converter to maintain a constant 3-V output. Compare the output voltage ripple of the regulator with (problem 7.3) and without (problem 7.2) the switching preregulator.

7.4. Modify the universal-input AC–DC power supply shown in Figure 7.16 to accept AC input voltages from 94 to 264 V. Hint: the load connected to this utility interface absorbs a constant power. You will have to apply feedback to recalculate a different reference current for each input voltage level.

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8

Switched Capacitor Converters

8.1 INTRODUCTION

Switched capacitor converters (SCCs) are implemented by a combination of switches and capacitors. The switches are controlled in such a way that the capacitors are charged and discharged through different paths; producing an output voltage that is proportional to the input voltage. The different combinations of capacitors and switches result in SCC topologies able to produce an output voltage that may be higher or lower than the input voltage as well as polarity reversal.

The main advantage of the SCC is the absence of inductors and transformers, making possible a complete integration of the switching converter using integrated circuit technology. Also, they are easier to control than the magnetic-based switched-mode converters. The main disadvantage of SCC is that they require more switches than the magnetic-based switching converters. The switching currents in these SCC are also high, and thus, EMI is a major concern. However, SCCs are useful for small output power applications that do not require isolation between the input and output.

8.2 UNIDIRECTIONAL POWER FLOW SCC

Three basic SCC topologies are first discussed to introduce the mechanism of SCC. These converters do not regulate the output voltage satisfactorily, because the output voltage cannot be changed by controlling the duty cycle or the switching frequency [1]. Since the capacitors are charged and discharged through the switches, the output voltage depends on the impedances of the switches.

8.2.1 Basic Step-Up Converter

A basic step-up SCC is displayed in Figure 8.1. The gate signals, g_1 and g_2, of the MOSFETs, M_1 and M_2, are complementary signals and require a dead time to avoid short-circuiting the input voltage source, V_1, during switching transient. When M_1 is off and M_2 is on, capacitor C_1 is charged to V_1 through D_1 (see Figure 8.2(a)). When M_1 is on and M_2 is off, capacitor C_2 is charged to $V_1 + V_{C1} = 2V_1$ through D_2, according to the equivalent circuit of Figure 8.2(b). Therefore, the output voltage of the basic step-up SCC of Figure 8.1 is ideally twice the input voltage. As such, this circuit is also known as a voltage doubler. However, the output voltage is usually smaller than twice the input voltage due to losses. Note that the energy transfer capacitor, C_1, is charged in parallel with the voltage source and discharged in series with it.

Figure 8.3 and Figure 8.4 show the steady-state voltage and current waveforms of the basic step-up SCC shown in Figure 8.1 for a 25% duty cycle on M_1. Notice how the output voltage increases as C_2 is charged through M_1. When M_2 is on, C_2 discharges through the load resistor and the output voltage decreases. The average output voltage is smaller than 20 V due to the voltage drop across the nonideal switches.

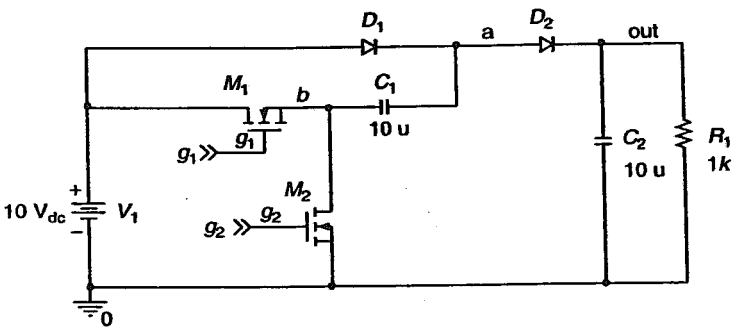
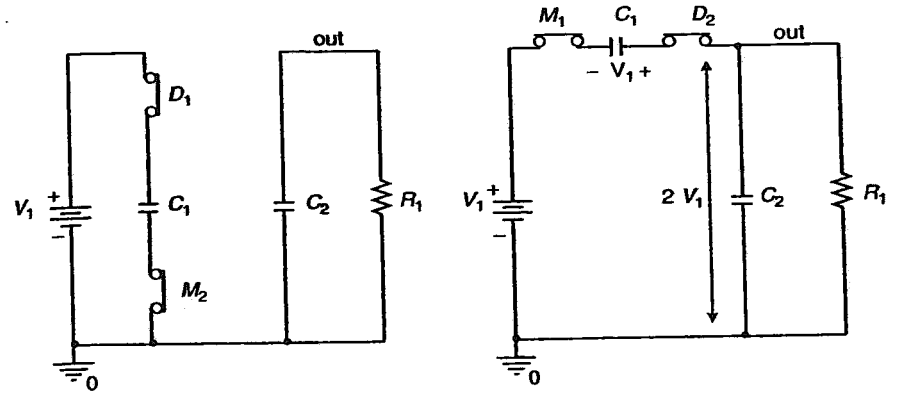


Figure 8.1 Step-up converter.



(a) equivalent circuit while M_2 is on. (b) equivalent circuit while M_1 is on.

Figure 8.2 Equivalent circuits for the basic step-up SCC.

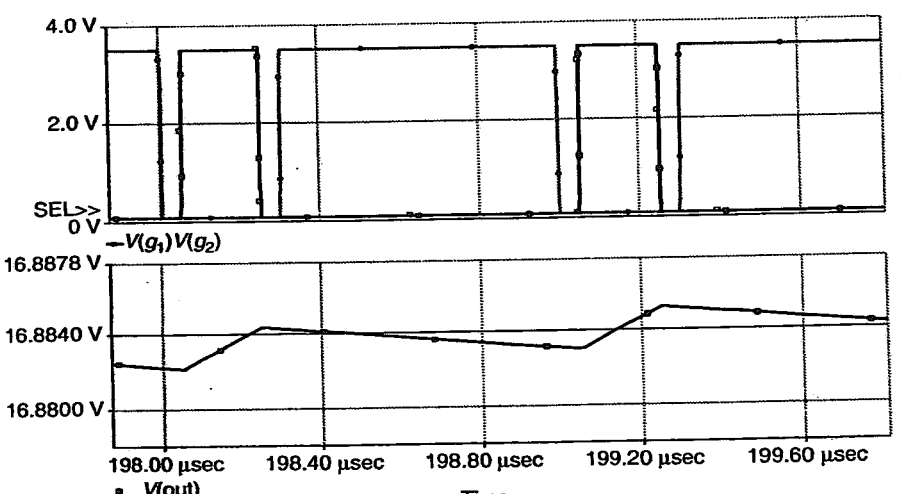


Figure 8.3 Steady-state waveforms of the basic step-up SCC for $D = 25\%$.

For an average load current, $I(R_1)$, close to 17 mA, the currents through the switches, $I(D_1)$ and $I(D_2)$, increase up to 45 and 135 mA, respectively. Since the charging and discharging currents are only limited by the circuit losses, they may become very large, degrading the efficiency and aggravating EMI emission.

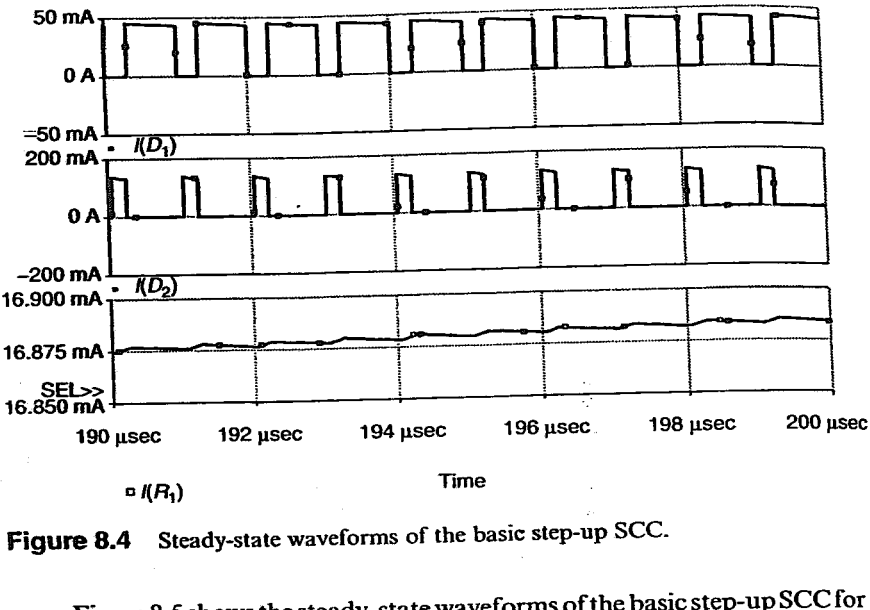


Figure 8.4 Steady-state waveforms of the basic step-up SCC.

Figure 8.5 shows the steady-state waveforms of the basic step-up SCC for $D = 50\%$. Note that even when the duty cycle has changed considerably (i.e., from 25 to 50%) the output voltage has barely changed. This proves the poor output voltage regulation that can be achieved by changing the duty cycle in this topology.

8.2.2 Basic Step-Down Converter

The basic step-down SCC shown in Figure 8.6 has two modes of operation, depending on the two complementary switches M_1 and M_2. In the steady state, $V_{C_1} > V_{C_2} > 0$.[1] When M_1 is on ($V(g_1) = hi$), C_1 and C_2 are connected in series through D_2, as shown in Figure 8.7(a). C_1 is charged from the voltage source, V_1. The corresponding steady-state waveforms are shown in Figure 8.8. If the charging current $I_{C_1} < I_{R_1}$ (see Figure 8.9), then C_2 has to provide the rest of the load current; thus, I_{C_2} is negative when C_1 is charging (i.e., $I_{C_2} = I_{C_1} - I_{R_1}$).

When M_2 is on, the two capacitors are connected in parallel, as displayed in Figure 8.7(b). Since $V_{C_1} > V_{C_2}$, the capacitor C_1 provides enough current to charge C_2 and supply the load.

Figure 8.9 shows the current waveforms through the two capacitors and the load. While C_1 is charged, C_2 discharges through the load. On the

[1] With ideal switches, $V_{C_1} = V_{C_2} = V_1/2$.

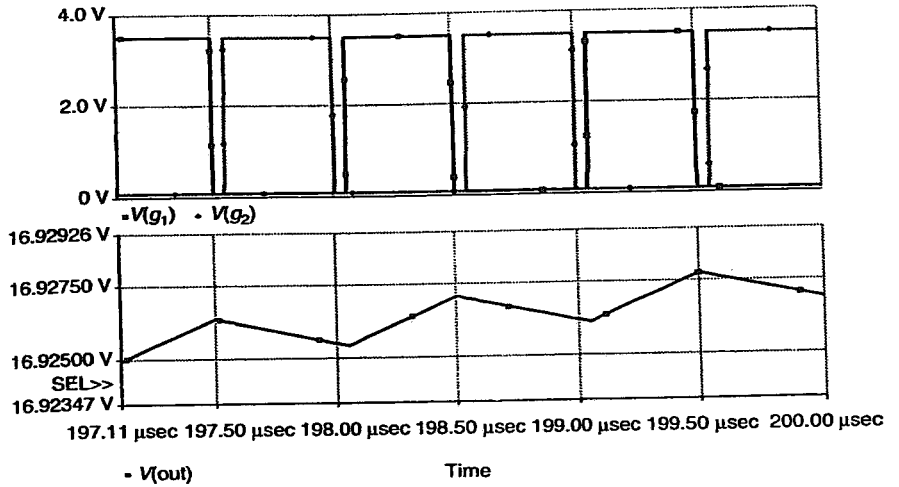


Figure 8.5 Steady-state waveforms of the basic step-up SCC for $D = 50\%$.

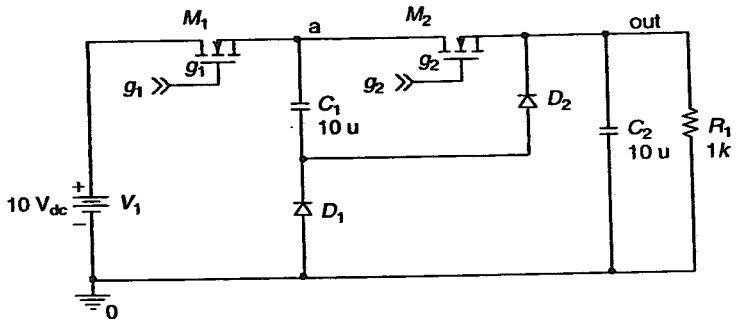
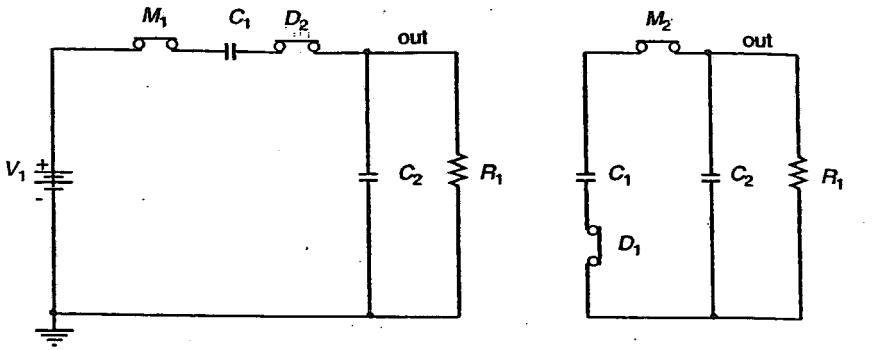


Figure 8.6 Basic step-down SCC.

other hand, when C_1 discharges, its current is large enough to charge C_2 and supply the load current.

8.2.3 Basic Inverting Converter

The output voltage of the basic polarity inverting SCC as shown in Figure 8.10 is ideally at $-V_1$. However, smaller magnitude is usually obtained due to the voltage drop across the switches. There are two modes of operation for this circuit. Capacitor C_1 is charged to V_1 when M_1 is on, with the polarity indicated in the equivalent circuit of Figure 8.11(a).



(a) equivalent circuit while M_1 is on. (b) equivalent circuit while M_2 is on.

Figure 8.7 Equivalent circuits for the basic step-down SCC.

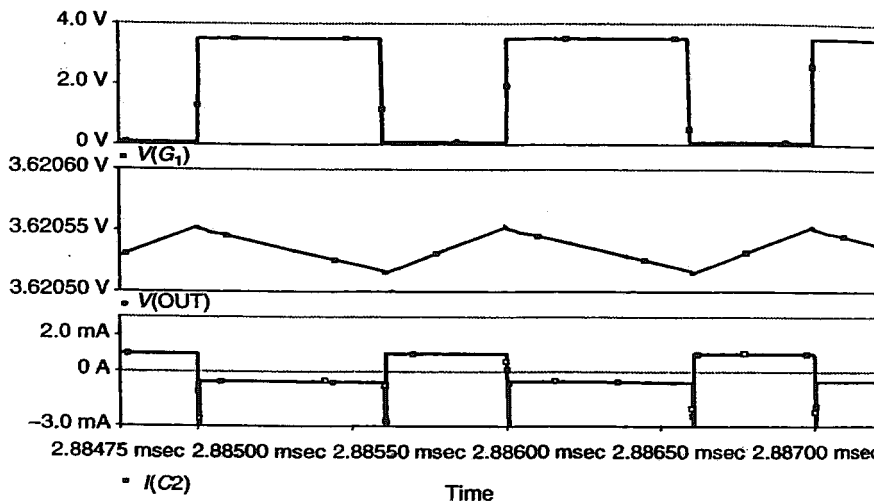


Figure 8.8 Steady-state output capacitor waveforms for the basic step-down SCC.

When M_2 is switched on, C_1 is connected to the output capacitor, C_2, through D_2, transferring a negative voltage. The equivalent circuit for this mode of operation is shown in Figure 8.11(b).

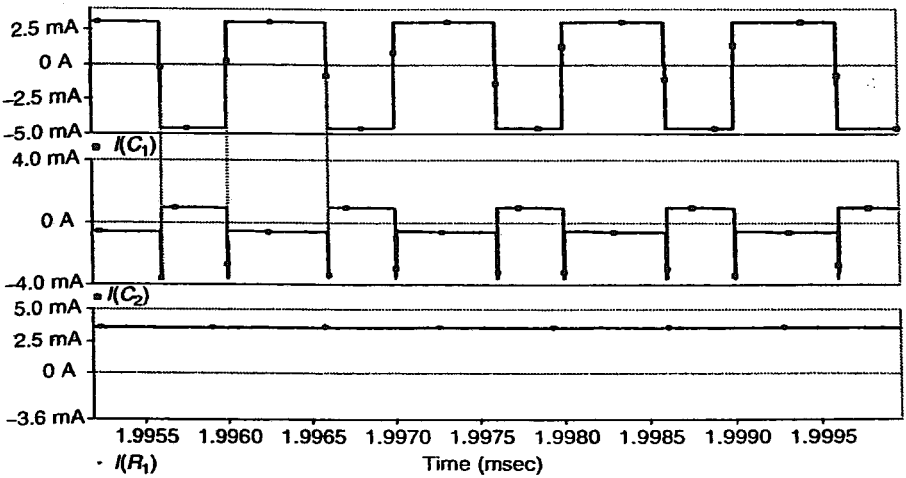


Figure 8.9 Steady-state current waveforms for the basic step-down SCC.

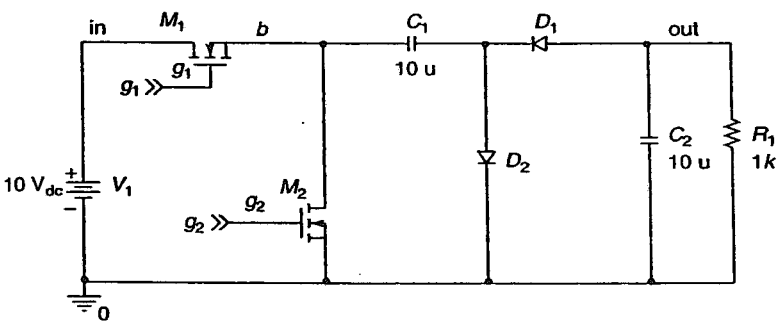
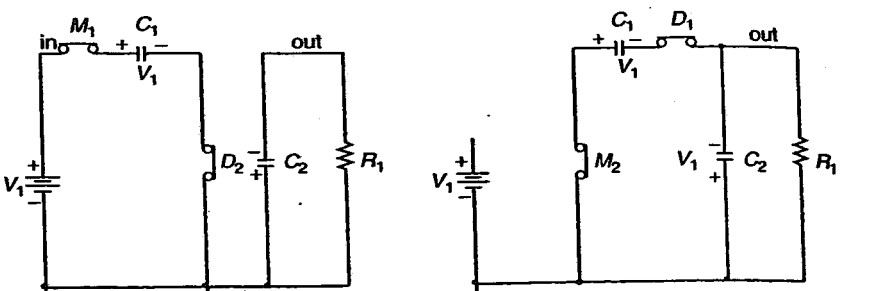


Figure 8.10 Voltage polarity inverting converter.

8.3 ALTERNATIVE SWITCHED CAPACITOR CONVERTER TOPOLOGIES

The output voltage of the basic SCC analyzed in Section 8.2 depends on the circuit topology. As such, this lack of flexibility limits their uses. Many alternative topologies have been proposed to overcome this limitation [2,3], providing a flexible conversion ratio governed by the duty cycle. This section analyzes some of these circuits.



(a) equivalent circuit while M_1 is on. (b) equivalent circuit while M_2 is on.

Figure 8.11 Equivalent circuits for the basic polarity inverting SCC.

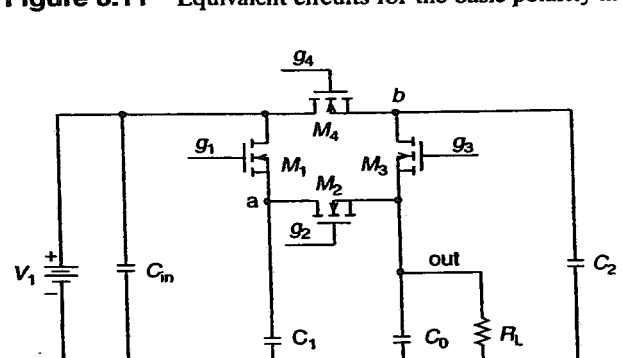


Figure 8.12 Step-down SCC.

8.3.1 Step-Down Converter

The conversion ratio of the step-down SCC proposed in Cheong et al. [2] can be fixed by choosing an appropriate steady-state value of the duty ratio. The circuit shown in Figure 8.12 has four controlled switches, M_1–M_4, two energy transfer capacitors, C_1 and C_2, an output capacitor, C_o and an input capacitor, C_i. R_L is the load resistance.

The converter has four modes of operation. The gate signals, g_1–g_4, corresponding to the switches M_1–M_4, are shown in Figure 8.13. The timing diagram of Figure 8.13 corresponds to a conversion ratio of 0.5. g_2 and g_3 are complementary signals with a 50% duty cycle. The gate signals g_1 and g_4

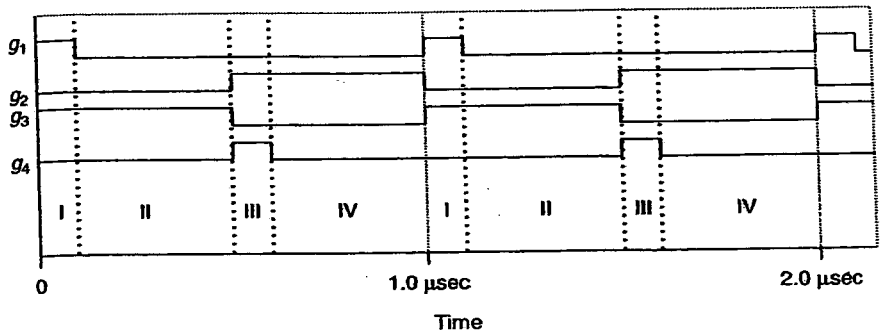


Figure 8.13 Time diagram of the gate signals.

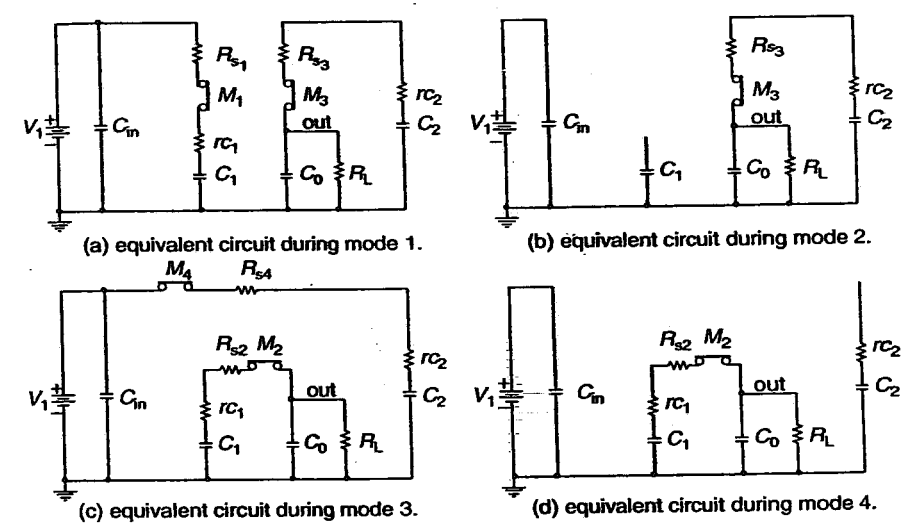


Figure 8.14 Equivalent circuits during the operating modes.

are synchronously turned on at nT_s and $(n + 0.5)T_s$, respectively. g_1 and g_4 have the same pulse width, t_{on}.

Mode 1 is determined by M_1 and M_3 being both turned on; the equivalent circuit for this mode of operation is shown in Figure 8.14(a). C_1 is charged slightly higher than $V_1/2$. The charging time, T_{on}, must be sufficient to cover the losses in the parasitic resistances and transfer a voltage $V_1/2$ to the output in mode 2. During mode 1, C_2 discharges into the load.

Throughout mode 2, C_2 continues to discharge into the load; and C_1 is disconnected. In mode 3, C_2 is charged slightly higher than $V_1/2$, while the energy transfer capacitor, C_1, discharges into the load. In mode 4, C_2 is disconnected and C_1 continues to supply the load current.

The discharging times for C_1 and C_2 are calculated so that their respective voltages at the end of modes 4 and 2 are slightly less than $V_1/2$. This condition is required to support a constant average output voltage with a small ripple.

The duty cycle is determined by the on time of switches M_1 and M_3, and defined as

$$d = \frac{t_{on}}{T_s}, \tag{8.1}$$

where d is always less than 0.5. For other conversion ratios, the duration of modes 1 and 3 have to be adjusted in order to charge capacitors C_1 and C_2 to a voltage level slightly higher than the desired output voltage. Regulation of the output voltage can be achieved by applying a negative feedback on the PWM controller.

8.4 STATE–SPACE AVERAGING MODEL

In state–space averaging [4], the weighted average of the state–space descriptions of the switched topologies is taken to be the overall state–space description of the converter over each switching period. For a converter that commutates between two topologies during each switching cycle, the state–space equations for each topology are combined to form the overall state–space description.

Let the circuit description during the time interval dT be:

$$\begin{aligned} \dot{x} &= A_d x + B_d u, \\ y &= C_d x + D_d u. \end{aligned} \tag{8.2}$$

Let the circuit description during the time interval $(1 - d)T$ be:

$$\begin{aligned} \dot{x} &= A_{(1-d)} x + B_{(1-d)} u, \\ y &= C_{(1-d)} x + D_{(1-d)} u. \end{aligned} \tag{8.3}$$

The average state–space equations are then

$$\begin{aligned} \dot{x} &= Ax + Bu, \\ y &= Cx + Du, \end{aligned} \tag{8.4}$$

where

$$\begin{aligned} A &= dA_d + (1-d)A_{(1-d)}, \\ B &= dB_d + (1-d)B_{(1-d)}, \\ C &= dC_d + (1-d)C_{(1-d)}, \\ D &= dD_d + (1-d)D_{(1-d)}. \end{aligned} \tag{8.5}$$

By applying the state–space averaging method, the average state equation is obtained:

$$\begin{aligned} \dot{x} &= Ax + BV_1, \\ x &= [V_{C1} \quad V_{C2} \quad V_{C0}], \\ y &= V_2 = V_{C0}. \end{aligned} \tag{8.6}$$

Neglecting the input capacitor and the effective series resistance of the output capacitor, the state matrices are:

$$A = \begin{bmatrix} -\dfrac{(1/2)+d}{C_1(R_s+r_{C_1})} & 0 & \dfrac{1}{2C_1(R_s+r_{C_1})} \\ 0 & -\dfrac{(1/2)+d}{C_2(R_s+r_{C_2})} & \dfrac{1}{2C_2(R_s+r_{C_2})} \\ \dfrac{1}{2C_0(R_s+r_{C_1})} & \dfrac{1}{2C_0(R_s+r_{C_2})} & -\dfrac{1}{2C_0}\left(\dfrac{1}{R_s+r_{C_1}}+\dfrac{1}{R_s+r_{C_2}}+\dfrac{2}{R_L}\right) \end{bmatrix},$$

$$B = \begin{bmatrix} d/C_1(R_s+r_{C_1}) \\ d/C_2(R_s+r_{C_2}) \\ 0 \end{bmatrix}, \quad C = [0 \quad 0 \quad 1], \quad y = C(-A^{-1}B). \tag{8.7}$$

Solving (8.7) for the conversion ratio gives

$$\frac{V_2}{V_1} = \frac{1}{1+((R_s+r)/R_L)(1+(1/2d))}, \tag{8.8}$$

where $R_s = R_{s1} = \ldots = R_{s4}$ is the MOSFET's on resistance, r_{ci} is the capacitor's effective series resistance and R_L is the output resistance. Equation (8.8) was simulated for different values of the load resistance and the result is plotted in Figure 8.15, which shows the conversion ratio versus the duty cycle for this converter.

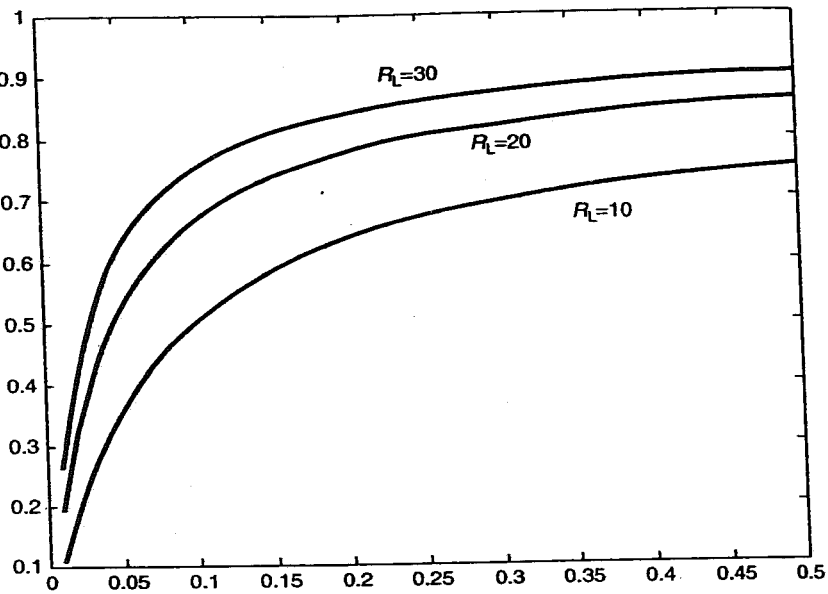


Figure 8.15 Conversion ratio versus duty cycle.

Figure 8.16 shows the voltages across the capacitors (points *a*, *b*, and out). Notice how the voltages at points *a* and *b* converge to the same value very rapidly, while the output voltage settles to 6.2 V. Figure 8.17 shows the gate signals switching at 1 MHz, and the output voltage ripple for a R_L = 20 Ω, resulting in a voltage ripple of 18 μV at a load current of 300 mA.

8.4.1 Step-Up Converter

The step-up SCC of Figure 8.18 is composed of the basic cell (C_1, C_2, S_2, S_3, and S_4), the voltage source V_1, the input switch S_1, the output switch S_5, the output capacitor C_o, and the load resistance, R_L. This circuit has two modes of operation, namely the charging and the discharging modes.

The equivalent circuits for the charging and discharging modes are shown in Figure 8.19(a) and (b), respectively. During the charging mode, the energy-transfer capacitors, C_1 and C_2, are charged in parallel; switches S_1, S_2, and S_3 are switched on. During the discharging mode, the capacitors C_1 and C_2 are connected in series by S_4 and discharged to the load through S_5. Therefore, the voltage levels obtained by the two capacitors during the charging mode are

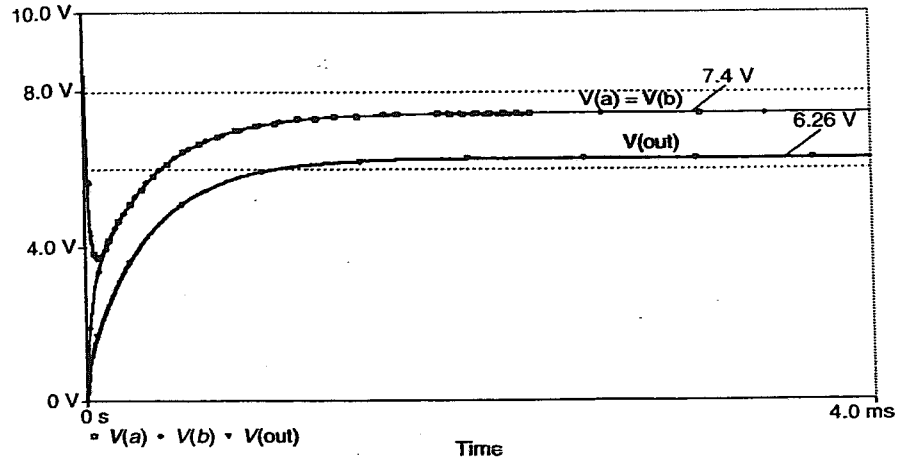


Figure 8.16 Voltage waveforms of the step-down SCC.

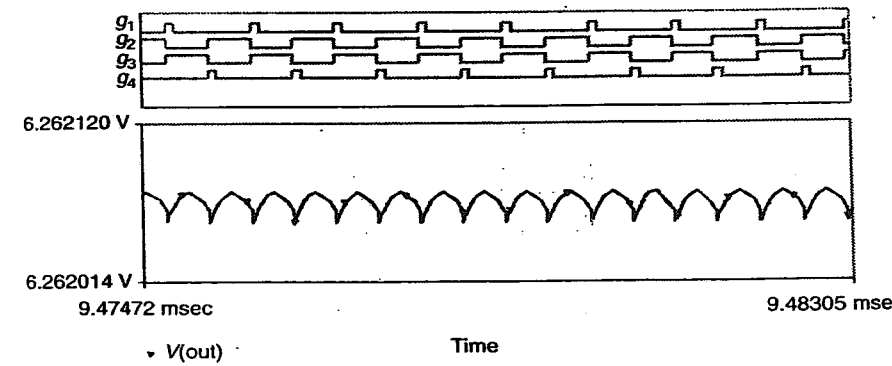


Figure 8.17 Gate signals and output voltage ripple.

added during the discharging mode to boost the output voltage up to $V_{C_1} + V_{C_2}$. The maximum output voltage supplied by this circuit is $2V_1$.

8.4.2 *n*-Stage Step-Down SCC

The n-stage step-down SCC shown in Figure 8.20 provides a good regulation of the output voltage [3]. N stages are stacked on top of the output capacitor, C_o. Each stage is composed by a capacitor C_i and three switches, S_i, S_{ig}, and S_{io}. The energy-transfer capacitors are charged in series by closing all the

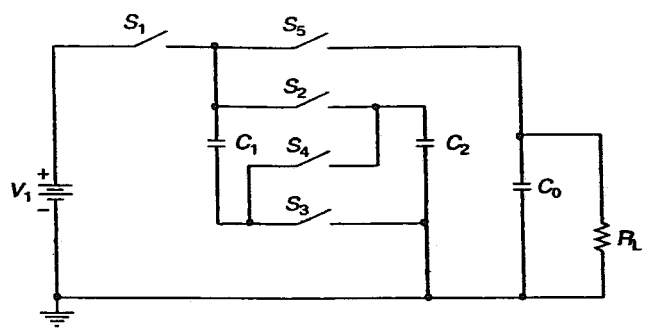


Figure 8.18 Step-up SCC.

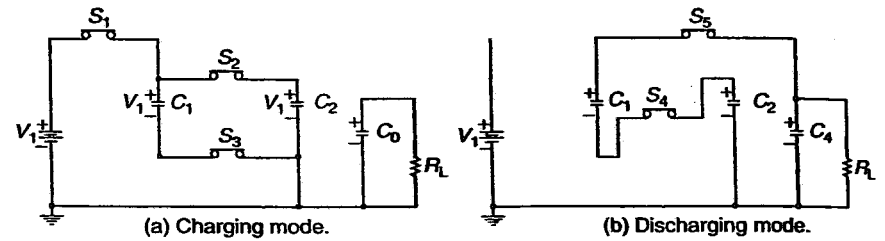


Figure 8.19 Equivalent circuits for the charging and discharging modes.

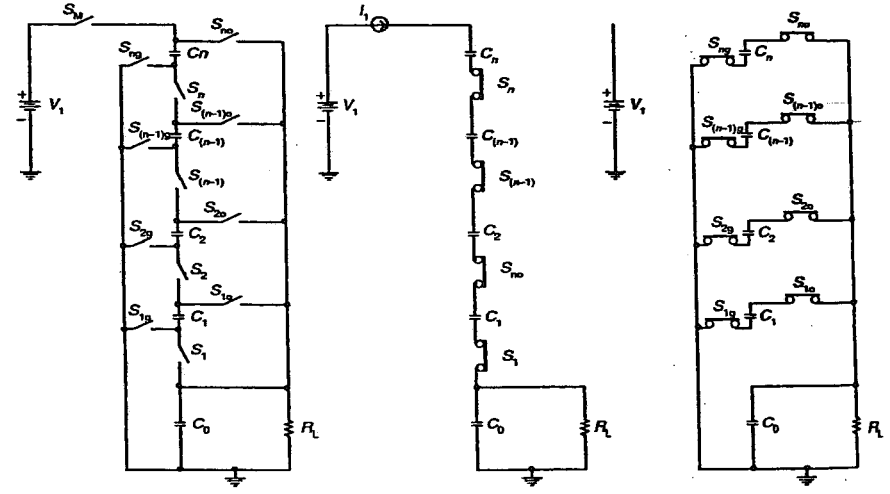


Figure 8.20 *n*-Stage step-down switching capacitor converter.

switches S_i (S_1 to S_n), as shown in Figure 8.20(b). The voltage level at the end of the charging mode is determined by the current supplied by the charging current source provided by the switch S_M functioning in the saturation region. Since the switches S_i are operated at a 50% duty cycle; the voltage at the energy-transfer capacitors is controlled by the gate to source voltage of the switch S_M, according to:

$$i_D = K(v_{GS} - V_T)^2. \tag{8.9}$$

This is the basic principle of current control scheme of SCC [5].

During the discharging mode, S_{ig} and S_{io} are switched on; all the other switches are open, giving the equivalent circuit of Figure 8.20(c). The energy-transfer capacitors are discharged in parallel, adding their respective currents. The resulting voltage can be stepped down to a maximum voltage V_1/n.

The steady-state output voltage is given by:

$$V_o = dI_{on}R_L. \tag{8.10}$$

8.4.3 *n*-Stage Step-Up SCC

When it is necessary to obtain an output voltage higher than $2V_1$, the SCC circuit of Figure 8.18 is inadequate. The *n*-stage step-up SCC shown in Figure 8.21 is a good alternative. *n* Stages are stacked on top of the output capacitor C_o. Each stage is comprised of a capacitor C_i and three switches, S_i, S_{ig}, and S_{io}. The energy-transfer capacitors are charged in parallel, by closing the switches S_{ig} and S_{io}, as shown in Figure 8.21(b). The voltage level at the end of the charging mode is determined by the current provided by the charging current source when the switch S_M is operating in the saturation region. Since the switches, S_i, S_{ig}, and S_{io} are operated at a 50% duty cycle; the voltage at the energy-transfer capacitors is controlled by the gate to source voltage of the switch S_M, according to:

$$i_D = K(v_{GS} - V_T)^2. \tag{8.11}$$

During the discharging mode S_i, S_{io}, and S_o are closed; all the other switches are open, giving the equivalent circuit of Figure 8.21(c). The energy-transfer capacitors are connected in series, adding their respective voltages. The resulting voltage can add up to nV_1. This voltage is then transferred to C_o, stepping up the input voltage to a higher level. With proper control, this circuit is capable of providing the step-up and the step-down functions. Other boost converter topologies and control strategies are discussed in Chung and Mok [6].

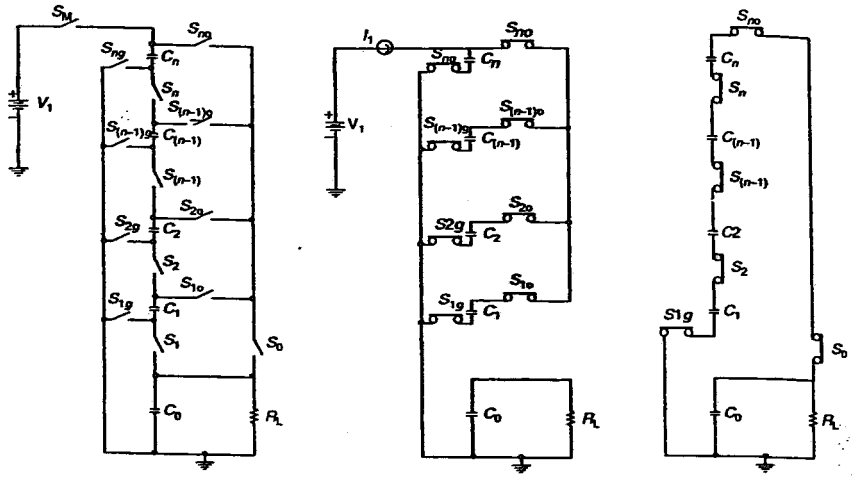


Figure 8.21 *n*-Stage step-up switching capacitor converter.

8.5 BI-DIRECTIONAL POWER FLOW SCC

The SCCs presented in Sections 8.4.1 to 8.4.3 are only capable of transferring power from the source to the load. For applications like DC motor control or battery charging it may be necessary to permit the power flow in both directions. This section presents various topologies of SCC with bi-directional power flow.

8.5.1 Step-Up Step-Down Converter

Chung and Chow [7] presented a SCC with bi-directional power flow based on a single structure that can provide the step-down and step-up functions. The basic bi-directional cell is shown in Figure 8.22. The cell converts electric power from the high-voltage side (HV) to the low-voltage side (LV). The switches S_i are operated in switched mode, while Q_s is either in cutoff, saturation, or the triode region. Q_s is used in the saturation region to control the charging current of the energy-transfer capacitor, C, thus, linearly increasing the capacitor's voltage. The drain current of Q_s is given by the MOSFET's equation in the saturation region:

$$i_D = K(v_{GS} - V_T)^2. \tag{8.12}$$

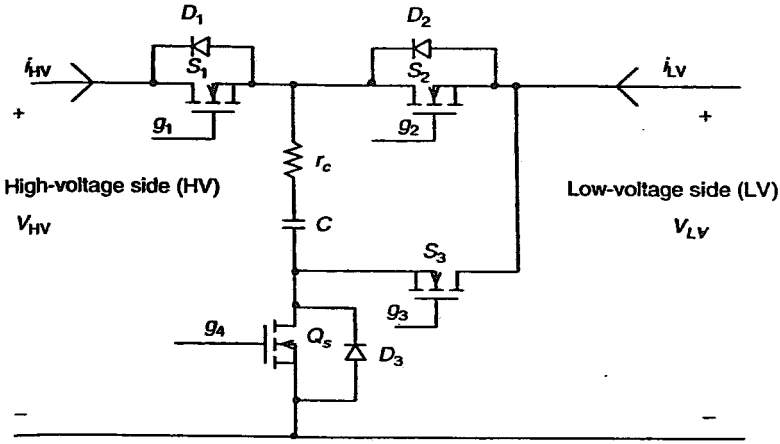


Figure 8.22 Basic bi-directional converter cell.

The cell can function either in the step-down or in the step-up modes. When the step-down operation is performed, energy is transferred from HV to LV. During the step-up operation, the power flow is from LV to HV.

8.5.1.1 Step-Down Operation

Figure 8.23 represents the two equivalent circuits for the step-down operation. Two modes of operation can be identified. During mode 1, S_1 is closed, Q_s is in saturation, and C is linearly charged with a current I_{sdch} for a duration $t_{on} = T_s/2$. At $T = t_{on}$, C will be charged to a voltage that is slightly higher than the voltage at LV, in order to compensate for parasitic resistances and diode voltage drops. During mode 2 ($T_s/2 < t < T_s$), S_2 and D_3 conduct. All other switches are open. C is then disconnected from HV and it transfers its stored energy to LV.

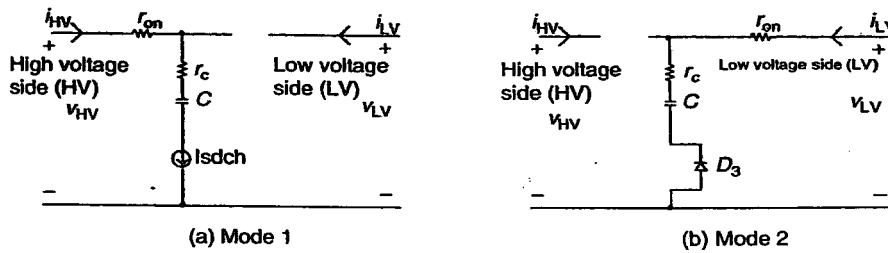


Figure 8.23 Equivalent circuits during the step-down operation.

8.5.1.2 Step-Up Operation

Figure 8.24 shows the two equivalent circuits for the step-up operation. During mode 1, D_2 is closed and Q_s is in saturation mode. All other switches are open. C is linearly charged from the LV side through D_2 and Q_s with a current I_{upch} for a duration $T_s/2$. At $T_s/2$, the capacitor is charged to a voltage level that is slightly higher than the voltage difference between the voltages at HV and LV; i.e., $V_c = V_{HV} - V_{LV}$, in order to compensate for the component losses. Mode 2 extends from $T_s/2$ to T_s; during this mode D_1 and S_3 conduct, while all the other switches are open. C is then connected in series with the LV side to supply energy to the HV side. The voltage at HV is then higher than at LV.

The complete bi-directional converter is shown in Figure 8.25, where two basic cells are connected in parallel. The input and output capacitors are needed to smooth the two terminal voltages. The two cells are operated in antiphase, that is, if the converter operates in the step-down mode, then both cells operate in the step-down mode. However, when cell 1 is in mode 1, cell 2

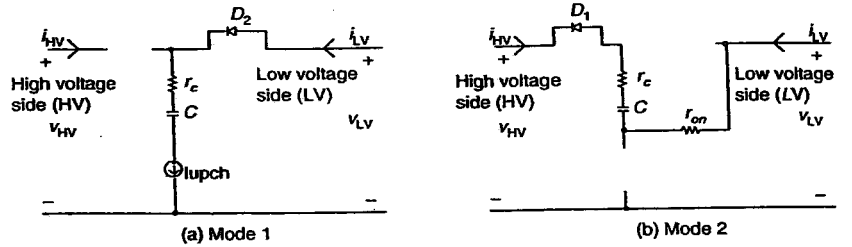


Figure 8.24 Equivalent circuits during the step-up operation.

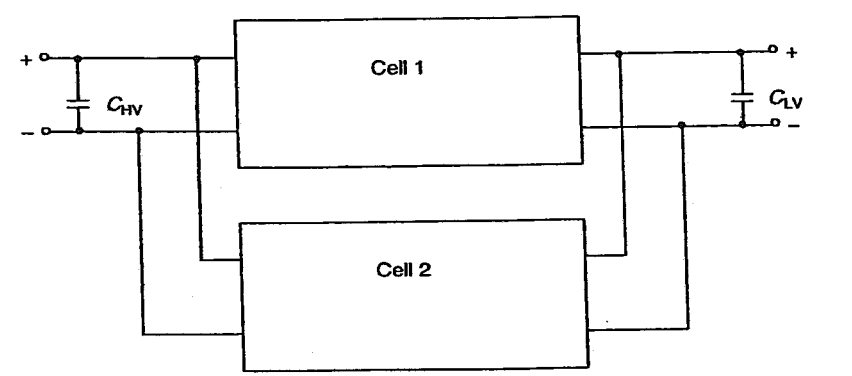


Figure 8.25 Bi-directional converter.

is in mode 2, and vice versa. For the step-down mode, the HV side is connected to a voltage source and the LV side is connected to a load, then

$$I_{HV} = I_{sdch}. \tag{8.13}$$

For the step-up mode, the HV side is connected to a load resistance while the LV side is connected to a voltage source. Thus,

$$I_{LV} = -i_{HV} + I_{upch}. \tag{8.14}$$

Since I_{sdch}, I_{upch}, and i_{HV} are constants, the input current at both sides is also constant and continuous, introducing only low-level EMI. The HV and the LV voltage levels for the steady-state operation can be found by applying the state-space averaging technique, resulting in

$$v_{LV} = I_{Ach} R_{LV} = K(V_{cont} - V_T)^2 R_{LV} \tag{8.15}$$

and

$$v_{HV} = I_{Bch} R_{HV} = K(V_{cont} - V_T)^2 R_{HV}. \tag{8.16}$$

It is obvious that the output voltage in both directions can be controlled by V_{cont}.

A typical application for a bi-directional converter is shown in Figure 8.26, where the HV side is connected to a rechargeable battery and the LV side is connected to the supply rail. In normal operation, the battery is charged from the supply rail through the converter. When an outage in the supply rail occurs, the converter will transfer the stored energy in the battery back to the supply rail.

8.5.2 Luo Converter

Luo et al. [8] introduced a switched capacitor four-quadrant DC–DC converter, namely the Luo converter. It can perform step-up or step-down DC–DC voltage conversion in all the four quadrants using a low switching frequency. Since the frequency is low compared to the classical converters, the EMI is very weak. It has been proven to provide high efficiency and high power. It is also potentially capable of achieving a high-output current that is needed to charge the modern automobile power supply systems. The Luo converter is shown in Figure 8.27. It consists of eight switches, two capacitors, the source voltage V_1, and the load voltage V_2 (e.g., a battery or DC motor back EMF). The energy-transfer capacitors, C_1 and C_2, have the same value. There are four modes of operation for this converter.

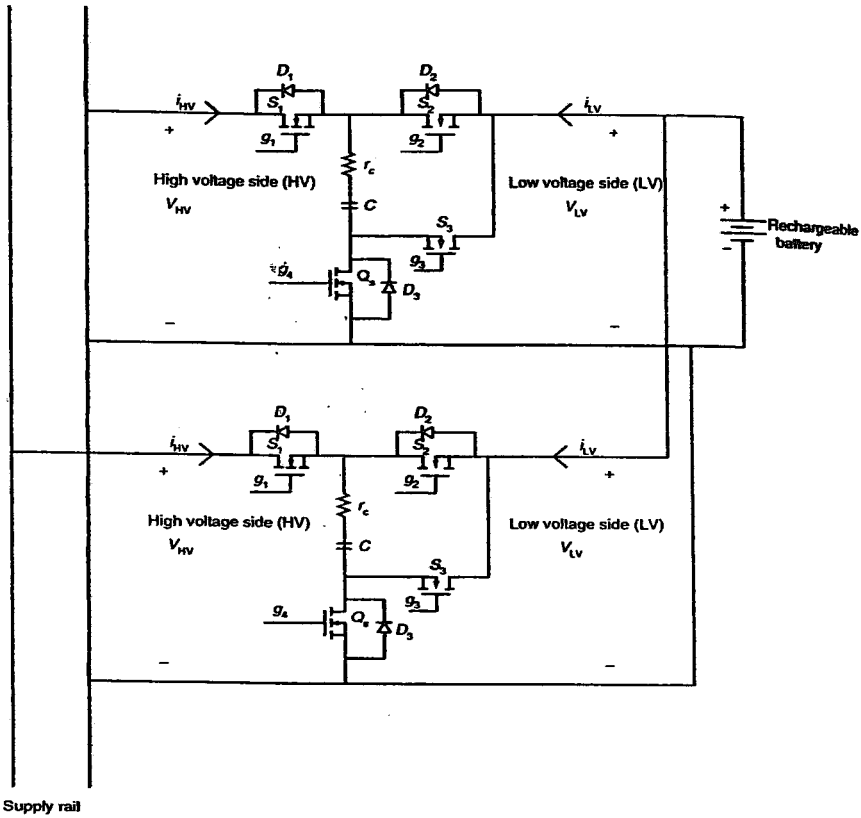


Figure 8.26 Bi-directional converter application.

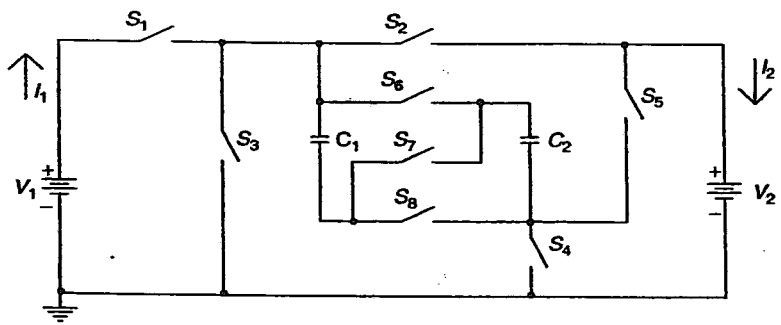


Figure 8.27 Switched capacitor Luo converter.

First quadrant operation: the energy is transferred from the source to the positive voltage load. This mode is also called the forward motoring operation. V_1, V_2, I_1, and I_2 are all positive.

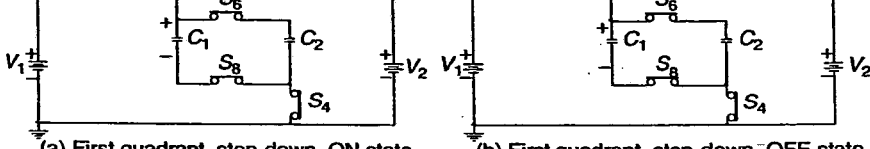
Second quadrant operation: the energy is transferred from the positive voltage load to the source. The second quadrant is also called the forward regenerative braking operation. V_1 and V_2 are positive, while I_1 and I_2 are negative.

Third quadrant operation: the energy is transferred from the source to the negative voltage load. This mode is also called the reverse motoring operation. V_1 and I_1 are positive, while V_2 and I_2 are negative.

Fourth quadrant operation: the energy is transferred from the negative voltage load to the source. The fourth quadrant is also called the reverse regenerative braking operation. V_1 and I_2 are positive, while I_1 and V_2 are negative.

Each mode of operation has two possible operating conditions, depending on the magnitudes of the input and output voltages; that is, $V_1 > |V_2|$ and $V_1 < |V_2|$. Therefore, there is a step-down mode and a step-up mode for the operation in each quadrant. Each condition has two states: ON and OFF. Usually, each state has a different duty cycle.

First quadrant operation. In this mode of operation, the capacitors C_1 and C_2 transfer the energy from the source to the load. The output voltage is positive. The equivalent circuits for the *step-down mode* ($V_1 > V_2$) are shown in Figure 8.28. Since $V_1 > V_2$, the two capacitors C_1 and C_2 are charged and discharged in parallel. During the ON state, the switches S_1, S_4, S_6, and S_8 are closed, while all the other switches are open. The two capacitors C_1 and C_2 are charged in parallel via the circuit $V_1-S_1-C_1//C_2-S_4$, and the voltage across the capacitors C_1 and C_2 increases according to the indicated polarity in Figure 8.28(a). During the OFF state, switches S_2, S_4, S_6, and S_8 are closed while all the other switches are open, resulting in the equivalent circuit of Figure 8.28(b). In this case, the capacitors $C_1//C_2$ are discharged via the circuit $S_2-V_2-S_4-C_1//C_2$, and the voltage across the capacitors C_1 and C_2 decreases.



(a) First quadrant, step-down, ON state. (b) First quadrant, step-down, OFF state.

Figure 8.28 Equivalent circuits for the first quadrant step-down operation.

The equivalent circuits for the *step-up mode* ($V_1 < V_2$) are shown in Figure 8.29. Since $V_1 < V_2$, the two capacitors C_1 and C_2 are charged in parallel and discharged in series.[2] During the ON state (Figure 8.29(a)), switches S_1, S_4, S_6, and S_8 are closed and all the other switches are open. In this case, capacitors $C_1//C_2$ are charged via the circuit $V_1-S_1-C_1//C_2-S_4$, and the voltage across the capacitors C_1 and C_2 increases. During the OFF state (Figure 8.29(b)), switch S_2, S_4, and S_7 are closed and all the other switches are open. In this case, capacitors C_1 and C_2 are discharged via the circuit $S_2-V_4-S_4-C_1-S_7-C_2$, and the voltages across the capacitors C_1 and C_2 decrease.

Second quadrant operation. In this mode of operation, capacitors C_1 and C_2 transfer the energy from the load to the source. The output voltage is positive. The equivalent circuits for the *step-up mode* ($V_1 > V_2$) are shown in Figure 8.30. Since $V_1 > V_2$, the voltage at the load has to be stepped-up to the source level; therefore, the two capacitors C_1 and C_2 are charged in parallel during the ON state and discharged in series during the OFF state. During the ON state (Figure 8.30(a)), the switches S_2, S_4, S_6, and S_8 are closed. In this case, the capacitors $C_1//C_2$ are charged via the circuit $V_2-S_2-C_1//C_2-S_4$, and the voltage across the capacitors C_1 and C_2 increases. During the OFF state, the switches S_1, S_4, and S_7 are closed, as shown in Figure 8.30(b). In this case, the capacitors C_1 and C_2 are dis-

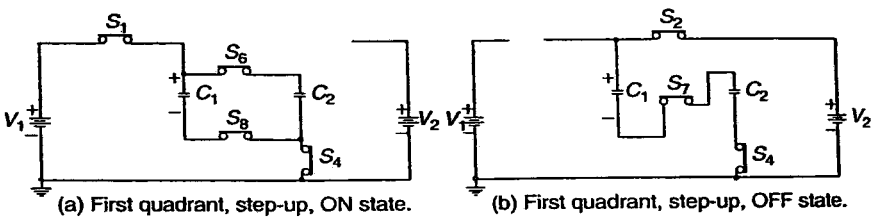


Figure 8.29 Equivalent circuits for the first quadrant step-up operation.

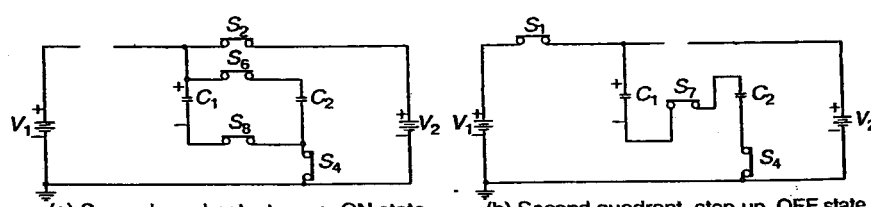


Figure 8.30 Equivalent circuits for the second quadrant step-up operation.

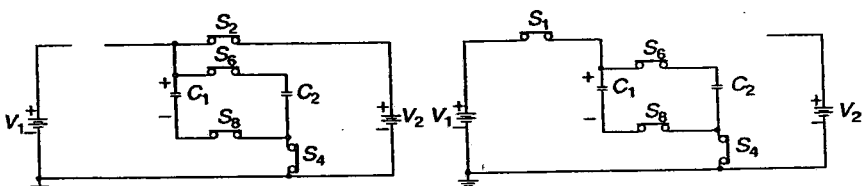
[2] This is the so-called voltage lift technique.

charged via the circuit $S_1-V_1-S_4-C_2-S_7-C_1$, thus, the voltages across the capacitors C_1 and C_2 decrease.

The equivalent circuits for the *step-down mode* ($V_1 < V_2$) are shown in Figure 8.31. Since $V_1 < V_2$, the two capacitors C_1 and C_2 are charged and discharged in parallel. During the ON state, the switches S_2, S_4, S_6, and S_8 are closed. In this case, the capacitors $C_1//C_2$ are charged via the circuit $V_2-S_2-C_1//C_2-S_4$; thus, the voltage across the capacitors C_1 and C_2 increases. During the OFF state, the switches S_1, S_4, S_6, and S_8 are closed. In this case, the capacitors $C_1//C_2$ are discharged via the circuit $S_1-V_1-S_4-C_1//C_2$, and the voltage across the capacitors C_1 and C_2 decreases.

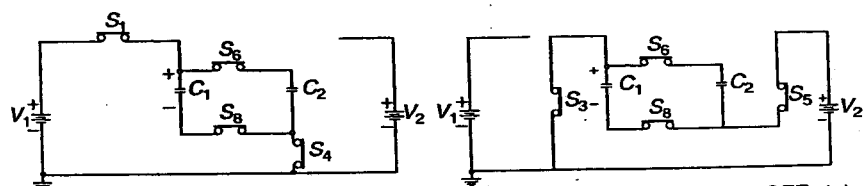
Third quadrant operation. In this mode of operation, the capacitors C_1 and C_2 transfer the energy from the source to the load. The output voltage, V_2, is negative. The equivalent circuits for the inverting *step-down mode* ($V_1 > |V_2|$) are shown in Figure 8.32. Since $V_1 > |V_2|$, the two capacitors C_1 and C_2 are charged in parallel. During the ON state (Figure 8.32(a)), the switches S_1, S_4, S_6, and S_8 are closed. In this case, the capacitors $C_1//C_2$ are charged via the circuit $V_1-S_1-C_1//C_2-S_4$, and the voltage across the capacitors C_1 and C_2 increases. During the OFF state (Figure 8.32(b)), the switches S_3, S_5, S_6, and S_8 are closed. The capacitors C_1 and C_2 are discharged via the circuit $S_3-V_2-S_5-C_1//C_2$ and the voltage across them decreases.

The equivalent circuits for the inverting *step-up mode* ($V_1 < |V_2|$) are shown in Figure 8.33. Since $V_1 < |V_2|$, the two capacitors C_1 and C_2 are



(a) Second quadrant, step-down, ON state. (b) Second quadrant, step-down, OFF state.

Figure 8.31 Equivalent circuits for the second quadrant step-down operation.



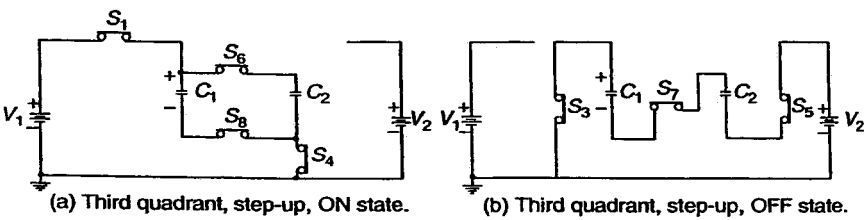
(a) Third quadrant, step-down, ON state. (b) Third quadrant, step-down, OFF state.

Figure 8.32 Equivalent circuits for the third quadrant step-down operation.

charged in parallel during the ON state and discharged in series during the OFF state. During the ON state (Figure 8.33(a)), the switches S_1, S_4, S_6, and S_8 are closed. The capacitors C_1 and C_2 are charged via the circuit $V_1-S_1-C_1//C_2-S_4$, increasing the voltage across the capacitors. During the OFF state (Figure 8.33(b)), the switches S_3, S_5, and S_7 are closed. The capacitors C_1 and C_2 are discharged via the circuit $S_3-V_2-S_5-C_1-S_7-C_2$, decreasing their voltages.

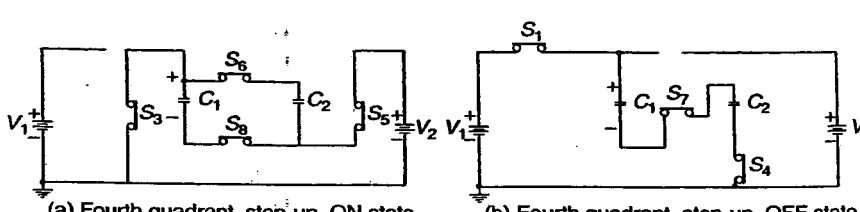
Fourth quadrant operation. In this mode of operation, capacitors C_1 and C_2 transfer the energy from the load to the source. The output voltage, V_2, is negative. The equivalent circuits for the inverting *step-up mode* ($V_1 > |V_2|$) are shown in Figure 8.34. Since $V_1 > |V_2|$, the two capacitors C_1 and C_2 are charged in parallel during the ON state and discharged in series during the OFF state. During the ON state (Figure 8.34(a)), the switches S_3, S_5, S_6, and S_8 are closed. In this case, the capacitors $C_1//C_2$ are charged via the circuit $V_2-S_3-C_1//C_2-S_5$, and the voltage across the capacitors C_1 and C_2 increases. During the OFF state (Figure 8.34(b)), the switches S_1, S_4, and S_7 are closed. The capacitors C_1 and C_2 are discharged via the circuit $S_1-V_1-S_4-C_2-S_7-C_1$ and the voltage across the capacitors decreases.

The equivalent circuits for the inverting *step-down mode* ($V_1 < |V_2|$) are shown in Figure 8.35. Since $V_1 < |V_2|$, the two capacitors C_1 and C_2 are charged and discharged in parallel. During the ON state (Figure 8.35(a)), the switches S_3, S_5, S_6, and S_8 are closed. In this case, the capacitors $C_1//C_2$



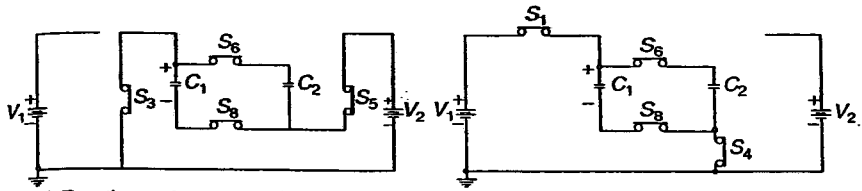
(a) Third quadrant, step-up, ON state. (b) Third quadrant, step-up, OFF state.

Figure 8.33 Equivalent circuits for the third quadrant step-up operation.



(a) Fourth quadrant, step-up, ON state. (b) Fourth quadrant, step-up, OFF state.

Figure 8.34 Equivalent circuits for the fourth quadrant step-up operation.



(a) Fourth quadrant, step-down, ON state. (b) Fourth quadrant, step-down, OFF state.

Figure 8.35 Equivalent circuits for the fourth quadrant step-down operation.

are charged via the circuit V_2–S_3–$C_1//C_2$–S_5, and the voltage across them increases. During the OFF state (Figure 8.35(b)), the switches S_1, S_4, S_6, and S_8 are closed. The capacitors C_1 and C_2 are discharged via the circuit S_1–V_1–S_4–$C_1//C_2$, and the voltage across them decreases.

8.6 RESONANT CONVERTERS

Hard switching SCCs have the disadvantages of high switching current that induces EMI and exposes the switches to high stresses. Also, the regulation of the output voltage is poor. Soft-switching SCC can alleviate some of these problems. In 1998, Cheng [9,10] presented a new topology of switched capacitor converters, which can operate at a high switching frequency with reduced EMI. The new circuit utilizes smaller numbers of switches, which switch at zero-current. Thus, the circuit can operate at a high switching frequency with a high efficiency. However, a small inductor is needed in this type of resonant SCC.

8.6.1 Zero-Current Switching

A family of zero-current switching switched capacitor converters, consisting of double mode, inverting mode, and half mode functions are proposed by Cheng [4]. These circuits use smaller number of active switches and diodes than the classical switched capacitor converter topologies. All the devices are zero-current switched; therefore it is suitable for the operation at high switching frequencies. The characteristic of zero-current switching minimizes the losses and the EMI, and hence, the switching frequency can be further increased, resulting in smaller capacitor sizes.

This circuit uses two controlled switching devices, two diodes, one resonant inductor, one energy-transfer capacitor, and one output filter capacitor. One switch is used to charge the energy-transfer capacitor and the other one is used to discharge it. The resonant inductor is usually very small, and hence, it can still be integrated.

Figure 8.36 shows a family of zero-current switching SCC [9]. Each circuit uses two controlled switches and a small resonant inductor. The resonant inductor, L_r, is connected in series with the energy-transfer capacitor to create a resonance cycle when each of the switches Q_1 or Q_2 is switched on. The switches are connected in series with the resonant inductor, creating a zero-current turn-on mechanism. Once the resonant current reaches the peak value, it decreases to zero; after that, it cannot reverse polarity because the diodes stop the current from reversing.

Figure 8.37 shows the simulated waveforms of the double-mode topology under steady-state conditions. The circuit parameters used in the simulation are: $f_s = 200\,\text{kHz}$, dead time $= 50\,\text{ns}$, $V_s = 50\,\text{V}$, $C_1 = 2.2\,\mu\text{f}$, $C_2 = 2.7\,\mu\text{f}$, $L_r = 0.1\,\mu\text{Hy}$, and $R_L = 50\,\Omega$.

The operation of the circuit can be described by four states of operation. The currents of the switches start resonating from zero and the conduction stops when the currents return to zero. This creates the zero-current turn-on and turn-off condition for the two switches. The duty-cycle of the two complementary switches is about 50% and can be varied to less than 50% if output voltage regulation is required.

State 1 (Figure 8.38(a)) $[t_o - t_1]$. When Q_2 is turned on at $t = t_0$, Q_1 is turned off; L_r and C_1 start to resonate. Due to L_r, Q_2 is turned on with zero current. C_2 is discharged to the load R_L. This state is represented by

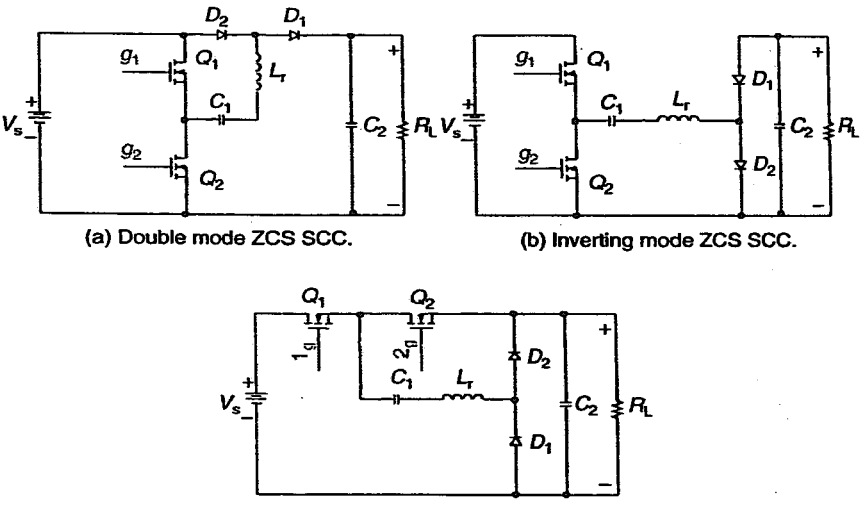


Figure 8.36 Family of the zero-current switching SCC.

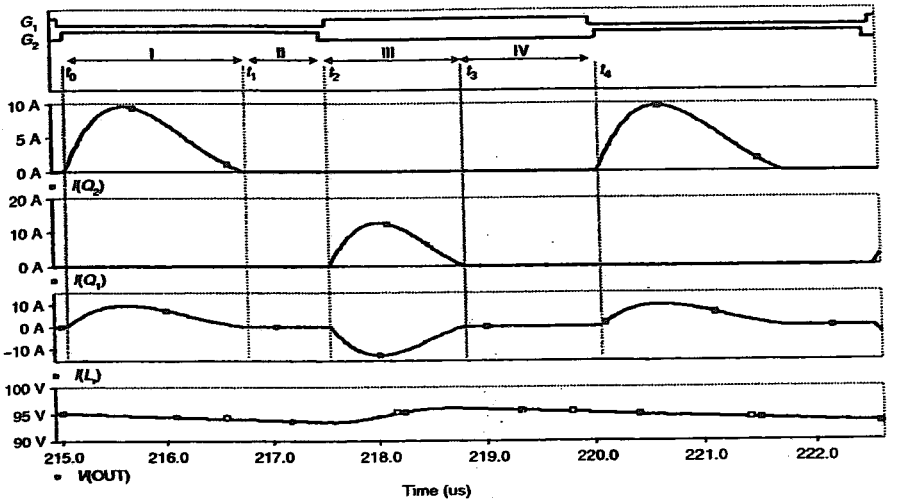


Figure 8.37 Simulated waveforms of the ZCS SCC.

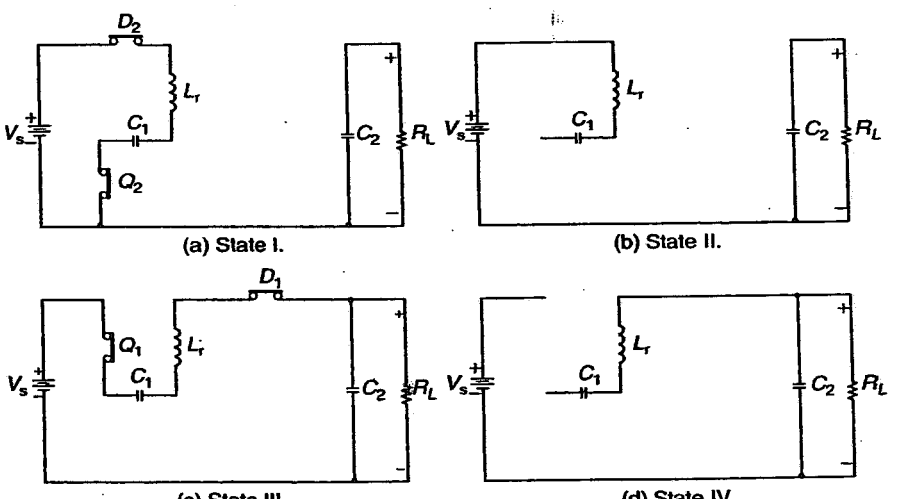


Figure 8.38 Equivalent circuits of the double-mode SCC.

$$i_{L_r} = \frac{V_s - V_{c10}}{L_r \omega_1} \sin(\omega_1 t), \qquad (8.17)$$
$$V_{c_1} = V_s + (V_{c10} - V_s)\cos(\omega_1 t),$$

where $V_{c_{10}}$ is the initial voltage of C_1 at $t = t_0$ and $\omega_1 = 1/\sqrt{L_r C_1}$. L_r and C_1 resonate for half a cycle and the resonance stops because D_1 and D_2, become reverse-biased.

State 2 (Figure 8.38(b)) $[t_1 - t_2]$. In this mode, the currents through the inductor and the switches are zero. C_2 is still discharging to the load. Q_2 is switched off at zero current at $t = t_2$.

State 3 (Figure 8.38(c)) $[t_2 - t_3]$. Q_1 is turned on with zero-current at $t = t_2$. L_r, C_1, and C_2 start to resonate. i_{L_r} begins increasing from zero towards the negative cycle. The resonance equations of the inductor and capacitors depend on the size of the load. Their equations for a large R_L can be approximated as:

$$\begin{aligned} i_{L_r} &= \frac{V_d}{L_r \omega_n} \sin(\omega_n t), \\ V_{c_1} &= \frac{V_d}{C_1 L_r \omega_n^2}(1 - \cos(\omega_n t)) + V_{c_{10}}, \\ V_{c_2} &= \frac{V_d}{C_2 L_r \omega_n^2}(1 - \cos(\omega_n t)) + V_{c_{20}}, \end{aligned} \tag{8.18}$$

where

$$\omega_n = 1/\sqrt{L_r C_p},\ C_p = C_1 // C_2 \quad \text{and} \quad V_d = (V_s - V_{c_{10}} - V_{c_{20}}). \tag{8.19}$$

This state terminates after i_{Lr} resonates back to zero, and D_1 and D_2 are reverse-biased.

State 4 (Figure 8.38(d)) $[t_3 - t_4]$. i_{Lr} is zero and C_2 is discharged to the load. Q_1 is turned off at zero current when $t = t_4$.

8.6.1.1 Condition of Zero-Current Switching

If the duty cycles of Q_1 and Q_2 are d_1 and d_2, respectively, the condition for zero-current switching of Q_1 is

$$d_1 T_s \geq \frac{\pi}{\omega_n}. \tag{8.20}$$

The condition for zero-current switching of Q_2 is

$$d_2 T_s \geq \frac{\pi}{\omega_1}, \tag{8.21}$$

where T_s is the switching period.

8.7 LOSSES ON SWITCHED-CAPACITOR POWER CONVERTERS [11]

One important fact, which many designers may tend to overlook, is the presence of losses in SCC. Consider the circuit of Figure 8.39, representing the series connection of a voltage source, an ideal switch, and a capacitor. Assume that the initial voltage on the capacitor is $v_c(0^-) = 0$, the voltage at the source is $V > 0$, and that the switch is closed at $t = 0$.

The Laplace transform of the current is given by

$$I(s) = sCV_c(s) \tag{8.22}$$

for an input voltage step

$$V_c(s) = \frac{1}{s} \tag{8.23}$$

in that case,

$$I(s) = CV \tag{8.24}$$

by applying the inverse Laplace transform; the temporal response is obtained as

$$i(t) = CV\partial(t). \tag{8.25}$$

The amount of lost energy during the charging process can be calculated by comparing the energy delivered by the source and the energy stored in the capacitor.

The energy delivered by the source is

$$E_v = \int_0^\infty Vi(t)\,dt = \int_{0-}^\infty CV^2\partial(t)\,dt = CV^2. \tag{8.26}$$

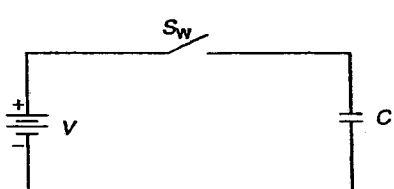


Figure 8.39 Evaluating SCC losses.

The energy stored in the capacitor is

$$E_c = \frac{1}{2}CV^2. \tag{8.27}$$

Therefore, the energy lost in the charging process is

$$E_v - E_c = \frac{1}{2}CV^2. \tag{8.28}$$

There are no lossy components in the circuit. Where did the energy go?

If a resistance R is connected in series with the capacitor, then the loss can be calculated by

$$\int_0^\infty [V - v_c(t)]\, i(t)\, dt. \tag{8.29}$$

Irrespective of the value of the resistor, the final energy in the capacitor remains the same, given by Equation (8.27). If we make the resistor smaller, in the limit when $R \to 0$, the current amplitude tends to ∞ and the loss still takes a finite value. Therefore, if a capacitor is charged by a voltage source whose magnitude differs from the initial voltage of the capacitor, then a fixed amount of energy is lost, equal to

$$i_c(\Delta V)^2 \tag{8.30}$$

will always accompany the charging process, where ΔV is the step change in the capacitor voltage.

PROBLEMS

8.1. Find the state–space average model for the step-up converter of Figure 8.1.
8.2. Find the voltage conversion ratio of the converter in problem 8.1.
8.3. Find the state–space average model for the step-up converter of Figure 8.18.
8.4. Find the voltage conversion ratio of the converter in problem 8.3.
8.5. Use Ref. [3] to determine Equation (8.10).
8.6. Calculate the efficiency of the step-up SCC of Figure 8.1: (a) consider ideal components, (b) consider the losses in the MOSFETS and diodes.

8.7. Obtain the state–space averaged model for the double mode ZCS SCC of Figure 8.36(a).
8.8. Analyze the inverting mode ZCS SCC of Figure 8.36(b) and derive the equations describing each operating mode.
8.9. Obtain the state–space averaged model for the inverting mode ZCS SCC of Figure 8.36(b).
8.10. Analyze the half mode ZCS SCC of Figure 8.36(c) and derive the equations describing each operating mode.
8.11. Obtain the state–space averaged model for the half mode ZCS SCC of Figure 8.36(c).

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9

Simulation of Switching Converters

9.1 INTRODUCTION

As the complexity of the power electronic circuits and systems increases, simulation has replaced breadboarding as a means of verifying and analyzing these complex circuits or systems. It has become a cost-efficient way to design many complex power electronic circuits or systems. Both large- and small-signal simulations can be performed on switching converters. Large-signal simulations yield the circuit behaviors such as the bias points for the switching converters. On the other hand, small-signal simulations usually require the knowledge of small-signal behaviors of switching converters through analytical models. It should be noted that small-signal simulations do not provide the normal electronic circuit behaviors as in actual switching converters. Both large- and small-signal simulations should be performed to better predict and verify the design for the switching converters.

In this chapter, several simulation tools such as SPICE, MATLAB, and Simulink are discussed. Some prior elementary knowledge in SPICE, MATLAB, and Simulink are assumed. The averaged state–space and transfer

function models for switching converters will be illustrated. Examples on the calculations of system poles, feedback gains, closed-loop system matrix, frequency, and transient responses will be discussed.

9.2 PSPICE CIRCUIT REPRESENTATION

SPICE is a general-purpose circuit analysis program widely used in the simulation of electronic circuits. SPICE is an acronym for Simulation Program with Integrated Circuit Emphasis. It was developed by the Integrated Circuit Group of the Electronic Research Laboratory at the University of California, Berkeley, California in the late 1960s and was released to the public in 1972 [1]. Over the years, SPICE has gone through many upgrades. The most recent version, SPICE3, is written in C language for easier portability. SPICE became popular when MicroSim, in 1984, introduced a personal-computer (PC) version of SPICE known as PSpice. The availability of the student-version of PSpice has revolutionized many electrical engineering curriculums. This is evident by the addition of PSpice utilizations to many popular electrical engineering textbooks. MicroSim was acquired by OrCad, and the latter was acquired by Cadence. At the time this book is written, the Cadence Suite 2002 Lite version of PSpice is available free for users. There are other free evaluation versions of SPICE-based circuit simulators from other vendors as well, such as the Electronics Workbench and Intusoft SPICE ICAP/4. The use of SPICE is increasing among the electrical engineering professionals, at the point that it is becoming an industrial standard. Most electronic component vendors now provide Spice model for their products.

As in many other circuit simulation programs, PSpice requires accurate circuit element models in order to faithfully simulate the operation of the switching converter. PSpice remains a viable simulation tool for the switching converter despite its many limitations.

Difficulties in PSpice simulation of switching converters arise from the fact that practical switching converters are switching systems with feedback. Switching converters with multiple feedback paths sometimes fail to converge or take considerable time to do so using the PSpice default conditions. Performing transient analysis on switching converter circuit often takes a considerable execution time, since the internal time step must be short compared to the switching period. In general, simulations of switching converters must extend over a few switching cycles to reach their steady-state conditions. Many of the PSpice simulations of the switching converters presented in this chapter can be performed using the student or the Lite versions of PSpice, which are limited versions of the full simulation tool.

Four different methods of representing a switching converter in PSpice are discussed. The classical text file input in a .CIR file is replaced by graphical input files in the latter versions of PSpice. Based on the student version of OrCad PSpice 9.2, a switching converter is represented by control blocks and behavioral models, which permits a rapid implementation to check its functionality. A more accurate simulation, using vendor-provided controller models, can be performed later. Two examples showing how to evaluate an open-loop and a closed-loop switching converters will be illustrated. Some guidelines to solve the common convergence problems in PSpice are discussed.

9.3 PSPICE SIMULATIONS USING .CIR

The first versions of Spice used a text file with a .CIR extension containing the circuit description as the circuit input file. The actual versions of Spice support a graphical input interface that automatically generates the .CIR file. We do not recommend the use of the text file input method since the graphical input is more easily interpreted, unless you need to write your own subcircuit or modify an existing one. Nevertheless, for the sake of completeness, we dedicate this subsection to an example of the circuit file description. Vendor models (subcircuits or macromodels) are often provided as a text file according to the .CIR syntax.

9.3.1 An Ideal Open-Loop Buck Converter

An ideal buck converter can be simulated using a pulse voltage source to replace the switching transistor as shown in Figure 9.1. The input voltage source is a pulse train having an amplitude equal to the DC input voltage and a duty cycle identical to the steady-state duty cycle of the switching converter. This is evident from the nonlinear continuous equivalent circuit of the ideal buck converter shown in Figure 6.47. Assuming a switching frequency

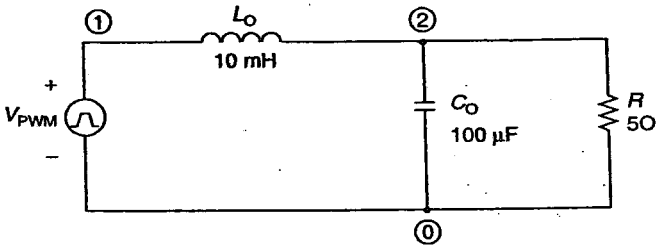


Figure 9.1 An ideal buck converter with a pulse voltage source.

of 1 kHz and a steady-state duty cycle of 50%, the program listing is as follows:

```
Open-loop buck converter simulation
*SWITCHING FREQUENCY = 1 KHZ; DUTY CYCLE = 50%
VPWM 1 0 PULSE(0 10 0 1US 1US 0.5MS 1 MS)
*PULSE PWM SOURCE: PULSED VOLTAGE = 10 V, RISE TIME = 1 US,
*FALL TIME = 1 US, PULSE WIDTH = 500 US, PERIOD = 1 MS.
L0 1 2 10M
C0 2 0 100U
RL 2 0 5
.TRAN 50US 20MS
.OPTION ITL5 = 0
.PROBE
.END
```

The PROBE statement is to activate the PSpice graphic postprocessor that calculates and displays the waveforms. The 50 μs transient step yields 200 switching cycles for a total of 400 iterations. Since PSpice continuously adjusts the time step for the transient analysis, it actually takes more than 400 iterations to complete the simulation. The ITL5 = 0 on the OPTION statement resets the transient analysis iteration limit to enable PSpice to execute more than 5000 transient analysis iterations.

PSpice calculates the DC bias points before the execution of the transient analysis. Figure 9.2 shows the output voltage, the inductor current, and the capacitor current waveforms of the simulated converter. The output voltage reaches its steady-state value of 5 V at about 5 ms, which corresponds to five switching cycles. As shown, the inductor and capacitor currents are in phase with each other, but they lead the output voltage by 90°. The output ripple voltage and the inductor ripple current are 300 mV and 0.4 A, respectively, as shown in Figure 9.2. The capacitor ripple current is 235 mA. The average capacitor current is initially positive since it does not store any energy at the beginning of the simulation. However, the average capacitor current is zero during the steady-state operation, as shown in Figure 9.2. The theoretical output ripple voltage according to Equation (2.20) is

$$\Delta v_o = \frac{V_s D(1-D)}{8 f_s^2 LC} = \frac{10(0.5)^2}{8(1000)^2 \cdot 10 \times 10^{-3} \cdot 100 \times 10^{-6}}$$
$$= 0.3125\,\text{V} \tag{9.1}$$

in comparison to the simulated value of 0.3 V. The theoretical inductor ripple current from Equation (2.14) is

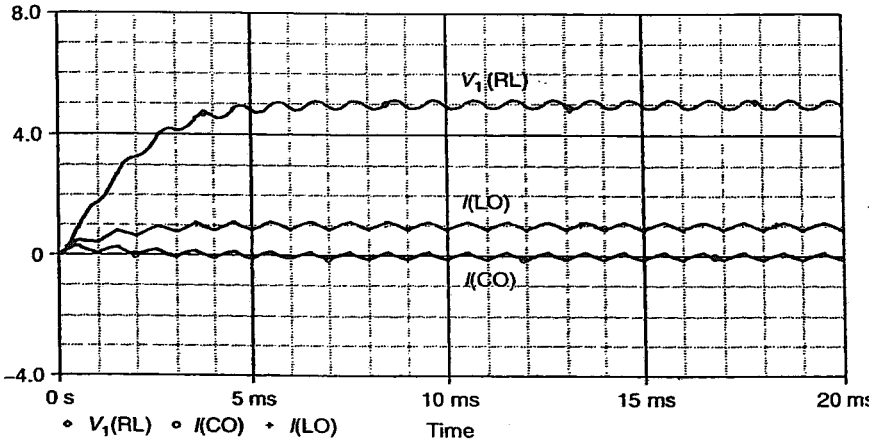


Figure 9.2 Output voltage (V_1(RL)), inductor current (I(LO)) and capacitor current (I(CO)) waveforms of the simulated buck converter with an output inductance of 10 mH.

$$\Delta I = \frac{DV_s(1-D)}{f_s L} = \frac{0.5(10)(1-0.5)}{1000 \times 10 \times 10^{-3}} = 0.25\,\text{A}, \tag{9.2}$$

which is in good agreement with the simulated inductor ripple current of 0.25 A. The inductor ripple current is approximately equal to the capacitor ripple current, because there is no load modulation.

Increasing the output inductance of the buck converter to 50 mH reduces the output ripple voltage and the inductor ripple current to 60 mV and 50 mA, respectively, as shown in Figure 9.3. The capacitor ripple current also reduces to 47 mA. These reductions are expected in accordance with Equations (2.20) and (2.14). However, the output voltage response is more sluggish compared with the buck converter with a 10-mH output inductor. It reaches its steady-state value at about 50 ms or 50 switching cycles.

Decreasing the output inductance to 5 mH increases its output ripple voltage and inductor ripple current to 0.6 V and 0.5 A, respectively, as shown in Figure 9.4. The capacitor ripple current also increases to 479 mA; however, the output voltage response depicts an underdamped characteristic. It reaches its steady-state value at about 4 ms. The onset of the discontinuous mode of operation for a constant load current occurs at about 1.25 mH, as predicted from Equation (2.31). Figure 9.5 shows the waveforms of the simulated converter with an output inductance of 1.25 mH. Although the average output voltage remains at about 5 V, the ripple voltage increases

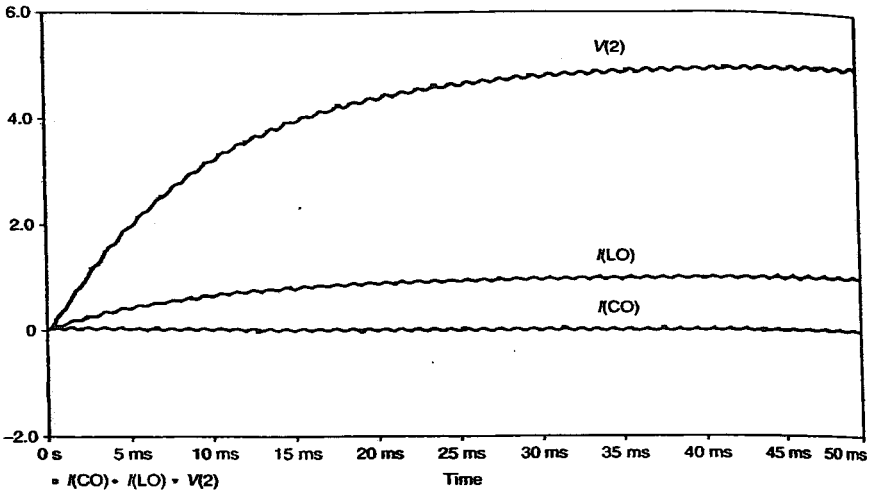


Figure 9.3 Output voltage ($V(2)$), inductor current ($I(LO)$), and capacitor current ($I(CO)$) waveforms of the simulated buck converter with an output inductance of 50 mH.

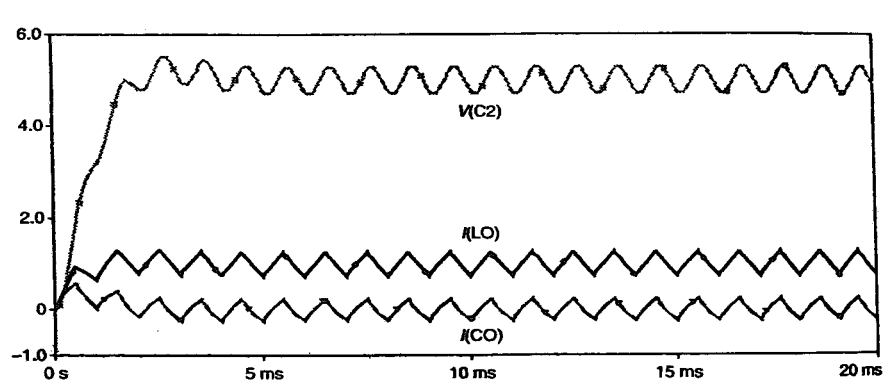


Figure 9.4 Output voltage ($V(2)$), inductor current ($I(LO)$), and capacitor current ($I(CO)$) waveforms of the simulated buck converter with an output inductance of 5 mH.

to 2.3 V. In addition, the steady-state inductor current begins to show discontinuities and reaches a peak value of 1.96 A. The simulated output capacitor ripple current is 1.9 A. Increasing the output capacitance from 100 to 500 μF, while keeping the output inductance at 10 mH, yields an underdamped output

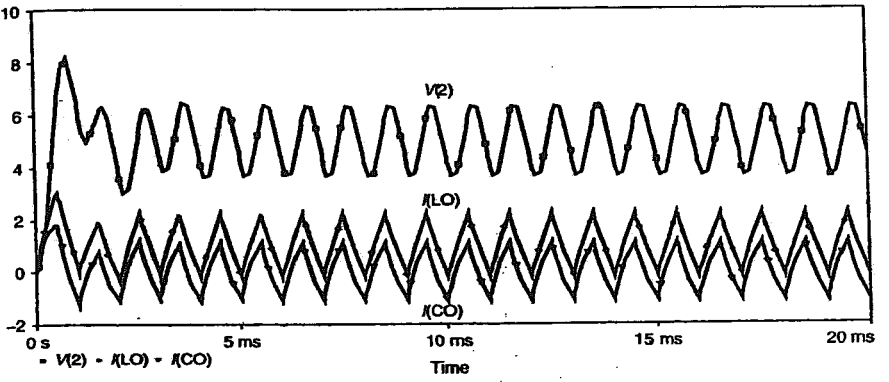


Figure 9.5 Output voltage ($V(2)$), inductor current ($I(LO)$), and capacitor current ($I(CO)$) waveforms of the simulated buck converter with an output inductance of 1.25 mH.

voltage response, as shown in Figure 9.6. The output voltage overshoots to 6 V and reaches its steady-state value at about 25 ms or 25 switching cycles. The output ripple voltage as well as the inductor ripple current, decrease to 60 mV and 0.25 A, respectively. The capacitor ripple current is approximately 0.25 A. Increasing the output capacitance to 100 μF, while keeping the same inductance of 1.25 mH yields an output ripple voltage of 0.57 V, an inductor ripple current of 1.96 A and a capacitor ripple current of about 1.96 A, as

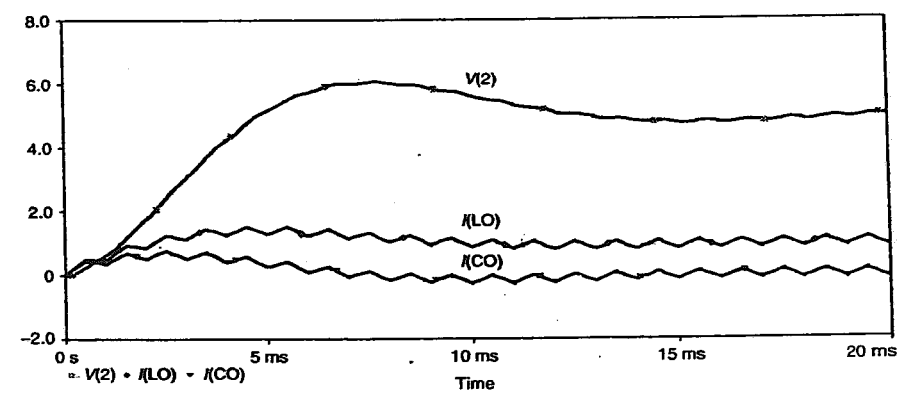


Figure 9.6 Output voltage ($V(2)$), inductor current ($I(LO)$), and capacitor current ($I(CO)$) waveforms of the simulated buck converter with an output capacitance of 500 μF and output inductance of 10 mH.

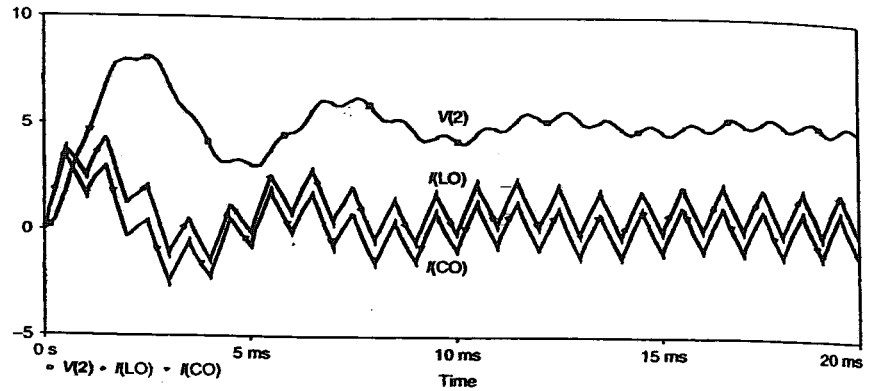


Figure 9.7 Output voltage ($V(2)$), inductor current ($I(LO)$), and capacitor current ($I(CO)$) waveforms of the simulated buck converter with an output capacitance of 500 μF and output inductance of 1.25 mH.

shown in Figure 9.7. It can be seen that the increase in output capacitance only reduces the output ripple voltage according to Equation (2.20). The inductor and capacitor ripple current waveforms are similar to the case of a 100-μF-output capacitor since the ripple components of the signal are inversely proportional to the output inductance and not the output capacitance.

The harmonic contents of the output voltage and input current can be obtained by performing a Fourier analysis using PSpice with the addition of the following statement to the previous program listing:

```
.FOUR 1 KHZ V(2)
```

Note that Fourier analysis must be performed in conjunction with transient analysis. Table 9.1 shows the Fourier analysis results for the output voltage and input current of the simulated buck converter with an output inductance of 10 mH and an output capacitance of 100 μF. As can be seen, only the odd harmonics of the output voltage and the input currents are significant. The fundamental harmonic components of the output voltage and input current are 0.14 V and 0.1 A, respectively. The third and higher harmonic components are progressively smaller.

The output inductance and capacitance were increased to 50 mH and 500 μF, respectively, and the Fourier analysis was obtained. Increasing the output inductance and output capacitance reduces the harmonic content of the converter as can been inferred by comparison of the values in Table 9.1 to Table 9.4.

Table 9.1 Fourier Components of the Output Voltage of the Simulated Buck Converter with $L = 10\,\text{mH}$ and $C = 100\,\mu\text{F}$

**** FOURIER ANALYSIS

FOURIER COMPONENTS OF TRANSIENT RESPONSE V(2)

DC COMPONENT = 5.000999E+00

HARMONIC NO.	FREQUENCY (HZ)	FOURIER COMPONENT	NORMALIZED COMPONENT	PHASE (DEG)	NORMALIZED PHASE (DEG)
1	1.000E+03	1.435E−01	1.000E+00	−1.585E+02	0.000E+00
2	2.000E+03	1.327E−05	9.252E−05	−1.266E+02	1.904E+02
3	3.000E+03	2.902E−03	2.023E−02	9.671E+01	5.723E+02
4	4.000E+03	5.810E−06	4.050E−05	−8.770E+01	5.464E+02
5	5.000E+03	4.695E−03	3.273E−02	1.289E+02	9.216E+02
6	6.000E+03	5.248E−06	3.658E−05	1.499E+02	1.101E+03
7	7.000E+03	1.368E−03	9.538E−03	−2.745E+01	1.082E+03
8	8.000E+03	4.318E−06	3.010E−05	−6.585E+01	1.202E+03
9	9.000E+03	1.799E−03	1.254E−02	1.437E+02	1.571E+03

Table 9.2 Fourier Components of the Input Current of the Simulated Buck Converter with $L = 10\,\text{mH}$ and $C = 100\,\mu\text{F}$

**** FOURIER ANALYSIS

FOURIER COMPONENTS OF TRANSIENT RESPONSE I(LO)

DC COMPONENT = 1.000200E+00

HARMONIC NO.	FREQUENCY (HZ)	FOURIER COMPONENT	NORMALIZED COMPONENT	PHASE (DEG)	NORMALIZED PHASE (DEG)
1	1.000E+03	1.034E−01	1.000E+00	−8.972E+01	0.000E+00
2	2.000E+03	1.559E−05	1.508E−04	−1.986E+01	1.596E+02
3	3.000E+03	1.154E−02	1.116E−01	−9.151E+01	1.776E+02
4	4.000E+03	5.996E−06	5.798E−05	−2.582E+01	3.331E+02
5	5.000E+03	4.179E−03	4.041E−02	−9.160E+01	3.570E+02
6	6.000E+03	3.884E−06	3.755E−05	−1.957E+01	5.187E+02
7	7.000E+03	2.101E−03	2.032E−02	−9.289E+01	5.351E+02
8	8.000E+03	3.625E−06	3.506E−05	−2.004E+01	6.977E+02
9	9.000E+03	1.300E−03	1.257E−02	−9.085E+01	7.166E+02

9.3.2 Buck Converter with an Ideal Switch

An ideal switch is often used to model the switching transistor in the initial simulation of a switching converter. The use of ideal switch can reduce the frequent convergence problems, which occur in PSpice due to discontinuities in the device equations of the switching transistors. It can also eliminate

Table 9.3 Fourier Components of the Output Voltage of the Simulated Buck Converter with $L = 50\,\text{mH}$ and $C = 500\,\mu\text{F}$

**** FOURIER ANALYSIS

FOURIER COMPONENTS OF TRANSIENT RESPONSE *V*(2)

DC COMPONENT = 5.001000E+00

HARMONIC NO.	FREQUENCY (HZ)	FOURIER COMPONENT	NORMALIZED COMPONENT	PHASE (DEG)	NORMALIZED PHASE (DEG)
1	1.000E+03	5.763E−03	1.000E+00	−1.714E+02	0.000E+00
2	2.000E+03	6.290E−07	1.091E−04	−1.641E+02	1.787E+02
3	3.000E+03	2.280E−04	3.955E−02	6.387E+01	5.780E+02
4	4.000E+03	1.681E−07	2.917E−05	−3.370E+01	6.518E+02
5	5.000E+03	2.217E−04	3.847E−02	1.228E+02	9.797E+02
6	6.000E+03	2.839E−07	4.927E−05	1.272E+02	1.155E+03
7	7.000E+03	7.123E−05	1.236E−02	−1.278E+01	1.187E+03
8	8.000E+03	1.692E−07	2.935E−05	−3.977E+01	1.331E+03
9	9.000E+03	7.993E−05	1.387E−02	1.354E+02	1.678E+03

Table 9.4 Fourier Components of the Input Current of the Simulated Buck Converter with $L = 50\,\text{mH}$ and $C = 500\,\mu\text{F}$

**** FOURIER ANALYSIS

FOURIER COMPONENTS OF TRANSIENT RESPONSE *I*(*LO*)

DC COMPONENT = 1.000200E+00

HARMONIC NO.	FREQUENCY (HZ)	FOURIER COMPONENT	NORMALIZED COMPONENT	PHASE (DEG)	NORMALIZED PHASE (DEG)
1	1.000E+03	2.032E−02	1.000E+00	−9.006E+01	0.000E+00
2	2.000E+03	3.053E−06	1.502E−04	−1.984E+01	1.603E+02
3	3.000E+03	2.282E−03	1.123E−01	−9.071E+01	1.795E+02
4	4.000E+03	1.204E−06	5.922E−05	−2.555E+01	3.347E+02
5	5.000E+03	8.251E−04	4.060E−02	−9.183E+01	3.585E+02
6	6.000E+03	7.589E−07	3.734E−05	−1.917E+01	5.212E+02
7	7.000E+03	4.181E−04	2.057E−02	−9.226E+01	5.381E+02
8	8.000E+03	7.256E−07	3.570E−05	−1.999E+01	7.005E+02
9	9.000E+03	2.565E−04	1.262E−02	−9.109E+01	7.194E+02

problems introduced by the driver circuitry. There are two types of ideal switches in PSpice: voltage-controlled switch and current-controlled switch. Figure 9.8 shows the circuit symbol for a voltage-controlled switch.

The designation for the voltage-controlled switch PSpice is *S*. The general statement for this type of switch is

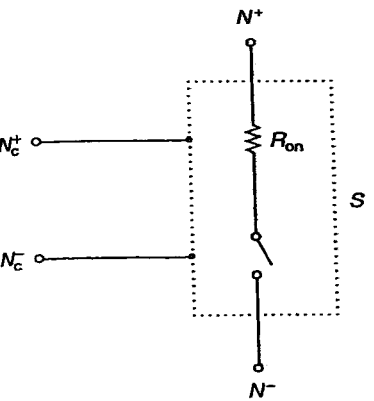


Figure 9.8 Symbol of a voltage-controlled switch.

```
S<name> N+ N− NC+ NC− SNAME
.MODEL SNAME VSWITCH (RON = 0.01 ROFF = 1E + 7 VON = 0.7 VOFF = 0)
```

where N+ and N− are the two nodes of the switch. NC+ and NC− are the positive and negative nodes of the controlling voltage source, respectively. The current is assumed to flow from the N+ node through the switch to the N− node. The on-resistance of the switch is 0.01 Ω when the voltage across the switch is equal to or greater than 0.7 V. The off-resistance is 10 MΩ when the voltage across the switch is 0 V. A rather complex relationship exits between the controlling voltage and the resistance when the controlling voltage is between 0 and 0.7 V. In this voltage range, the resistance is a function of the voltage. The off-resistance, ROFF, should be less than 1/GMIN [1] or 10^{12} Ω, since the default value of GMIN is 10^{-12} S. The on-resistance, RON, should be greater than zero. Thus, the ratio of ROFF to RON should be less than 10^{12}. Figure 9.9 shows the circuit symbol for a current-controlled switch.

The PSpice designation for a current-controlled switch is *W*. The general statement for this type of switch is

```
W<name> N+ N− VN WNAME
.MODEL WNAME ISWITCH (RON = 0.01 ROFF = 1E + 7 ION = 0.1
IOFF = 0)
```

where N+ and N− are the two nodes of the switch. VN is an independent voltage source from which the controlling current flows. The on-resistance of the switch is 0.01 Ω when a current of 0.1 A or greater flows through the controlling source VN. The off-resistance is equal to 10 MΩ when the

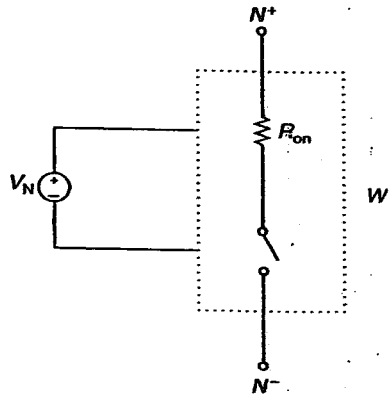


Figure 9.9 Symbol of a current-controlled switch.

controlling current is zero and the switch is open. In the simulation of a switching converter using an ideal switch, an infinitely high off-resistance or zero on-state resistance often results in convergence problems during transient analysis due to infinitely large current or voltage associated with storage elements. Therefore, the off-state or on-state resistance of an ideal switch should be limited to practically acceptable values. Figure 9.10 shows the circuit schematic of an open-loop buck converter with an ideal voltage-controlled switch replacing the switching transistor.

Assuming a switching frequency of 1 kHz and a steady-state duty cycle, D of 50%, the program listing for the ideal buck converter is given below:

```
OPEN-LOOP BUCK CONVERTER WITH AN IDEAL SWITCH
* SWITCHING FREQUENCY = 1 KHZ; DUTY CYCLE = 50%
```

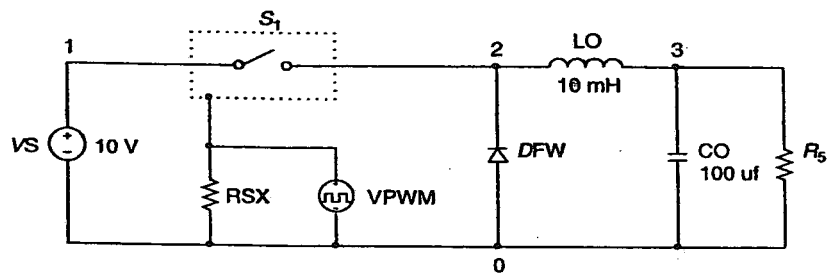


Figure 9.10 Circuit schematic of an open-loop buck converter with a voltage-controlled switch replacing the switching transistor.

```
VS 1 0 10.0
VPWM 100 101 PULSE(0 1 0 1US 1US 500US 1MS)
S1 1 2 100 101 SX
RSX 100 0 10G
DFW 0 2 D1
L0 2 3 10M
C0 3 0 100U
RL 3 0 5
.MODEL SX VSWITCH (RON = 0.01 ROFF = 1E+7 VON = 1 VOFF = 0)
.MODEL D1 D
.TRAN 0.05MS 20MS
.PROBE
.END
```

The resistor RSX is necessary to satisfy the PSpice requirement of having at least two circuit elements connected to a node. Its 10-GΩ resistance is essentially an open circuit.

Figure 9.11 shows the output voltage, the inductor current, and the capacitor current waveforms of the simulated buck converter. These waveforms are similar to those shown in Figure 9.2. Figure 9.12 shows the steady-state waveform for the current flowing through and the voltage across the output capacitor. In this case, the capacitor ripple voltage lags the current ripple by 90°.

In some simulations, it is desirable to define the initial conditions of the switching converter. This is essentially true for switching converters with a large output capacitance and a large output inductance. Otherwise, it may

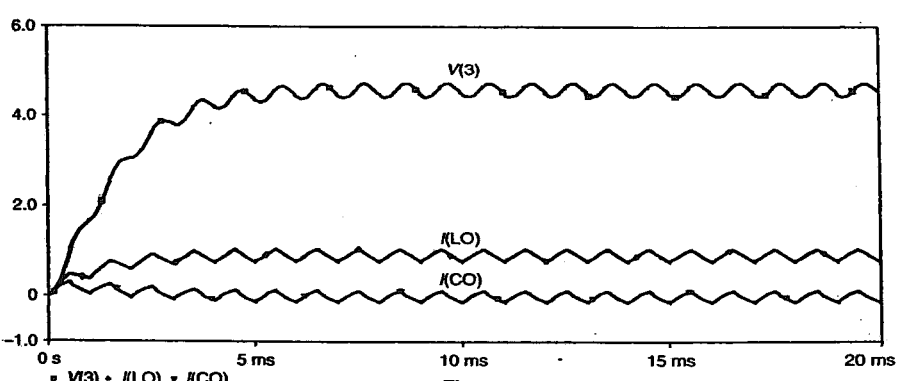


Figure 9.11 Output voltage ($V(3)$), inductor current ($I(LO)$), and capacitor current ($I(CO)$) waveforms of the simulated buck converter with an ideal switch.

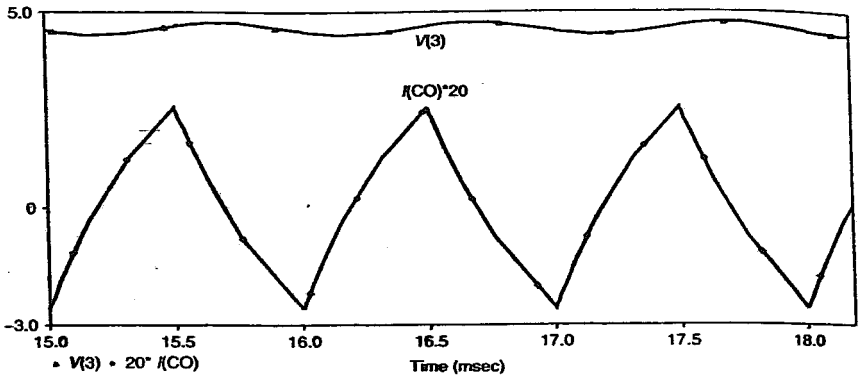


Figure 9.12 Steady-state waveforms of the current flowing through the output capacitor (I(CO)) and the voltage across the output capacitor (V(3)) of the simulated buck converter with an ideal switch.

take a considerable long execution time to perform a steady-state analysis on these switching converters. Performing transient analysis with initial conditions can be accomplished by inserting the initial conditions at the end of the statements and modifying the TRAN statement as follows:

```
LO 2 3 100U IC = 1
CO 3 0 IC = 5
.TRAN 2NS 200NS UIC
```

The initial inductor current is 1 A, while the initial voltage across the output capacitor CO is 5 V. PSpice does not calculate the transient analysis bias point before the beginning of the transient analysis if the UIC is inserted at the end of the TRAN statement, as done here. Figure 9.13 shows the output voltage, inductor current, and capacitor currents waveforms of the simulated buck converter using initial conditions. With the initial energy stored in the output capacitor, the average current–time product of the output capacitor over a switching cycle for the entire simulation is zero. The output voltage overshoots initially, but reaches its steady-state value in about 4 ms or four switching cycles. It should be noted that the time it takes for the converter to achieve a steady-state voltage of 5 V is less than the previous case without the use of initial conditions.

9.4 PSPICE SIMULATIONS USING SCHEMATICS ENTRY

The graphic input interface for the latest versions of PSpice (Capture in OrCad) permits rapid input, interpreting, documenting, and debugging of

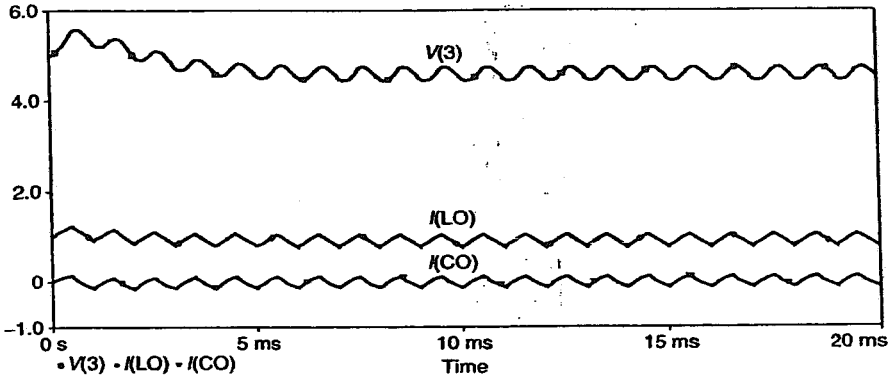


Figure 9.13 Output voltage ($V(3)$), inductor current ($I(LO)$), and capacitor current ($I(CO)$) of the simulated buck converter with an ideal switch using initial conditions.

PSpice input files. We encourage the use of the graphic input interface instead of the text input file. An example of schematic entry follows.

9.4.1 Boost Converter

The PSpice schematic of a boost converter with a voltage-controlled switch replacing the switching transistor is shown in Figure 9.14. The switching frequency is set to 1 kHz by PER = 1 ms, the duty cycle is 50%, since the PW is set to 0.5 ms.

Figure 9.15 shows the output voltage of the simulated boost converter. As can be seen, the response is underdamped and reaches its steady-state

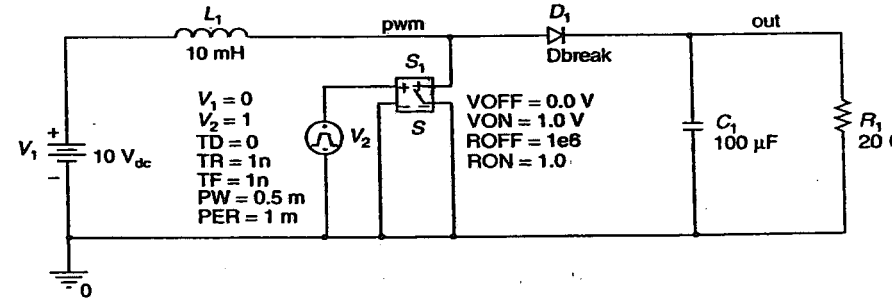


Figure 9.14 Circuit schematic of a boost converter with a voltage-controlled switch replacing the switching transistor.

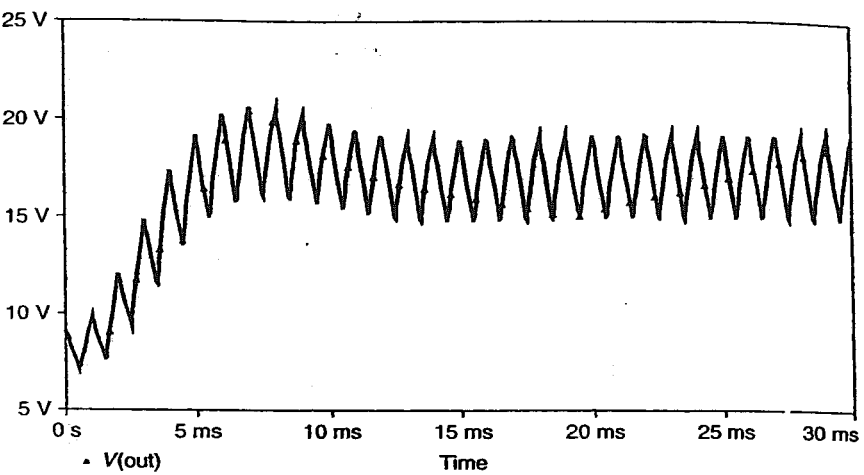


Figure 9.15 Output voltage waveform of the simulated boost converter.

voltage of 16 V in about 15 ms or 15 switching cycles. The simulated output ripple voltage is 4.7 V, in good agreement with the theoretical value:

$$\Delta v_c = \frac{I_a D}{C f_s} = \frac{0.5}{(100 \times 10^{-6})1000} = 5\,\text{V}. \tag{9.3}$$

Figure 9.16 shows the input inductor current and output capacitor current waveforms of the simulated boost converter. The input inductor current is underdamped with a ripple current of 0.5 A. The theoretical value is given by

$$\Delta I = \frac{V_s D}{L f_s} = \frac{10(0.5)}{(10 \times 10^{-3})1000} = 0.5\ \text{A}. \tag{9.4}$$

9.4.2 PSpice Simulations Using Behavioral Modeling

Analog behavioral modeling is a time-saving tool that can be used to design systems at an abstract level to test if the concepts are correct, before proceeding with the detailed circuit-level design. In PSpice, the ABM.OLB part library contains the ABM components. This library contains two sections. The first section includes parts that can be used to represent control-system-type of circuits. Some of these components are: SUM, GAIN, LAPLACE, and HIPASS. The second section contains controlled-source parts, like EVALUE and GFREQ that are based on extensions to traditional PSpice E and G device types. A detailed description of these components can be found in PSpice User's Guide [2].

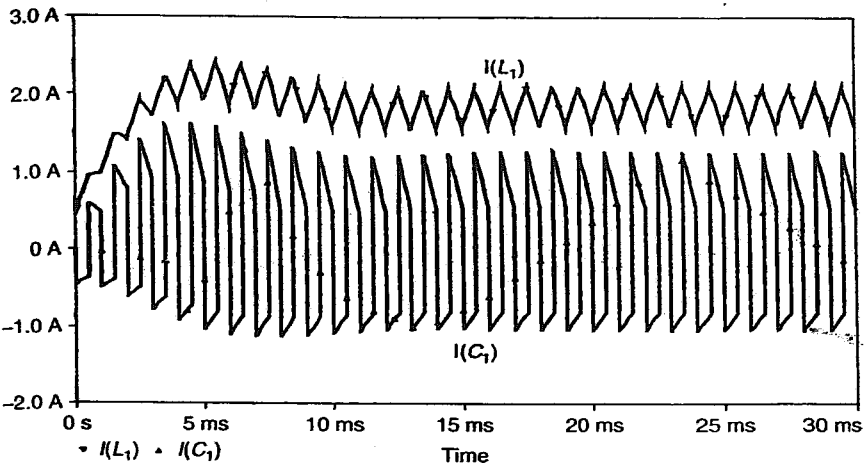


Figure 9.16 Input inductor current and output capacitor current waveforms of the simulated boost converter.

9.4.2.1 Control System Parts

Control system parts have one input and one output. The reference for the input and output voltages is the analog ground (node 0). These components can be connected together with no need for dummy loads or input resistors. Table 9.5 lists the control system parts, grouped by function. The fourth column displays the characteristic properties that differentiate each specific application.

9.4.2.2 PSpice-Equivalent Parts

PSpice-equivalent parts have a differential input and a double-ended output. They can be classified as either E or G device types. The E part type yields a voltage output, while the G device type yields a current output. Their transfer functions can contain any combination of voltages and currents as inputs. Hence, there is no division between voltage-controlled and current-controlled parts. Instead, the part type is defined merely by the output requirements. If a voltage output is required, use an E part type. If a current output is needed, use a G part type. Table 9.6 summarizes the PSpice-equivalent parts available in the ABM part library. Logical and arithmetic operators, as well as math functions, can be used in the expression field of all ABM parts. Table 9.7 and Table 9.8 summarize the operators and functions available in PSpice.

Table 9.5 Control System Parts [2]

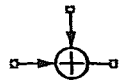
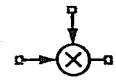
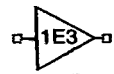
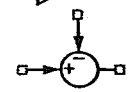
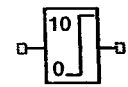
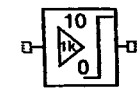
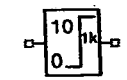
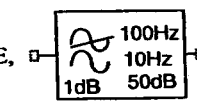
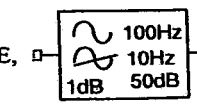
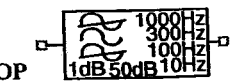
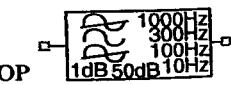
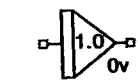
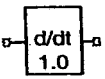
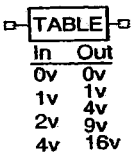
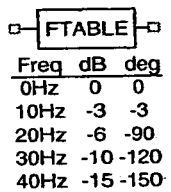
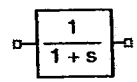
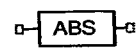
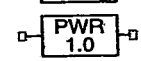
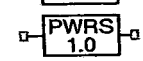
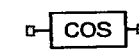
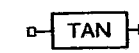
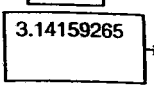
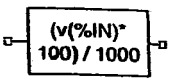
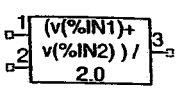
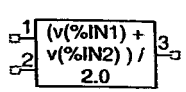
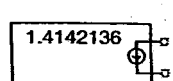
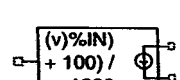
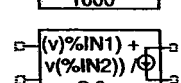
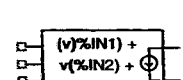
Category	Part	Description	Properties	Icon
Basic components	CONST	Constant	VALUE	
	SUM	Adder		
	MULT	Multiplier		
	GAIN	Gain block	GAIN	
	DIFF	Subtraction		
Limiters	LIMIT	Hard limiter	LO, HI	
	GLIMIT	Limiter with gain	LO, HI, GAIN	
	SOFTLIM	Soft (tanh) limiter	LO, HI, GAIN	
Chebyshev filters	LOPASS	Low pass filter	FP, FS, RIPPLE, STOP	
	HIPASS	High pass filter	FP, FS, RIPPLE, STOP	
	BANDPASS	Band pass filter	F0, F1, F2, F3, RIPPLE, STOP	
	BANDREJ	Band reject (notch) filter	F0, F1, F2, F3, RIPPLE, STOP	
Integrator and differentiator	INTEG	Integrator	GAIN, IC	

Table 9.5 Control System Parts—*Continued*

Category	Part	Description	Properties	Icon
	DIFFER	Differentiator	GAIN	
Table look-ups	TABLE	Lookup table	ROW1 ... ROW5	
	FTABLE	frequency lookup table	ROW1 ... ROW5	
Laplace transform	LAPLACE	Laplace expression	NUM, DENOM	
Math functions 'x' is the input	ABS	$\|x\|$		
	SQRT	$x^{1/2}$		
	PWR	$\|x\|^{EXP}$	EXP	
	PWRS	x^{EXP}	EXP	
	LOG	$\ln(x)$		
	LOG10	$\log(x)$		
	EXP	e^x		
	SIN	$\sin(x)$		
	COS	$\cos(x)$		
	TAN	$\tan(x)$		
	ATAN	$\text{Tan}^{-1}(x)$		

(*Continues*)

Table 9.5 Control System Parts—*Continued*

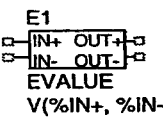
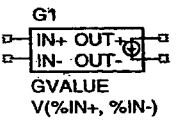
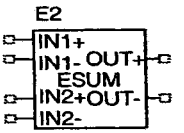
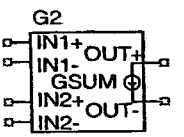
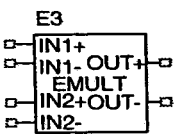
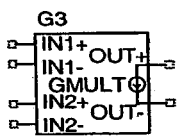
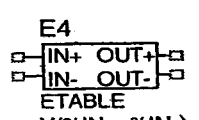
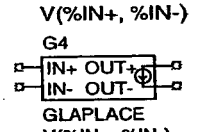
Category	Part	Description	Properties	Icon
	ARCTAN	$\text{Tan}^{-1}(x)$		
Expression functions	ABM	No inputs, V out	EXP1 ··· EXP4	
	ABM1	1 Input, V out	EXP1 ··· EXP4	
	ABM2	2 Inputs, V out	EXP1 ··· EXP4	
	ABM3	3 Inputs, V out	EXP1 ··· EXP4	
	ABM/I	No input, I out	EXP1 ··· EXP4	
	ABM1/I	1 Input, I out	EXP1 ··· EXP4	
	ABM2/I 2	Inputs, I out	EXP1 ··· EXP4	
	ABM3/I	3 Inputs, I out	EXP1 ··· EXP4	

9.4.3 Examples of ABM Blocks Use

We included a selection of simple examples that the reader may find handy when designing switching converter simulations, such as parameter definition, triangular waveform generator, PWM modulator, and a VCO for the control of resonant converters.

PARAM is a component in the Special library, which can be used to define global parameters that can be accessed from ABM blocks. In Figure 9.17, two parameters are defined: PI and FREQ. Both parameters are used in the ABM block to implement a sine wave generator of frequency FREQ. TIME is an internal global parameter that keeps track of the simulation time.

Table 9.6 PSpice-Equivalent Parts

Category	Part	Description	Properties	Icon
Mathematical expression	EVALUE	General purpose	EXPR	
	GVALUE			
	ESUM	Special purpose	(None)	
	GSUM			
	EMULT			
	GMULT			
Table look-up	ETABLE	General purpose	EXPR	
	GTABLE		TABLE	

(*Continues*)

Table 9.6 PSpice-Equivalent Parts—*Continued*

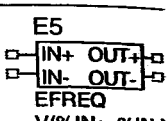
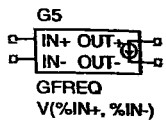
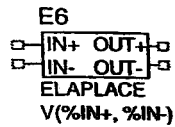
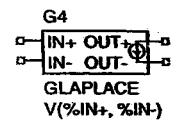
Category	Part	Description	Properties	Icon
Frequency table look-up	EFREQ	General purpose	EXPR	
	GFREQ		TABLE	
Laplace transform	ELAPLACE	General purpose	EXPR	
	GLAPLACE		XFORM	

Table 9.7 Operators in ABM Expressions

Operator class	Operators	Description
Arithmetic	+	Addition or string concatenation
	−	Subtraction
	*	Multiplication
	/	Division
	**	Exponentiation
Logical[a]	~	Unary NOT
	|	Boolean OR
	^	Boolean XOR
	&	Boolean AND
Relational[a]	=	Equality test
	≠	Nonequality test
	>	Greater than test
	≥	Greater than or equal to test
	<	Less than test
	≤	Less than or equal to test

[a]Logical and relational operators are used within the IF( ) function.

Table 9.8 Functions in Arithmetic Expressions

Function	Description
ABS(x)	$\|x\|$
SQRT(x)	$x^{1/2}$
EXP(x)	e^x
LOG(x)	ln(x) which is log base e
$LOG_{10}(x)$	Log(x) which is log base 10
PWR(x,y)	$\|x\|^y$
PWRS(x,y)	$+\|x\|^y$ (if $x > 0$); $-\|x\|^y$ (if $x < 0$)
SIN(x)	sin(x), where x is in radians
ASIN(x)	$\sin^{-1}(x)$, where the result is in radians
SINH(x)	sinh(x), where x is in radians
COS(x)	cos(x), where x is in radians
ACOS(x)	$\cos^{-1}(x)$, where the result is in radians
COSH(x)	cosh(x), where x is in radians
TAN(x)	tan(x), where x is in radians
ATAN(x) = ARCTAN(x)	$\tan^{-1}(x)$, where the result is in radians
ATAN2(y,x)	$\tan^{-1}(y/x)$, where the result is in radians
TANH(x)	tanh(x), where x is in radians
M(x)	Magnitude of x^a which is the same as ABS(x)
P(x)	Phase of x^a in degrees; returns 0.0 for real numbers
R(x)	Real part of x^a
IMG(x)	Imaginary part of x^a which is applicable to AC analysis only
DDT(x)	Time derivative of x which is applicable to transient analysis only
SDT(x)	Time integral of x which is applicable to transient analysis only
TABLE(x, x_1, y_1, ...)	y Value as a function of where x_n, y_n point pairs are plotted and connected by straight lines
MIN(x,y)	Minimum of x and y
MAX(x,y)	Maximum of x and y
LIMIT(x,min,max)	min if $x <$ min; max if $x >$ max else x
SGN(x)	+1 if $x > 0$; 0 if $x = 0$; −1 if $x < 0$
STP(x)	1 if $x > 0$; 0 otherwise which is used to suppress a value until a given amount of time has passed
IF(t,x,y)	x if t is true y otherwise where t is a relational expression using the relational operators shown in Table 9

[a]M(x), P(x), R(x), and IMG(x) apply to Laplace expressions only.

The node voltages can be accessed from any ABM block; this is the case of the output voltage of the previous example, which is multiplied by 3 to produce the control output, as shown in Figure 9.18. An ABM1 block has one input,

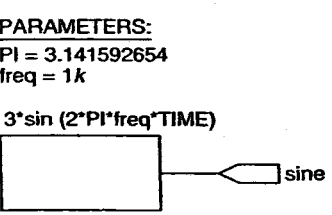


Figure 9.17 ABM and PARAM.

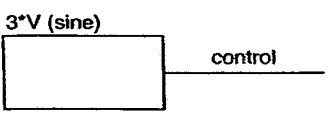


Figure 9.18 Node voltages can be accessed from ABM blocks.

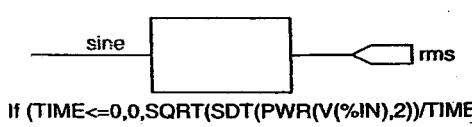


Figure 9.19 RMS meter.

V(%IN), and one output. A true rms meter can be implemented using the PARAM, as shown in Figure 9.19. The input voltage is squared, then integrated and divided by the elapsed time, and finally the square root is calculated. The IF statement is used to avoid the division by zero at TIME = 0.

The syntax for an IF THEN statement is as follows:

```
IF(ARGUMENT,THEN,ELSE)
```

The ARGUMENT, THEN, and ELSE statements can contain references to node voltages, currents through voltage sources, arithmetic symbols, logical symbols, and relational symbols. For example,

```
IF (TIME≤0, 0, SQRT(SDT(PWR(V(%IN),2))/TIME))
```

At TIME = 0 the output is set to 0; otherwise the rms expression is evaluated.

Another example of the use of the IF statement is

```
IF (V(IN)>3,12,V(IN)*4)
```

This statement evaluates if the input voltage is greater than 3 V; in that case, the output signal saturates to 12 V. Otherwise, the input signal is amplified by 4. This can be used to simulate a linear amplifier with a 12-V power supply.

A PWM modulator can be easily implemented with ABM blocks, as shown in Figure 9.20. V_4 is a VPULSE source whose parameters are set to simulate a triangular waveform generator. An ABM2 block is used in this case. It has two inputs, V(%IN1) and V(%IN2). The IF statement programmed into this block is an ideal comparator; if the control signal is greater than the triangular signal, then the PWM output is 1; otherwise is 0.

A common error message obtained while using ABMx parts is "part not annotated." Somehow, CAPTURE does not automatically assign a part reference to these components and the error message is generated. Remember to manually assign a part reference; e.g., ABM2a.

An implementation of a VCO is illustrated in Figure 9.21, where a sine wave generator is modeled with an ABM1 block. The frequency is proportional to the input voltage; thus, changing V(%IN) changes the VCO output frequency.

9.4.4 PSpice Simulations Using Control Blocks

A model of a PWM modulator using control blocks is shown in Figure 9.22. A DIFF part is used to subtract the control and the triangular signals. The result of this operation is passed through a high-gain GLIMIT that acts as a comparator. The PWM output is either at 0 or 10 V.

Figure 9.23 represents a simplified model for an operational amplifier. The finite input impedance is modeled by R_1 and R_2. The DIFF component subtracts the signal at the inverting input pin, In–, from the signal at the noninverting input pin, In+. The large open-loop gain of the operational

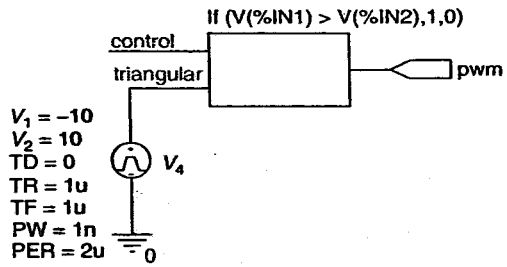


Figure 9.20 PWM modulator.

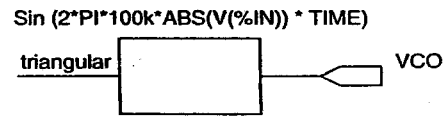


Figure 9.21 VCO implementation with ABM1.

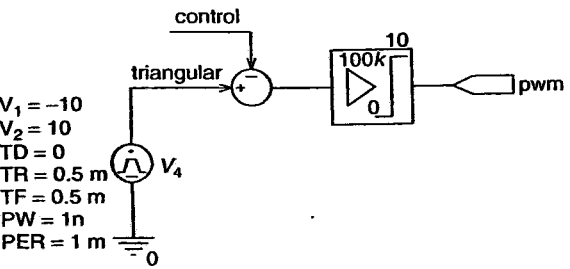


Figure 9.22 PWM modulator with control blocks.

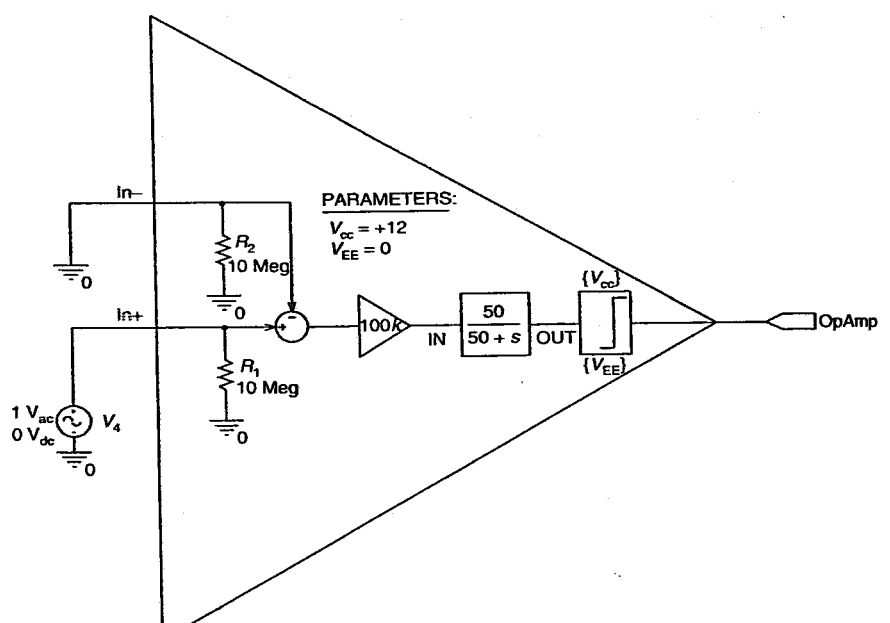


Figure 9.23 Model of an operational amplifier.

amplifier (i.e., 100 k) is represented by a GAIN block. The Laplace block models the open-loop frequency response, including only the low frequency pole. The LIMIT block limits the output voltage swing to the values set by the PARAMETERS V_{cc} and V_{EE}, emulating the saturation of the amplifier due to the output voltage swing reaching the power supply limits. The open-loop frequency response for the operational amplifier is shown in Figure 9.24.

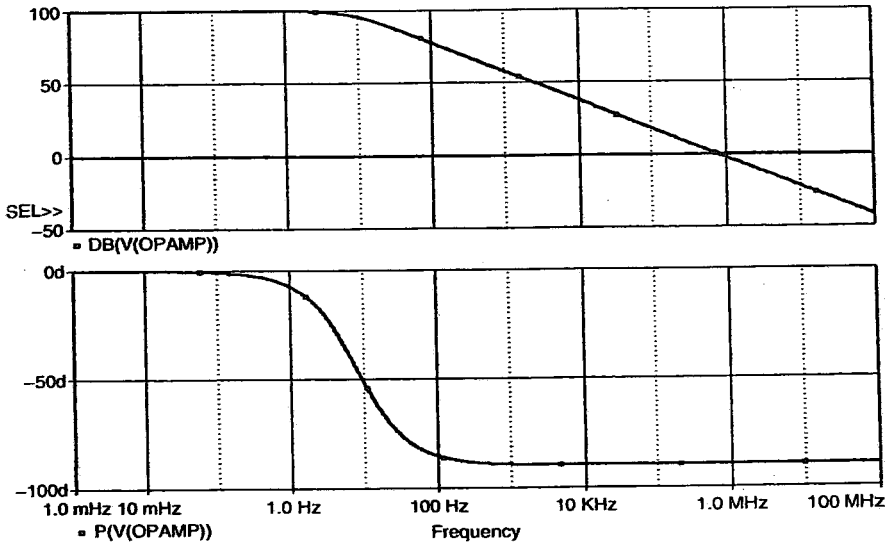


Figure 9.24 Open-loop frequency response.

A closed-loop amplifier with a gain of 11 V/V implemented with the above operational amplifier is shown in Figure 9.25 with its frequency response shown in Figure 9.26. Notice how the gain decreases while the bandwidth increases in the same proportion (i.e., $(1 + \beta A)$), according to feedback theory [3].

9.4.4.1 Voltage-Mode PWM Boost Converter

The same boost converter of Figure 9.14 is simulated in Figure 9.27 with a closed-loop control to obtain a regulated output voltage of 20 V and a critically damped transient response. Recall from Figure 9.15 that the output voltage of the open-loop converter settles to 17 V at 15 ms, after overshooting up to 22 V. The components of the feedback loop are modeled with ABM parts to speed up the design process. The voltage-controlled voltage-source *E*1 is used to sample the output voltage. The sensed voltage, *V*(sense) = *V*(out)*0.25; where 0.25 is the voltage gain of *E*1. This part can be physically replaced by a resistive voltage divider using the same ratio. The dashed box delimits the model for the error amplifier. The subtraction is followed by the gain block, representing the closed-loop gain of the error amplifier. The Laplace part models the closed-loop frequency response and the limiter represents the saturation of the supply voltage. The inputs to the error

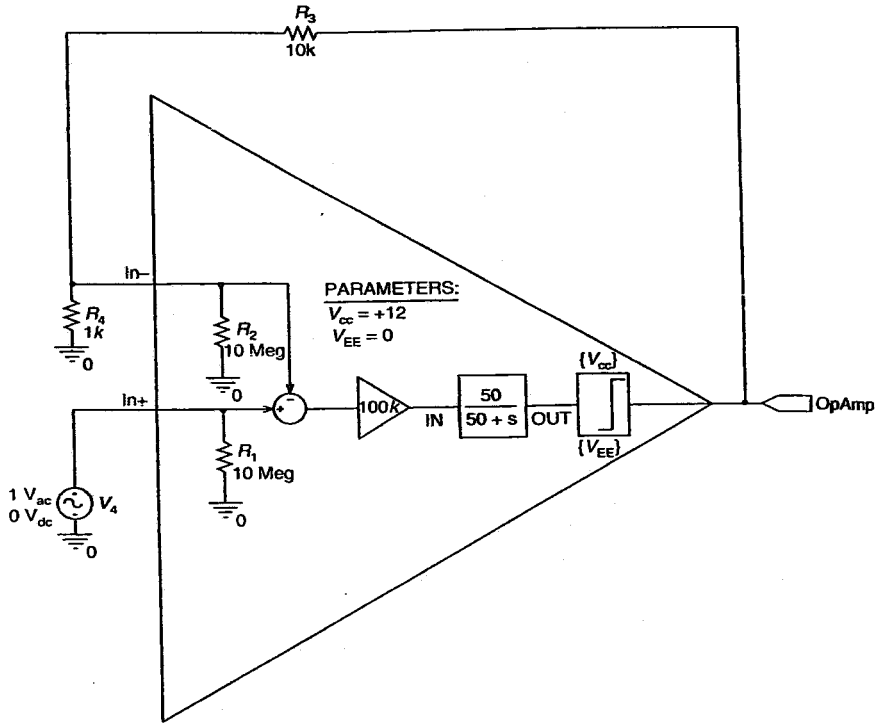


Figure 9.25 Closed-loop amplifier.

amplifier are the reference and the sensed voltages. As such, the error signal is then proportional to the difference of these two voltages. The PWM modulator is implemented using an ABM2 part, as discussed above. The inputs to the modulator are the control and the sawtooth signals. The sawtooth is generated using VPULSE, V4. The control signal is the result of adding the error voltage to the reference voltage. The use of the adder at that point is very convenient, since it enables the closed-loop response to be evaluated without modifying the circuit. The open-loop response can be evaluated by disconnecting the output of the error amplifier from the adder and grounding the unconnected adder input. In this case, the reference voltage can still be connected to the modulator with the switching converter in an open-loop configuration. It should be noted that the error signal still reflects the difference between the open-loop output voltage and the reference voltage.

Figure 9.28 shows the control, error, and output voltages for the closed-loop boost converter, together with their respective average values.

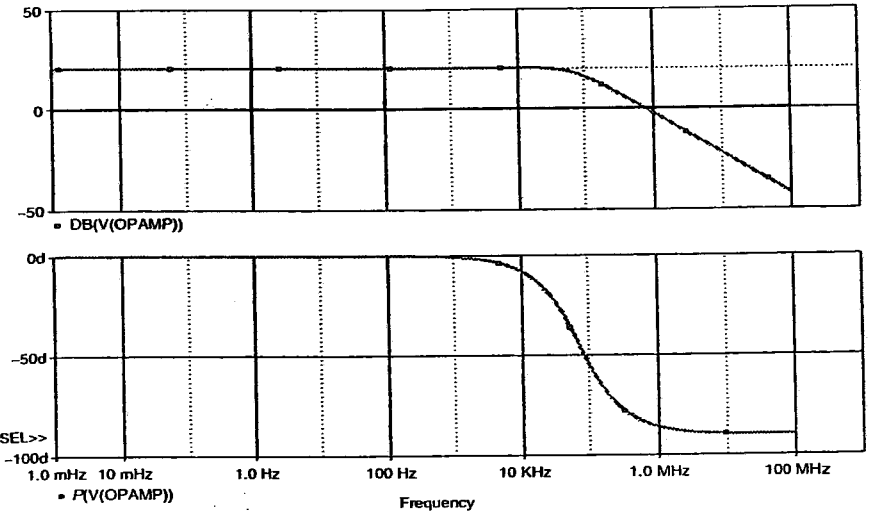


Figure 9.26 Closed-loop frequency response.

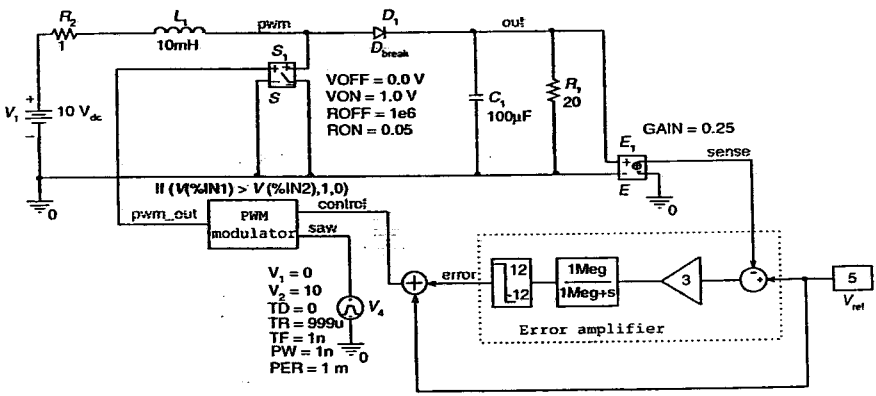


Figure 9.27 Closed-loop boost converter.

The error amplifier gain has been adjusted to give a critically damped transient response. Notice how the output voltage settles to its final value of 20 V in less than 4 ms and without overshooting. At the same time, the error approaches zero and the control voltage approaches 5 V (i.e.; 20 V/gain(E_1)).

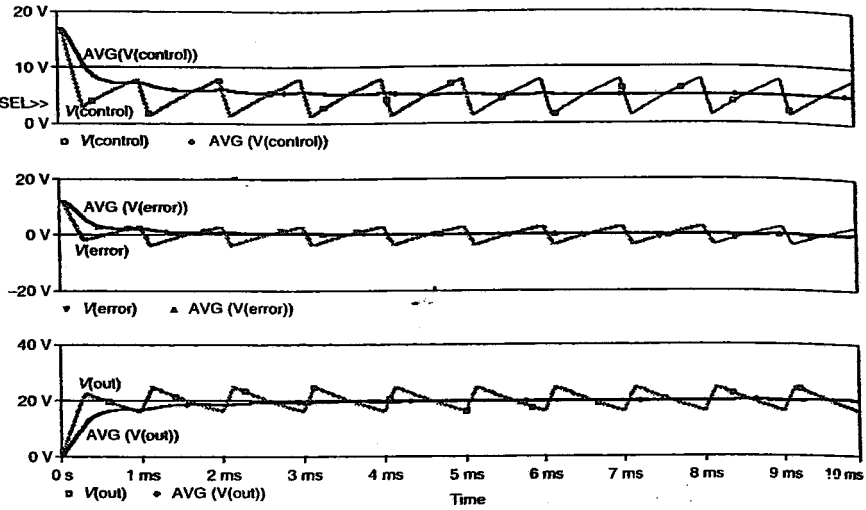


Figure 9.28 Voltage waveforms of the closed-loop boost converter.

9.4.5 PSpice Simulations Using Vendor Models

The last step before building a prototype is to simulate the circuit using the vendor models for the circuit components. In this simulation, it is recommended to include realistic circuit and element parasitics. .MODEL statements should not be used to model the effect of package parasitics. This is because these .MODEL statements cannot be used to model the transient response of most power semiconductor devices due to the extreme nonlinear characteristics of these power devices. Therefore, MODEL statement is seldom used in the transient analysis of switching devices. Instead, a SUBCIRCUIT representation for power MOSFET should be used in transient analysis.

Example 9.1. Continuing with the design of the boost converter of Figure 9.27, the ABM parts were replaced by vendor models. The inductor and capacitor parasitics are included, resulting in the circuit shown in Figure 9.29. The initial current flowing through the inductor L_1 is set to zero; otherwise, the simulation may yield an erroneous answer. The simulation options listed below can be used to improve convergence.

```
.TRAN 0 30m 0 0.1u
.OPTIONS STEPGMIN
.OPTIONS ABSTOL = 10p
```

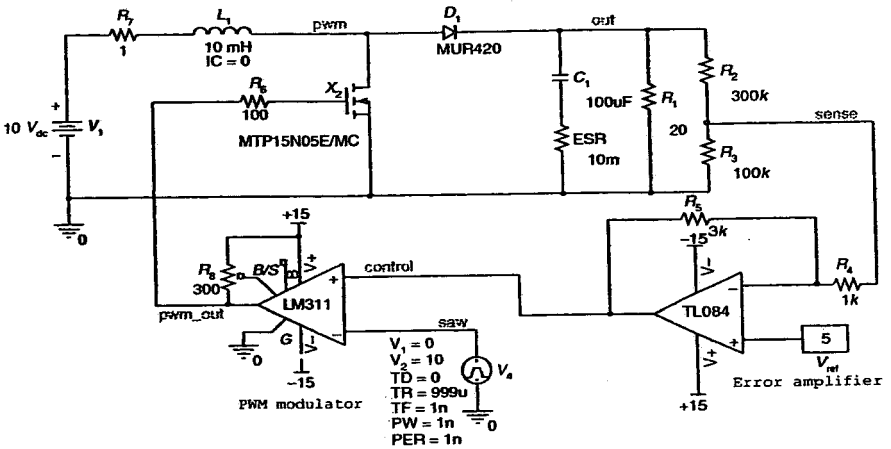


Figure 9.29 Closed-loop boost converter with vendor models.

```
.OPTIONS ITL1 = 400
.OPTIONS ITL4 = 500
.OPTIONS RELTOL = 0.01
.OPTIONS VNTOL = 10u
```

Figure 9.30 shows the inductor current, control voltage, and output voltage waveforms of the simulated converter. $I(L_1)$ starts from 0 due to the initial current of IC = 0. The control voltage settles to an average value slightly larger than 5 V to offset the losses due to nonideal circuit components. It is important to avoid saturation of the control signal in order to be able to control the converter at all time. The steady-state average output voltage of the boost converter is smaller than 20 V. A PI controller should be used to achieve a zero steady-state error of its output voltage. Nevertheless, V(out) settles to its final value with almost no overshoot. This simulation requires twice the simulation time compared to the simulation using ABM parts; also, the output data files are much larger.

9.5 SMALL-SIGNAL ANALYSIS OF SWITCHING CONVERTERS

As discussed in Chapter 6, many linear small-signal models for switching converters have been developed. Orcad PSpice includes a library with linear components based on the Vorpérian model [4]. The components of this library, named SWIT_RAV.LIB, are listed in Table 9.9.

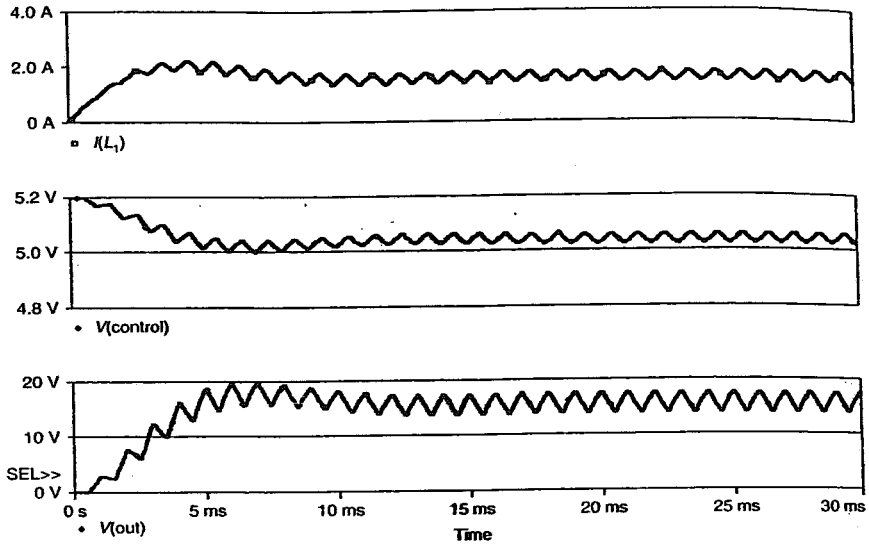


Figure 9.30 Waveforms of the simulated closed-loop converter.

Table 9.9 Vorperian models for PSpice [2]

SWIT_RAV.LIB components

Component	Description	Parameters
CMLSCCM	Current-mode large-signal continuous-conduction mode	Se: External ramp slope (*v/s*) FS: Operating frequency Lfil: Filter inductance Ri: Current feedback coefficient
CMSSCCM	Current-mode small-signal continuous conduction mode	Se: External ramp slope (*v/s*) Sn: Current semse ramp slope (*v/s*) FS: Operating frequency D: Duty cycle Lfil: Filter inductance Ic: Current from terminal C Vap: Voltage across terminals a and p Ri: Current feedback coefficient
QRLSZCS	Quasi-resonant large-signal zero-current-switching	VCOCOEFF: Coefficient for voltage to frequency conversion Fsoffset: Frequency from Vco at zero Vc

Table 9.9 Vorperian models for PSpice [2]—*Continued*

SWIT_RAV.LIB components

Component	Description	Parameters
		Lo: Resonant filter value Co: Resonant capacitor value N: full wave $N = 2$; half wave $N = 1$
VMCCMDCM	Voltage-mode continuous-conduction-mode and discontinuous-conduction-mode	RMPHITE: External ramp height VALLEYV: Valley voltage of external ramp LFIL: Filter inductance FS: Operating frequency START: Setup time necessary for the model to set itself up
VMLSCCM	Voltage-mode large-signal continuous-conduction-mode	RMPHITE: External ramp height VALLEYV: Valley voltage of external ramp
VMLSDCM	Voltage-mode large-signal discontinuous-conduction-mode	RMPHITE: External ramp height VALLEYV: Valley voltage of external ramp LFIL: Filter inductance FS: Operating frequency
VMSSCCM	Voltage-mode large-signal continuous-conduction-mode	RMPHITE: External ramp height D: Duty cycle Ic: Current flowing from terminal C Vap: Voltage across terminals a and b Rsw: Switch on resistance Rd: Diode on resistance Rm: Models the base storage effects Re: Capacitor ESR

The PSpice model for the voltage-mode small-signal continuous-conduction-mode (VMSSCCM) part is listed below. The parameters match with those in the model published by Vorpérian [4]; a description is also found in Chapter 6. These parameters have to be specifically set for each circuit. Note that the default ramp height is 2 V.

```
**** VMSSCCM ****
*
* Small signal continuous conduction voltage mode model
* Params: RMPHITE → External ramp height
* D → Duty cycle
* Ic → Current flowing from terminal C
*       See diagrams: but for buck it is Vo/r, for boost it is Iin
* Vap → Voltage across terminal A P
*         See diagrams: but for buck it is Vin
* Rsw → Switch on resistance
* Rd → diode on resistance
* Rm → which models the base storage effects
* Re → models ripple across ESR of cap
*
* Pins control voltage ———
* common ——|
* passive—— | |
* ACTIVE – | | |
*          | | | |
. subckt VMSSCCM A P C VC Params:
  RMPHITE = 2 D = 0.4 IC = 1 VAP = 20
+ Rsw = 1E-6 Rd = 1E-6 Re = 1E-6 Rm = 1E-6
efm 4 0 value = {v(Vc)/rmphite}
e2 A 6 value = {v(0,4)*Vap/d}
g1 A P value = {v(4)*IC}
gxfr 6 P VALUE = {I(vms)*D}
exfr 9 P VALUE = {V(6,P)*D}
vms 9 8 0
rd 8 C {d*rd+(1-d)*rsw+d*(1-d)*re+rm}
rope 4 0 1g
rgnd 0 P 1g
.ends
```

A small-signal model for the boost converter of Figure 9.14, including circuit losses is shown in Figure 9.31. A small-signal AC analysis will be performed to study the frequency dependence of the averaged parameters with respect to small-signal changes in the duty cycle, $\hat{d}$. In this figure, notice how the voltage-mode small-signal continuous-conduction-mode (VMSSCCM) component is connected. The common terminal (C) is connected to the common point where the switch and the diode are connected; the active terminal (A) is connected to the other end of the switch; the passive terminal (P) is connected to the other terminal of the diode; and the

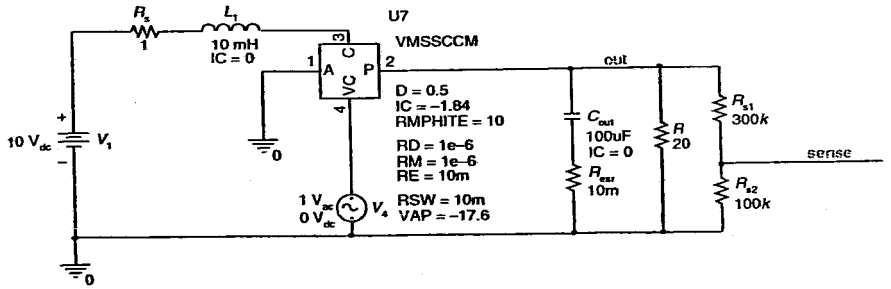


Figure 9.31 Small-signal AC analysis.

control terminal (VC) is connected to the duty cycle generator. The parameters of the VMSSCCM part are found from the average values of the parameters in Figure 9.14 as follows:

$D = 0.5$ is the average duty cycle

IC $= -1.84$ A is the average current flowing out of the common terminal, in this circuit is equal to $-I_{L_1}$

RD = 1e–6 is the dynamic resistance of the diode

RE = 10 m is the capacitor's ESR

RM = 1e–6 models the base storage effects

RMPHITE = 10 sets a ramp of 10 V, this parameter is used for the small-signal gain

RSW = 10 m is the switch on resistance

$V_{ap} = -17.6$ V is the average voltage between terminals (A) and (P); for this circuit is equal to $-V_{out}$.

The average current flowing through the inductor, I_{L_1}, and the average output voltage, V_{out}, are plotted in Figure 9.32. These waveforms follow the average trend of the waveform shown in Figure 9.15, without the switching ripple. It should be noted that this model accurately predicts the DC component, as well as the small-signal AC components up to half the switching frequency.

9.5.1 Open-Loop Transfer Function

Figure 9.33 shows the bode plot of the output-to-control transfer function for the boost switching converter. It represents the frequency dependence of the output voltage to small-signal variations in the duty cycle. It can be observed that these Bode plots correspond to an underdamped second-order system with a right-half-plane (RHP) zero. According to the equations listed in Table 6.3, the complex-conjugate poles due to the output filter are located at $f_0 = (1 - D)/2\pi\sqrt{LC_{out}} = 25$ Hz; the left-half-plane

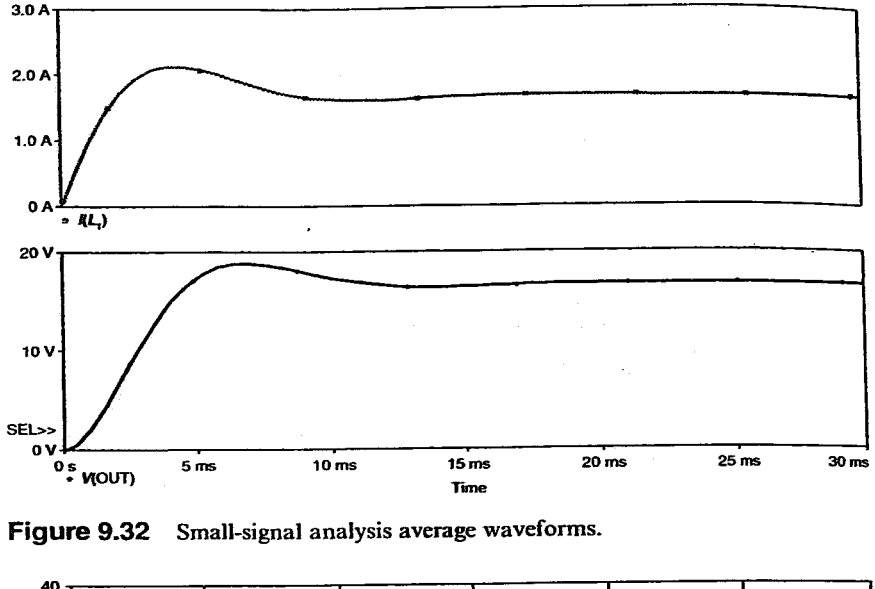


Figure 9.32 Small-signal analysis average waveforms.

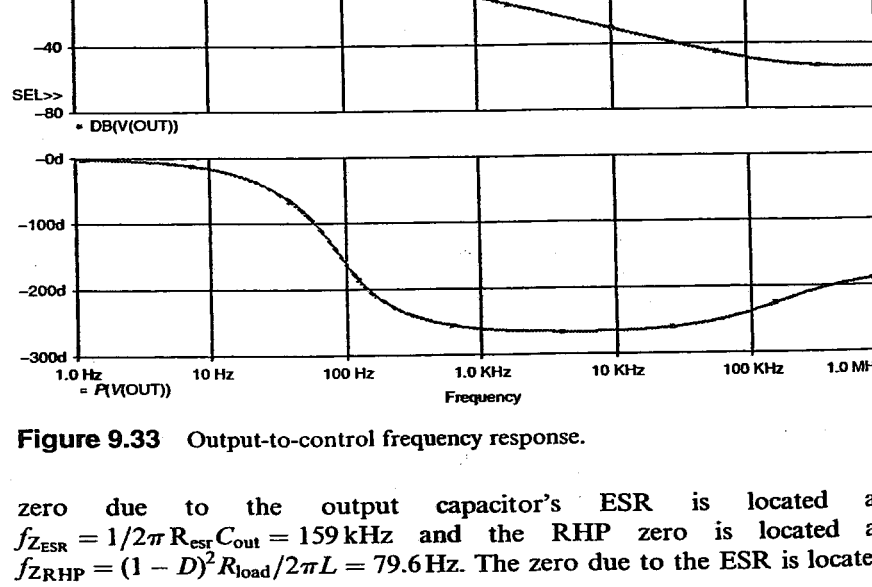


Figure 9.33 Output-to-control frequency response.

zero due to the output capacitor's ESR is located at $f_{Z_{ESR}} = 1/2\pi\, R_{esr} C_{out} = 159\,\text{kHz}$ and the RHP zero is located at $f_{ZRHP} = (1-D)^2 R_{load}/2\pi L = 79.6\,\text{Hz}$. The zero due to the ESR is located

at a very high frequency (more than 10 times the switching frequency), thus it produces no influence on the frequency response for frequencies below $f_s/2$. The RHP zero is located at low frequency, close to the corner frequency of the output filter. Due to the combined effect of the two poles and the RHP zero, the magnitude rolls down with a −20 dB/dec slope and the phase reaches −270° above 1 kHz.

9.5.2 Input Impedance

The input impedance can be evaluated by connecting a small-signal AC source in series with the DC voltage source as shown in Figure 9.34. After an AC analysis is performed, the input impedance can be plotted as the ratio of the voltage of the AC source to its current, as shown in Figure 9.35.

9.5.3 Output Impedance

To plot the output impedance, an AC source is connected in parallel with the output terminals, as shown in Figure 9.36. After performing an AC analysis, the output impedance can be plotted as the ratio of the voltage of the AC source to its current, as shown in Figure 9.37. As can be seen, the output impedance peaks at the frequency of 100 Hz.

9.5.4 Small-Signal Transient Analysis

The average models can also be used to simulate small-signal transient analysis. This is useful to predict the behavior of the switching converter due to changes in the circuit parameters, such as duty cycle, input voltage, load current, etc. Figure 9.38 shows the schematic diagram to simulate a step change in the duty cycle at 20 ms. The amplitude of the duty cycle step is 1 V. Figure 9.39 shows the input inductor current and output voltage waveforms before and after the step change in duty cycle. These waveforms show the average

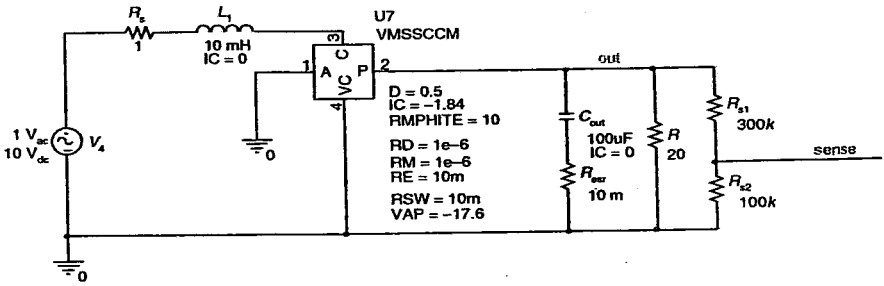


Figure 9.34 Simulation setup to plot the input impedance.

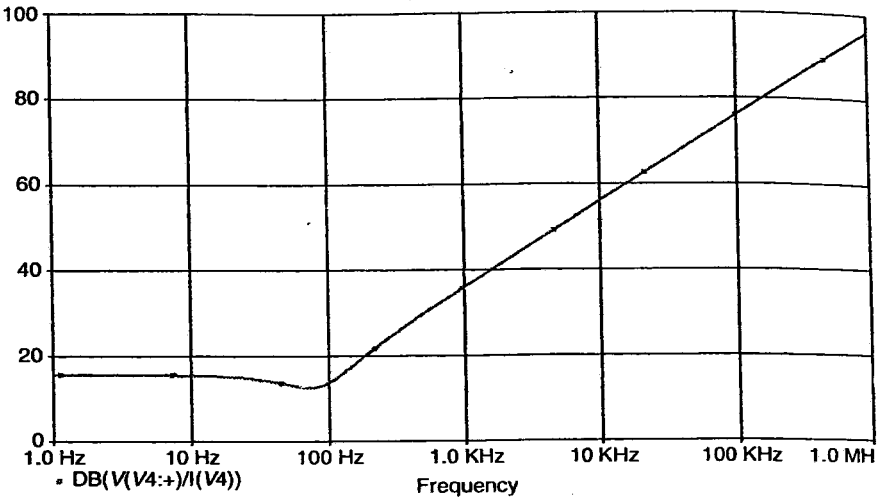


Figure 9.35 Input impedance.

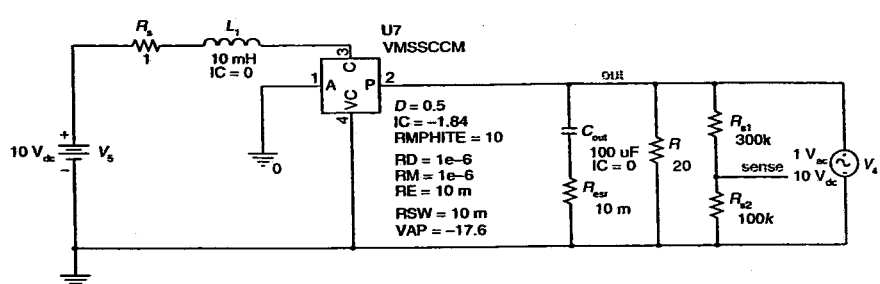


Figure 9.36 Simulation setup to plot the output impedance.

dynamic response of the switching converter to a step change in the duty cycle. The current waveform instantaneously increases, following the increase in the duty cycle. On the other hand, the voltage waveform shows the typical characteristic of a nonminimum-phase system, since the output voltage initially decreases prior to the increase corresponding to a larger duty cycle.

Other average models are available for free download from Basso's book [5] at its web page http://perso.wanadoo.fr/cbasso/Spice.htm. One of the models offered in the SMPSRECIPES.LIB is the average model developed by Ridley [6], which models both the voltage and current mode control schemes. Since this model includes the inductor, several components are provided to model the different switching converter topologies. That is the

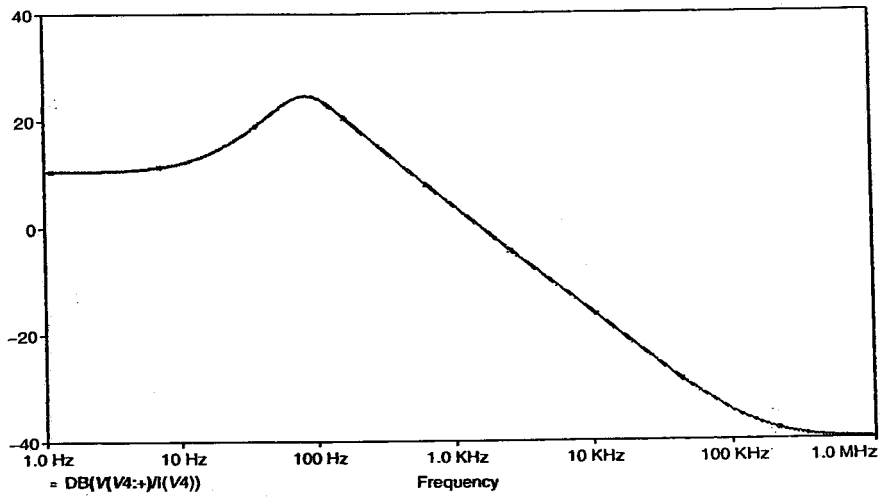


Figure 9.37 Output impedance.

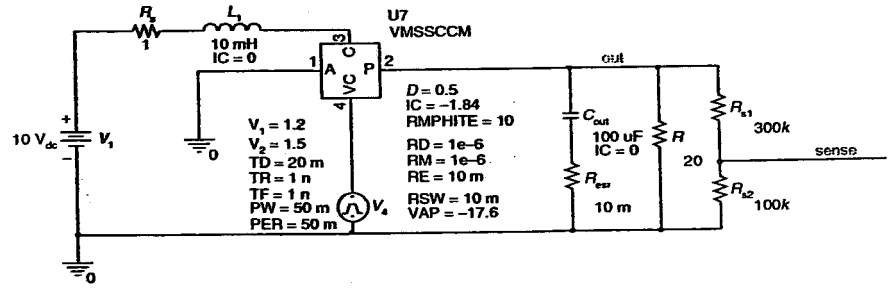


Figure 9.38 Simulation setup for the small-signal transient analysis.

case for all the average components based on the averaged-inductor model, such as the BOOSTVM component developed by Yaakov [7], as shown in Figure 9.40. As can be seen, one of the parameters for the component is the inductance, L. The average output voltage waveform obtained using this model is shown in Figure 9.41.

9.5.5 Measuring the Loop Gain

The circuit shown in Figure 9.42 is a method for measuring the loop gain. The diode is not necessary because no switching action takes place in the averaged model. However, it may be included, if desired, to add its dynamics

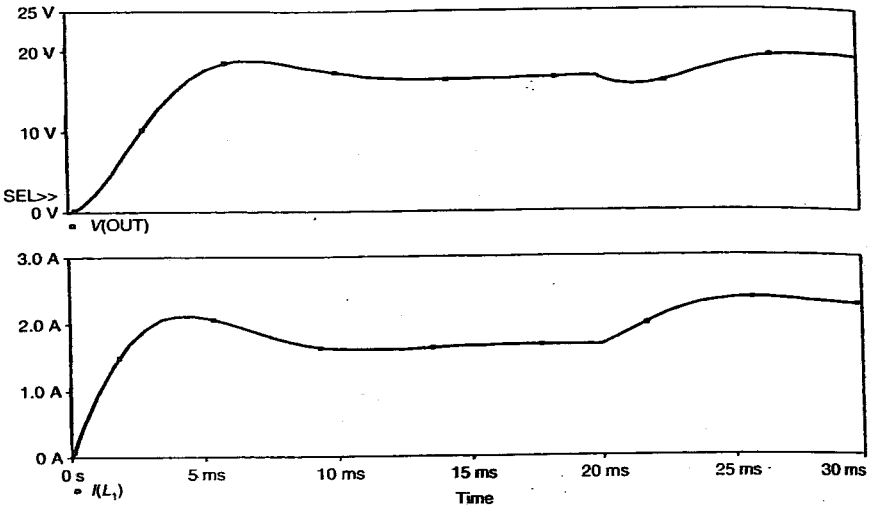


Figure 9.39 Small-signal transient analysis.

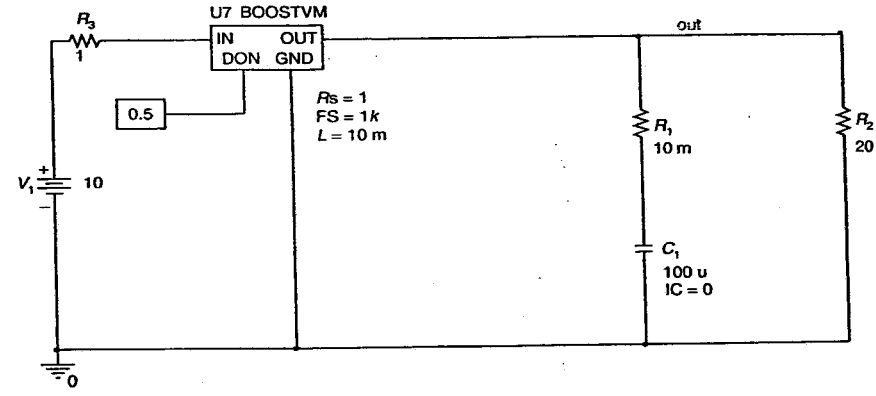


Figure 9.40 Averaged-inductor model for a voltage-mode boost converter.

such as diode voltage drop, capacitance, and dynamic resistance to the simulations. To measure the loop gain (i.e. βA)), we can measure the gain along the path through V_1 to V_f.

9.5.6 Frequency Compensation

For this circuit, we choose $f_1 = 100$ Hz for a switching frequency of 1 kHz. The Bode plot of the loop gain reveals that phase compensation is necessary

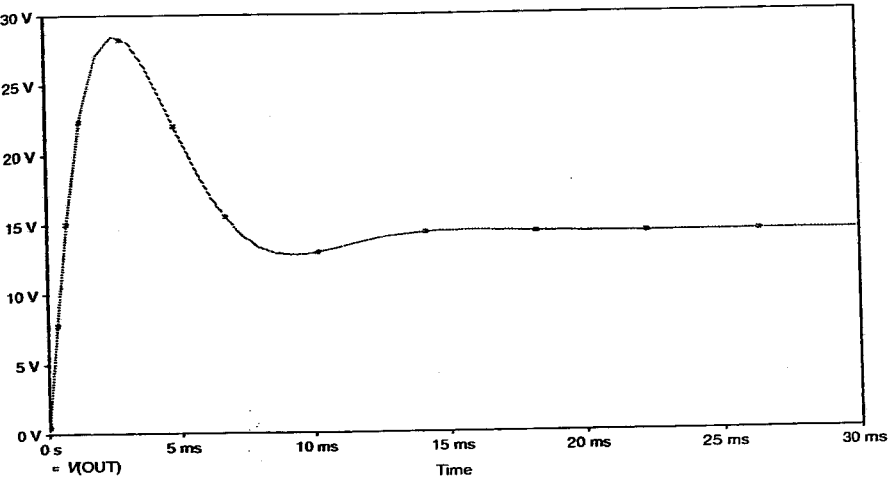


Figure 9.41 Output voltage obtained with the averaged-inductor model.

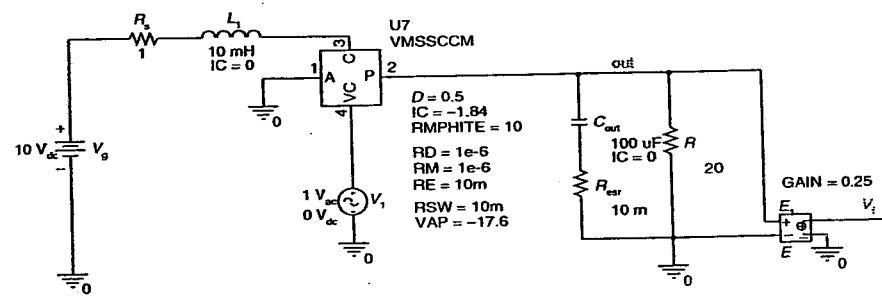


Figure 9.42 Circuit setup to measure the loop gain.

(Figure 9.43). Since the zero due to the ESR of the output capacitor is located at a relatively high frequency beyond f_1 (100 kHz), a 2-zero 3-pole (PID) compensation network is chosen to achieve the desired phase margin.

9.5.6.1 PID Compensation

The phase of the compensation network (2-zero and 3-pole) at f_1 is given by

$$\theta_{comp}(f_1) = -90 + 2\tan^{-1}\left(\frac{f_1}{f_z}\right) - 2\tan^{-1}\left(\frac{f_1}{f_p}\right) \tag{9.5}$$

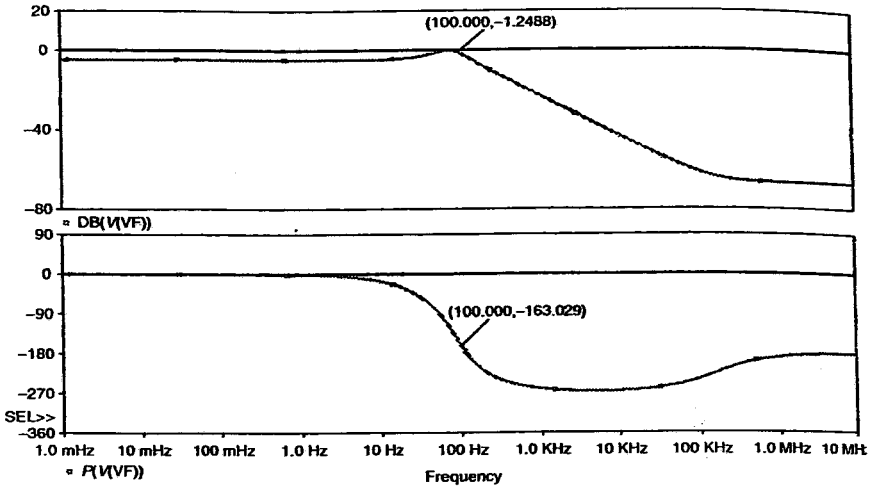


Figure 9.43 Bode plot of the loop gain.

and the magnitude is

$$M_{\text{comp}}(f_1) = -20\log_{10}(2\pi f_1) + 40\log_{10}\left(\sqrt{1+\left(\frac{f_1}{f_z}\right)^2}\right) - 40\log_{10}\left(\sqrt{1+\left(\frac{f_1}{f_p}\right)^2}\right). \tag{9.6}$$

From Equation (9.5),

$$f_{1z} = \frac{f_1}{f_z} = \tan\left(\frac{\theta_{\text{comp}} + 90 + 2\tan^{-1}(f_1/f_p)}{2}\right). \tag{9.7}$$

Substituting Equation (9.7) into Equation (9.6),

$$M_{\text{comp}}(f_1) = -20\log_{10}(2\pi f_1) + 40\log_{10}\left(\sqrt{1+f_{1z}^2}\right) - 40\log_{10}\left(\sqrt{1+\left(\frac{f_1}{f_p}\right)^2}\right). \tag{9.8}$$

Once the location of the double poles and double zeros have been chosen, we can calculate the value of the components of the compensation network:

$$f_{p1} = \frac{1}{2\pi R_3 C_3}, f_{p2} = \frac{(C_1 + C_2)}{2\pi R_2 C_1 C_2}, f_{z1} = \frac{1}{2\pi R_2 C_1},$$

$$f_{z2} = \frac{1}{2\pi(R_1 + R_3)C_3}, K_1 = \frac{R_2}{R_1}, K_2 = \frac{R_2(R_1 + R_3)}{R_1 R_3},$$

$$\frac{R_3}{R_2} C_3 = \frac{C_1 C_2}{C_1 + C_2}. \tag{9.9}$$

The following MATLAB program solves Equation (9.8) and calculates the network components according to Equation (9.9).

```
% iteratively solve for pole location on a
% 3-pole 2-zeros compensation network
clear all
PhaseBoost = 32; % needed phase boost at f1 (comp
  network phase at f1)
GainBoost = -7; % needed gain boost at f1 in dB
f1 = 100; % defined by designer, has to be <(fs/2) in Hz
d2r = pi/180; % degree to radian conversion
fpd = 7.5*f1; % initial guess
m = 1; % keeps the while going
while(m),
f1z = tan( (PhaseBoost*d2r+90*d2r+2*atan(f1/fpd) )/2); %f1/fz
f1z = abs(f1z);
fzd = f1/abs(f1z);
% Mag_comp_f1 is the Magnitude of the comp. network at f1
Mag_comp_f1 = -20*log10(2*pi*f1)+20*log10(1+(f1z)^2)-20*
log10
  (1 +(f1/fpd)^2)
Ph_comp = -90 + 2*atan(f1/fzd)/d2r -2*atan(f1/fpd)/d2r
if ( (Mag_comp_f1-GainBoost) >1)
  df = 2;% frequency resolution
  fpd = fpd+df;
elseif ( (Mag_comp_f1-GainBoost) >0.1)
  df = 0.01;
  fpd = fpd+df;
elseif ( (Mag_comp_f1-GainBoost) <-1)
  df = 2;
  fpd = fpd-df;
```

```
elseif ((Mag_comp_f1-GainBoost) <−0.1)
  df = 0.01;
  fpd = fpd-df;
  else
    m = 0; % stop the while
  end
end
% check phase
Ph_comp = −90 + 2*atan(f1/fzd)/d2r − 2*atan(f1/fpd)/d2r;
% Claculate k1 and k2
% k1 is the gain of the comp network at fzd
k1_db = −20*log10(2*pi*fzd)+20*log10(1+(fzd/fzd)^2)−20*log10
  (1 +(fzd/fpd)^2)
k1 = power(10, k1_db/20)
% k2 is the gain of the comp network at fpd
k2_db = −20*log10(2*pi*fpd) + 20*log10(1 +(fpd/fzd)^2)− 20*log10
  (1 +(fpd/fpd)^2)
k2 = power(10, k2_db/20)
% calculate components
R1 = 10e3; % selected by designer
R2 = k1*R1
R3 = R1/( (fpd/fzd)−1)
C1 = 1/(2*pi*R2*fzd)
C2 = C1/( (fpd/fzd)-1)
C3 = 1/(2*pi*R3*fpd)
```

The result of the calculation is:

```
Mag_comp_f1 = −7.0985
Ph_comp = 32
k1_db = −24.6094
k1 = 0.0588
k2_db = −5.0259
k2 = 0.5607
R2 = 588.2076
R3 = 269.7258
C1 = 5.0034e−005
C2 = 1.3496e−006
C3 = 2.8658e−006
```

The components of the compensation network may be optimized by performing small-signal AC simulations and adjusting their values to obtain the desired phase margin. Once final values of the components of the compensation network have been calculated, we are ready to evaluate the transient

closed-loop response of the switching converter. Due to unmodeled dynamics, the phase and gain contributions of the compensation network were changed to obtain a PhaseBoost = 52; GainBoost = −8 db; leading to the component values shown in Figure 9.44. The output voltage is shown in Figure 9.45 for a switching frequency $f_s = 1$ kHz.

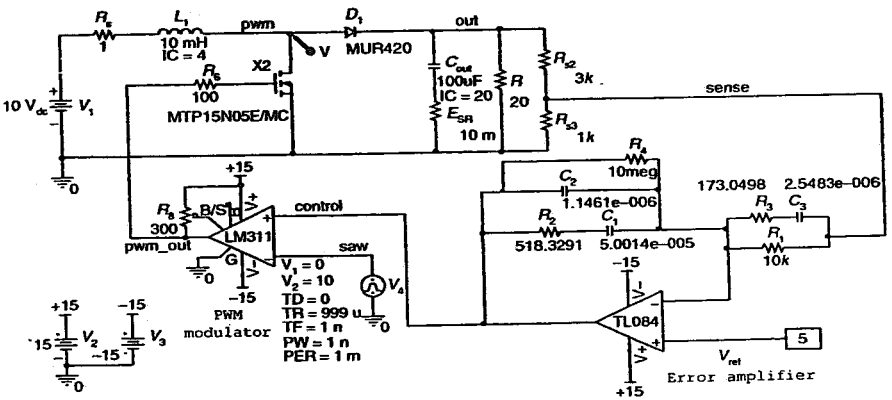


Figure 9.44 Boost switching converter with PID compensator.

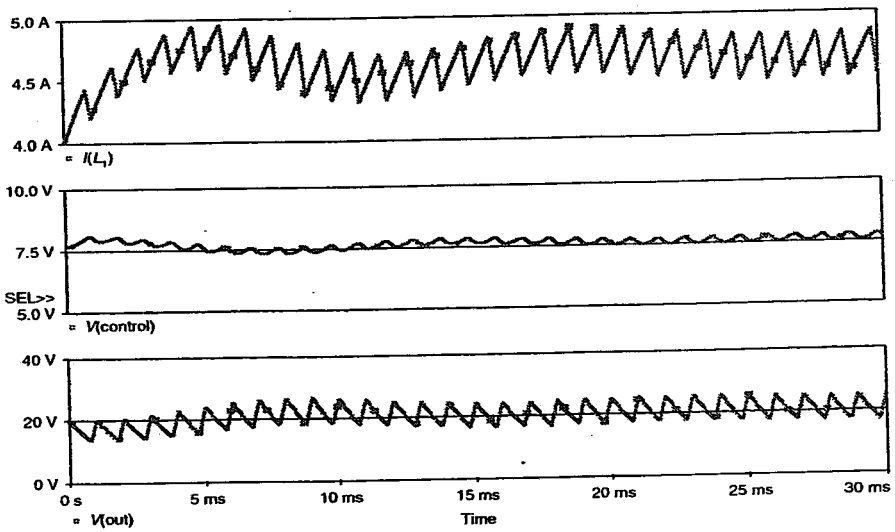


Figure 9.45 Simulation results with a PID compensator.

9.5.6.2 PI Compensation

Another compensation frequently used in voltage-mode boost converters is the PI compensation. The PI compensator is easier to calculate and requires fewer components, but it leads to smaller bandwidths and slower transient responses. The small-signal model for a PI compensator is shown in Figure 9.46.

The transfer function of the compensation network is

$$\mathrm{TF} = \frac{sC_1R_1 + 1}{sC_1R_2}. \tag{9.10}$$

Therefore, it has a pole at $s = 0$ and a zero at $s = -1/R_1C_1$. The phase of this compensation network starts at $-90°$ due to the pole at the origin and adds positive phase according to the location of the zero. From the Bode plots of Figure 9.47, we measured the frequency at which the uncompensated loop response reaches 90°, i.e., 53 Hz and we set f_1 at this point, thus $f_1 = 53$ Hz. Then we calculated R_1 and C_1 to set the zero at the same frequency. In this way, the phase of the loop gain at f_1 is: $-180°$ (inversion) $-90°$ (pole at the

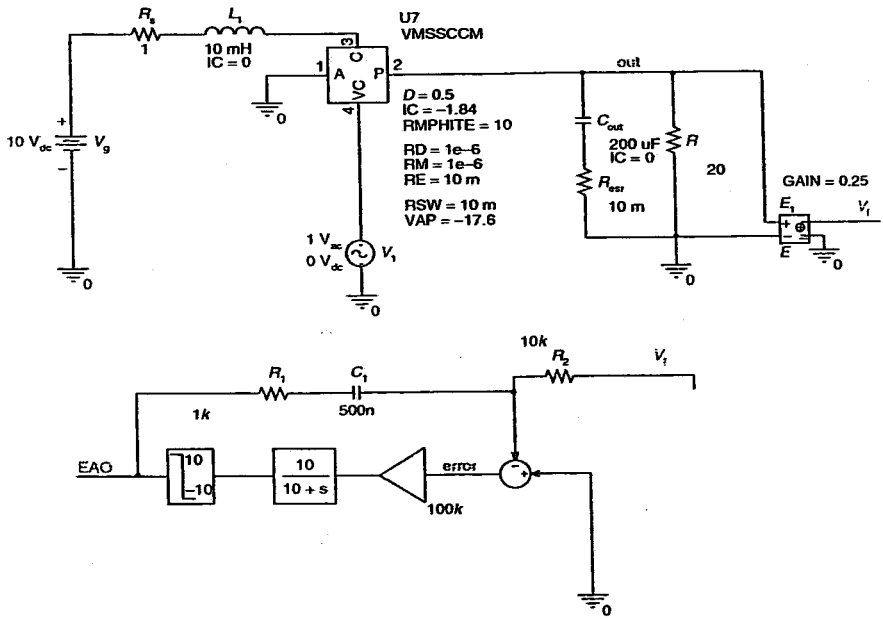


Figure 9.46 Small-signal model of the boost converter with PI compensation.

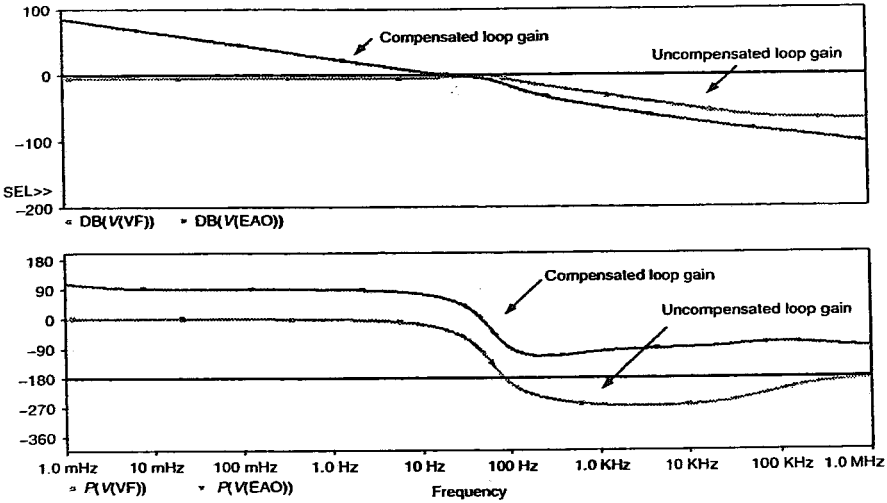


Figure 9.47 Bode plots of the uncompensated and compensated loop gains.

origin) $-90°$ (loop phase) $+45°$(zero) $= -135°$, or a phase margin of 45°. The magnitude of the compensation network at frequencies higher than f_1 is given by R_1/R_2. The magnitude of the uncompensated loop gain at f_1 is -1.45 dB. Therefore, to force the magnitude of the compensated loop gain to 0 db at f_1, we set $R_1/R_2 = 1.45$ dB or 1.18 (V/V). Choosing $R_2 = 10\,\text{k}\Omega$, results in $R_1 = 11.8\,\text{k}\Omega$ and $C = 254$ nf. These are starting values; the final values are obtained from the simulation results.

Figure 9.48 shows the schematic diagram of the boost converter with a PI compensator using ABM blocks. C_2 and R_3 were added to improve convergence. The sawtooth generator was adjusted for a 10-kHz switching frequency. The corresponding inductor current, output voltage, and control waveforms are shown in Figure 9.49. Notice that after an initial perturbation applied at $t = 0$, the waveforms slowly reach the steady-state value at the end of the simulation at $t = 30$ ms. The PI controller was simulated using vendor models, as shown in Figure 9.50. The simulation results, shown in Figure 9.51, are very similar to those obtained using ABM blocks.

Transient simulations using vendor models require longer execution time and generate much larger output files. They also present more convergence problems; therefore, they should be used only when they are strictly necessary. The OPTIONS used in this simulation, as extracted from the output file are:

```
*Analysis directives:
.TRAN 0 30m 0 10n SKIPBP
```

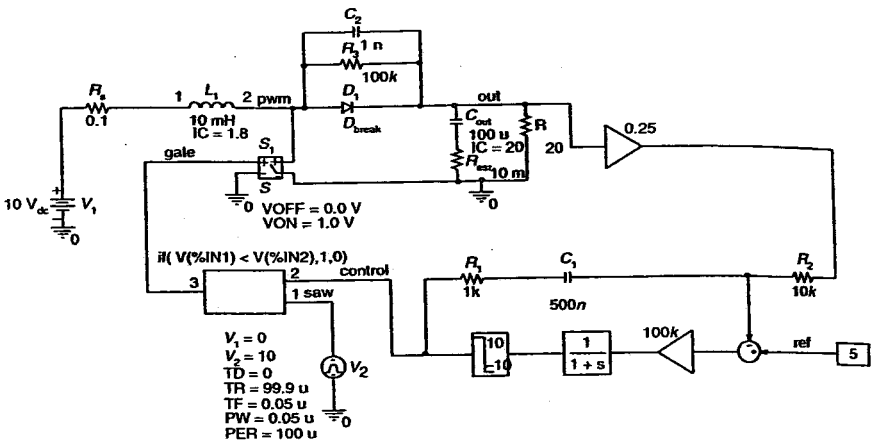


Figure 9.48 PI compensation using ABM blocks.

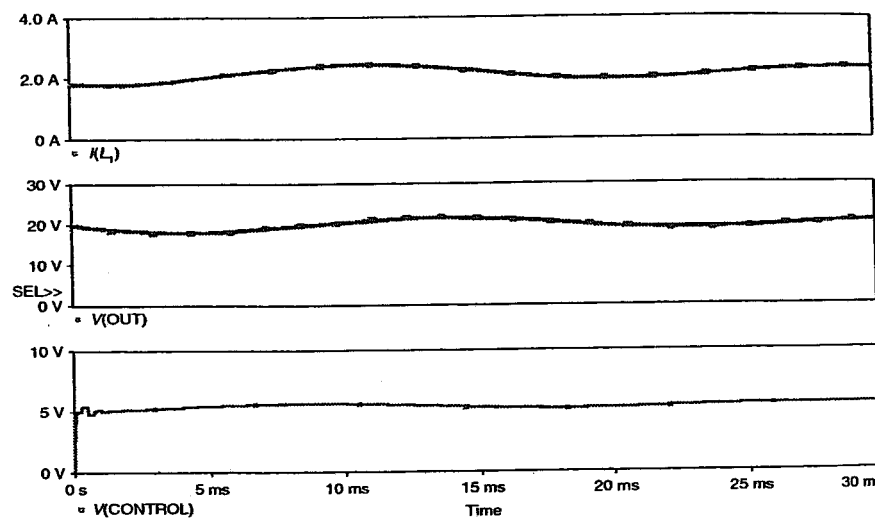


Figure 9.49 Simulation results of the PI compensation using ABM blocks.

```
.OPTIONS STEPGMIN
.OPTIONS PREORDER
.OPTIONS ABSTOL = 10.0 p
.OPTIONS CHGTOL = 0.1 p
.OPTIONS ITL2 = 200
```

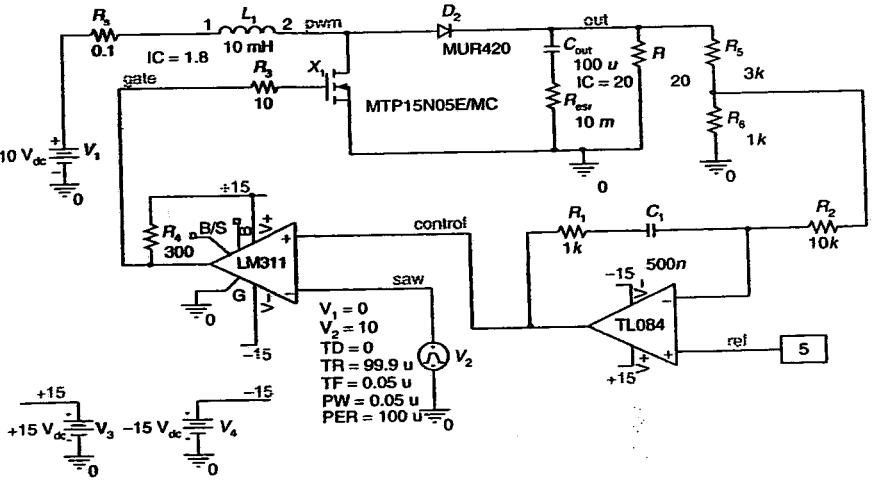


Figure 9.50 PI compensation using vendor models.

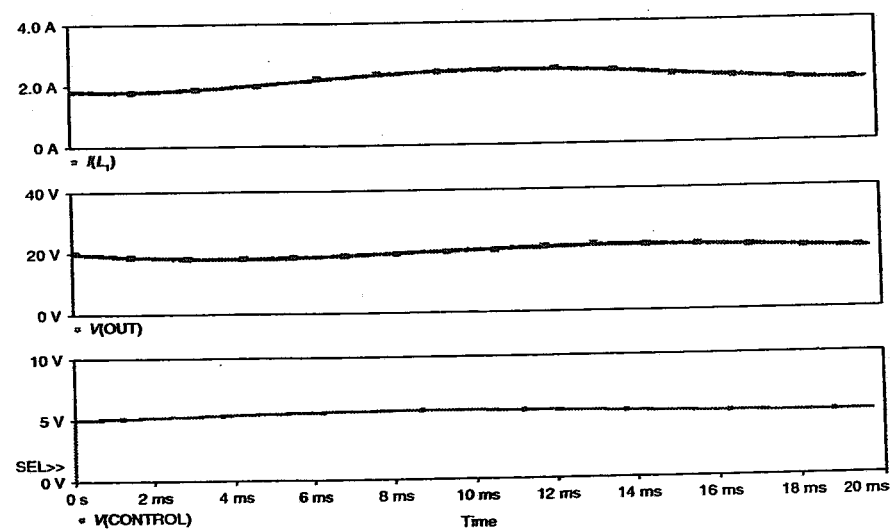


Figure 9.51 Simulation results of the PI compensation using vendor models.

```
.OPTIONS ITL4 = 400
.OPTIONS RELTOL = 0.01
.OPTIONS VNTOL = 10.0 u
```

This simulation ended before the reaching the final time because the data file became larger than the program can handle, giving he following error message:

```
I/O ERROR – Probe file size exceeds 2000000000
JOB ABORTED
TOTAL JOB TIME 912.11
```

The reader must note the large amount of data generated by this simulation and the long execution time required. If just a transient stability check was needed, a small-signal simulation using an average model or switching simulations with ABM blocks would have been sufficient.

9.6 CREATING CAPTURE SYMBOLS FOR PSPICE SIMULATION

Vendors often provide PSpice models for their circuit components. They are normally provided in a text file with extension .LIB; if the file has a different extension, it should be changed to .LIB. A good practice is to save the model libraries in a personal folder to avoid losing them. Start the PSpice Model Editor and from the File menu, choose Create Parts. Browse to find the input model library (.LIB file) and click OK to start. The message log should show 0 errors. This step creates an .OBL file with a schematic symbol linked to your model. The created symbol will have a meaningful shape if the model was provided with a .MODEL statement; in case of a .SUBCIRCUIT (sometimes called a macromodel) representation, the symbol will be a square box.

To place the new part into the schematic, open Capture, and from the Place menu choose Part. Click Add library, then find and add the new ".OLB" file. The simulator should be linked to the model library. Before running the simulation, the model library (.LIB file) is to be added into the simulation profile. In Capture from the PSpice menu, choose Edit Simulation Profile. Click the Libraries tab. Use the Browse button to find and then add the vendor ".LIB" file. The library can be added for the current design only or it can be made available for all designs. If you do not like the square box symbol created from the .SUBCIRCUIT model, you may create your own symbol. For more information, please refer to the PSpice A/D User's Guide (pspicead.pdf), in the chapter "Creating Parts for Models" [2].

9.7 SOLVING CONVERGENCE PROBLEMS [8]

This section gives a brief overview of the convergence problems commonly encountered in PSpice simulations and tips on how to solve

them. For a more detailed explanation, refer to PSpice User's Guide [2] and Rashid [3].

Convergence problems may arise in PSpice when solving for the bias point, DC sweep, and transient analysis of analog devices. PSpice uses the Newton–Raphson algorithm to solve the nonlinear equations in these analyses. The algorithm is guaranteed to converge only if the analysis is started close to the solution. If the initial guess is far away from the solution, it may cause a convergence failure or even a false convergence. When PSpice cannot find a solution to the nonlinear circuit equations, it gives a "convergence problem" message. The message gives a clue to which part of the circuit is causing the problem. Looking at these devices or nodes, or both, is a good starting point to solve the problems. The AC and noise analyses are linear and do not use an iterative algorithm, digital devices are evaluated using Boolean algebra, so the following discussion does not apply to both of them.

PSpice solves the nonlinear equations using an iterative algorithm. Starting from the initial guess, the algorithm calculates the node voltages and the mesh currents. The currents are then used to recalculate the node voltages and the algorithm keeps repeating until the entire node voltages settle to within certain tolerance limits set by various .OPTIONS parameters. If the node voltages do not settle down within a certain number of iterations, an error message will be issued. The error message will depend on the type of analysis performed.

9.7.1 DC Analysis Error Messages

The DC analysis calculates the small-signal bias points before starting the AC analysis or the initial transient solution for the transient analysis. Solutions to the DC analysis may fail to converge because of incorrect initial voltage guesses, model discontinuities, unstable or bistable operation, or unrealistic circuit impedances. The DC analysis will then issue an error message, such as "No convergence in DC analysis," "PIVTOL Error," "Singular Matrix," or "Gmin/Source Stepping Failed." When an error is found during the DC analysis, SPICE will then terminate the run because both the AC and transient analyses require an initial stable operating point in order to start. The DC SWEEP analysis may give "No Convergence in DC analysis at Step = ###" error message.

9.7.2 Transient Analysis Error Messages

During the transient analysis, the iterative process is repeated for each individual time step. If the node voltages do not settle down, the time step is reduced and SPICE tries again to determine the node voltages. If the time

step is reduced beyond a certain fraction of the total analysis time, the transient analysis will issue an error message "Time step too small" and the analysis will be halted. Transient analysis failures are usually due to model discontinuities or unrealistic circuit, source, or parasitic modeling.

9.7.3 Solutions to Convergence Problems

There are two ways to solve convergence problems; the first only tries to fix the symptoms by adjusting the simulator options; while the other attacks the root cause of the convergence problems. Invariably, the user will find that once the circuit is properly modeled, many of the modifications of the OPTIONS parameters will no longer be required. It should be noted that solutions involving simulation options may simply mask the underlying circuit instabilities.

The following techniques can be used to solve most convergence problems. When a convergence problem is encountered, the reader should follow the indications in the given order until convergence is achieved.

9.7.4 Bias Point (DC) Convergence

In case the calculation of the bias point fails to converge, the circuit topology and connectivity should first be checked, followed by modeling of circuit components. The PSpice options are checked to ensure that they are properly defined.

9.7.5 Checking Circuit Topology and Connectivity

- Make sure that all of the circuit connections are valid.
- Check for incorrect node numbering or dangling nodes.
- Verify component polarity.
- Check for syntax mistakes.
- Make sure that the correct PSpice units (i.e., MEG for 1E6, not M, which means mili in simulations) are used.
- Make sure that there is a DC path from every node to ground.
- Make sure that there are at least two connections at every node.
- Make sure that capacitors and/or current sources are not connected in series.
- Make sure that no (groups of) nodes are isolated from ground by current sources and/or capacitors.
- Make sure that there are no loops of inductors and/or voltage sources only.
- Place the ground (node 0) somewhere in the circuit.

- Be careful when floating grounds (e.g., chassis ground) are used; a large resistor should be connected from the floating node to ground. All nodes will be reported as floating if "0 ground" is not used.
- Make sure that voltage–current generators use realistic values, and verify that the syntax is correct.
- Make sure that dependent source gains are correct, and that E/G element expressions are reasonable. Verify that division by zero or LOG(0) cannot occur.
- Voltages and currents in PSpice are limited to the range $\pm 1 \times 10^{10}$. Care must be taken that the output of behavioral modeling expressions falls within this range.
- Make sure that there are no unrealistic model parameters, especially if the models are manually entered into the netlist.
- Avoid using digital components unless really necessary.
- Initialize the digital nodes with valid digital values to ensure the state is not ambiguous.
- Avoid situations where an ideal current source delivers current into a reverse-biased p–n junction without a shunt resistance. This is because p–n junctions in PSpice have no leakage resistance. As such, the junction voltage would go beyond 1×10^{10} V.

9.7.5.1 Setting up the Options for the Analog Simulation

Since Spice was originally designed for integrated circuits simulation, the default values of some overall parameters are not optimal for power electronic circuits. Some of the simulation parameters may have to be changed using the following guidelines.

- Increase ITL1 to 400. This increases the number of DC iterations that PSpice will perform before it gives up. In all, but the most complex circuits, further increases in ITL1 will not typically aid convergence.
- Use NODESETs to set node voltages to the nearest reasonable guess at their DC values, particularly at nodes that are isolated by high impedances, and at nodes that are inputs to high-gain devices. NODESETs hold these voltages at the specified value while the rest of the circuit converges to a reasonably stable point, and then "releases" these voltages for a few more iterations to find the final, complete solution.
- Enable the GMIN stepping algorithm [9] to aid with the bias point convergence.

- Set PREORDER in Simulation Profiles options. This is more important while editing schematic for marginally convergent circuits.
- Power electronic circuits may *not* require tight current–voltage tolerances. Setting the value of ABSTOL to 1 μ will help in the case of circuits that have currents which are larger than several amperes to converge.
- Unless the circuit conducts kiloamperes of current, however, setting ABSTOL to a value greater than 1 μ will cause more convergence problems than solving it.
- PSpice does not always converge when relaxed tolerances are used. For example, setting the tolerance option, RELTOL, to a value, which is greater than 0.01 can actually cause convergence problems.
- Setting GMIN to a value between 1*n* and 10*n* will often solve convergence problems.
- Setting GMIN to a value greater than 10*n* may cause convergence problems.

9.7.6 Transient Convergence

The transient analysis can fail to complete if the time step becomes too small. This can be due to either (a) the Newton–Raphson iterations would not converge even for the smallest time step size or (b) circuit paramaters are changing faster than can be accommodated by the minimum step size.

The circuit topology and connectivity should first be checked, followed by the modeling of circuit components. Finally, the PSpice options should be checked to ensure that they are properly set.

9.7.6.1 Circuit Topology and Connectivity

- Avoid using digital components unless really necessary.
- Initialize the nodes with valid digital value to ensure that there are no ambiguous states. These can cause the time step to go unnecessarily too small, and hence, a transient convergence issue.
- Use RC snubbers around diodes.
- Add capacitance for all semiconductor junctions (if no specific value is known: CJO = 3 pF for diodes, CJC and CJE = 5 pF for BJTs, CGS and CGD = 5 pF for JFETs and GaAsFETs, CGDO and CGSO = 5 pF for MOSFETs).
- Add realistic circuit and element parasitics.
- *Parasitic capacitances*: It is important that switching times be nonzero. This is assured if devices have parasitic capacitances. The semiconductor model libraries in PSpice have such capacitances. If

switches or controlled sources, or both, are used, then care should be taken to ensure that no sections of circuitry could try to switch in zero time.

- *Inductors and transformers*: It is recommended that all inductors have a parallel resistor (series resistance is good for modeling DC effects but does not limit the inductor's bandwidth). The parallel resistor gives a good model for eddy current loss and limits the bandwidth of the inductor. The size of resistor should be set to be equal to the inductor's impedance at the frequency at which its Q begins to roll off.
- Look for waveforms that transition vertically (up or down) at the point during which the analysis halts. These are the key nodes, which should be examined for problems.
- Increase the rise and fall times of the PULSE sources.
- Ensure that there is no unreasonably large capacitor or inductor.

9.7.6.2 PSpice Options

Set RELTOL = 0.01. This option is encouraged for most simulations since the reduction of RELTOL can increase the simulation speed by 10% to 50%. Only a minor loss in accuracy usually results. A useful recommendation is to set RELTOL to 0.01 for initial simulations, and then reset it to its default value of 0.001 when a more accurate answer is required. Setting RELTOL to a value less than 0.001 is generally not required.

Reduce the accuracy of ABSTOL/VNTOL if current/voltage levels allow it. ABSTOL and VNTOL should be set to about eight orders of magnitude below the level of the maximum voltage and current. The default values are ABSTOL = 1 pA and VNTOL = 1 uV. These values are generally associated with IC designs.

Increase ITL4, but not more than 100. This increases the number of transient iterations that PSpice will attempt at each time step before it gives up. This is particularly effective in solving convergence problems when the simulation needs to cover a long time period, and fast transitions occur within the circuit during that time. Values greater than 100 will not usually bring convergence.

Skipping the bias point: The SKIPBP option for the transient analysis skips the bias point calculation. In this case the transient analysis has no known solution to start from and, therefore, is not assured of converging at the first time point. Because of this, its use is not recommended. Its inclusion in PSpice is to maintain compatibility with UC Berkeley SPICE.

Any applicable .IC and IC= initial conditions statements should be added to assist in the initial stages of the transient analysis. The initial

conditions should be chosen carefully because a poor setting may cause convergence difficulties.

9.8 SWITCHING CONVERTER SIMULATION USING MATLAB

MATLAB [10] is a very convenient tool for the analysis of switching converters using the state-space averaging method and transfer functions. MATLAB can handle matrices and polynomials easily. This section introduces the use of MATLAB for switching converter analysis using an example.

9.8.1 Working with Transfer Functions

Consider a buck converter designed to operate in the continuous conduction mode having the following parameters: $R = 4\,\Omega$, $L = 1.330\,\text{mH}$, $C = 94\,\mu\text{f}$, $V_s = 42\,\text{V}$, $V_a = 12\,\text{V}$. The transfer function of a boost converter obtained using the averaged-switch model can be expressed as

$$\frac{\hat{v}_o(s)}{\hat{d}(s)} = K_d \frac{(1 + (s/s_{z1}))(1 - (s/s_{z2}))}{1 + (s/\omega_o Q) + (s^2/\omega_o^2)}, \tag{9.11}$$

where

$$K_d = \frac{V_s}{(1 - D)^2}, \tag{9.12}$$

$$s_{z1} = \frac{1}{R_{esr} C}, \tag{9.13}$$

$$s_{z2} = \frac{(1 - D)^2}{L}(R - R_{esr} \| R) - \frac{R_{ind}}{L}, \tag{9.14}$$

$$\omega_o = \frac{1}{\sqrt{LC}} \sqrt{\frac{R_{ind} + r_e D(1 - D)}{R_{esr} + R}}, \tag{9.15}$$

$$r_e = R_{esr} \| R, \tag{9.16}$$

and

$$Q = \frac{\omega_o}{((R_{ind} + r_e(1-D))/L) + (1/C(R_{esr} + R))}. \tag{9.17}$$

The listings for the MATLAB simulation are as follows:

```
% this is a comment
% parameters
R = 4;
L = 1.330 e−3;
Rind = 100 e−3;
C = 94 e−6;
Resr = 10 e−3
Vs = 42;
Va = 12;
D = Va/Vs;
Kd = Vs/(1-D)^2;
Sz1 = 1/(Resr*C);
Req = R−(Resr* R/(Resr+R) );
Sz2 = (1/L)* (1-D)^2* Req−Rind/L;
Re = (Resr*R)/(Resr+R);
Wo = (1/sqrt(L*C))*sqrt( (Rind+re* D*(1-D) )/ (Resr+R));
Q = Wo/(((Rind+ re*(1-D))/ L)+(1/(C*(Resr+R))));
```

The semicolon at the end of each line prevents the value to be displayed when the simulation is running. If the result of a calculation is desired, omit the semicolon.

% define numerator $\dfrac{\hat{v}_o(s)}{\hat{d}(s)} = K_d \dfrac{(1 + (s/s_{z1}))(1 - (s/s_{z2}))}{1 + (s/\omega_o Q) + (s^2/\omega_o^2)}$

```
% polynomials are entered in descending order of S.
n1 = [1/Sz1 1]
n2 = [−1/Sz2 1]
NUM = conv(n1,n2)
% the convolution realizes the product of 2 polynomials
% define denumerator
DEN = [1/(Wo^2) 1/(Wo*Q) 1]
% create TF variable
sysTF = Kd*tf(NUM,DEN)
```

which returns

Transfer function:

$$\text{sysTF} = \frac{-5.317\,\text{e}-008\,\text{s}\text{\^{}}2 - 0.05648\,\text{s} + 82.32}{4.913\,\text{e}-006\,\text{s}\text{\^{}}2 + 0.01343\,\text{s} + 1}$$

The location of the poles can be found using

```
poles = roots(DEN)
```

and the frequency response can be plotted using

```
bode(sysTF)
```

resulting in the plot shown in Figure 9.52.

The small signal transient step response can be plotted using

```
Figure % this command opens a new figure window
step(sysTF)
```

This yields the plot of the step response shown in Figure 9.53.

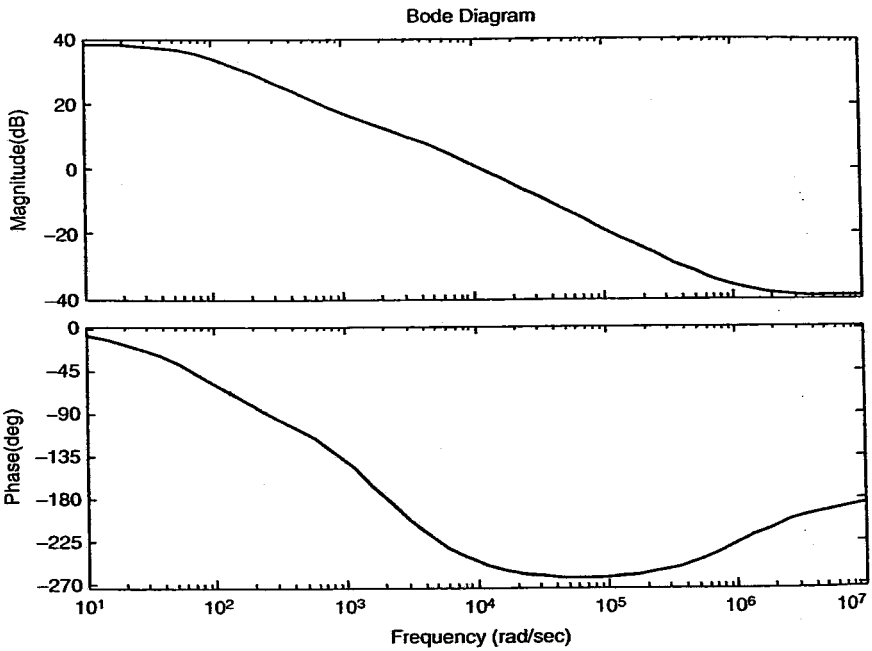


Figure 9.52 Bode plot of the system under study.

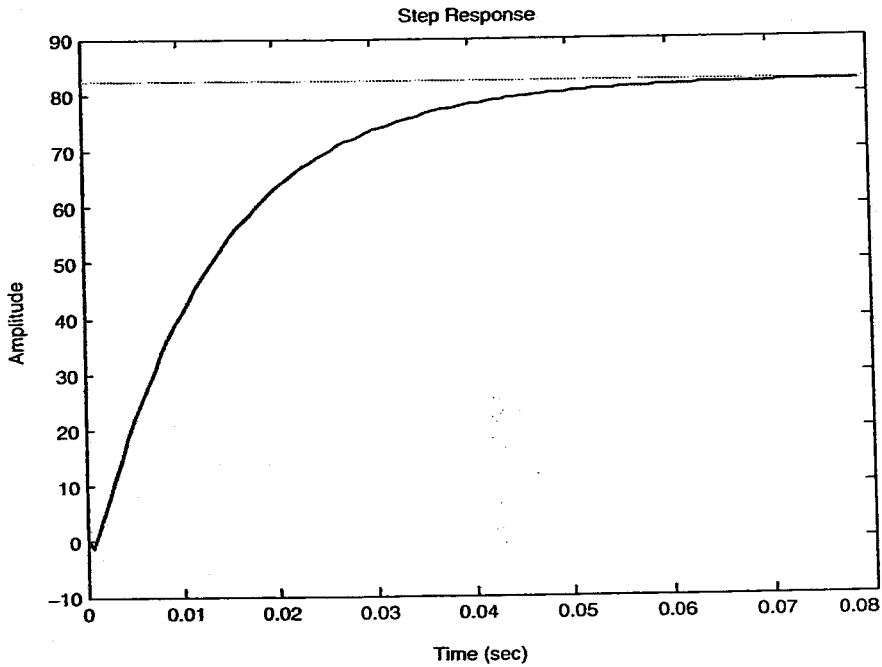


Figure 9.53 Step response of the system under study.

9.8.2 Working with Matrices

Consider a buck converter designed to operate in the continuous conduction mode having the following parameters: $R = 4\ \Omega$, $L = 1.330\,\text{mH}$, $C = 94\,\mu\text{f}$, $V_s = 42\,\text{V}$, $V_a = 12\,\text{V}$.

The model parameters can be defined by:

```
% state-space averaged model of a Buck converter
Rload = 4; % load resistance
L = 1.330E-3; % inductance
cap = 94E-6; % capacitance
Ts = 1E-4; % switching period
Vs = 42; % input DC voltage
Vref = 12; % desired output voltage
```

The average duty cycle is

```
D = Vref/(Vs); % ideal duty cycle
```

From state–space analysis of a buck converter in Chapter 6, the small-signal averaged state–space equations are

$$\dot{\hat{x}} = \begin{bmatrix} 0 & -(1/L) \\ 1/C & -(1/RC) \end{bmatrix} \begin{bmatrix} \hat{x}_1 \\ \hat{x}_2 \end{bmatrix} + \begin{bmatrix} D/L \\ 0 \end{bmatrix} \hat{u} + \begin{bmatrix} V_s/L \\ 0 \end{bmatrix} \hat{d}. \tag{9.18}$$

The matrices of the averaged state–space model A, B, and C are entered as follows:

```
A=[0
-1/L 1/cap-1/(Rload*cap)]
B1=[1/L 0]; % during Ton
B2=[0 0]; % during Toff
B=B1*D+B2*(1-D)
C=[0 1];
```

The open-loop poles of the Buck converter can be calculated by using the eig( ) function to evaluate the eigenvalues of the system matrix A.

```
OLpoles = eig(A)
```

The state–space open-loop model is defined as sysOL by the SS command. The step response of the open-loop converter can be plotted using the step( ) command:

```
sysOL=ss(A,B,C,0)
step(sysOL)
```

A "help" statement can be used to learn more on any MATLAB command. For example,

```
help step
```

Figure 9.54 shows the transient response of the small-signal model of the converter for a step input at $\hat{u}_1$ obtained using the step( ) command.

The command line

```
gamma=[Vs/L 0];
```

defines the vector that reflects the changes in the duty cycle on the state variables.

The feedback gains can be found in order to determine the closed-loop poles at any desired location. In this case, the closed-loop poles are arbitrarily chosen to be located at $(-0.3298 \pm j\ 0.1)$. Start by defining a vector containing the desired closed-loop poles:

```
P = 1e3* [-0.3298 + 0.10i -0.3298 -0.10i]';
```

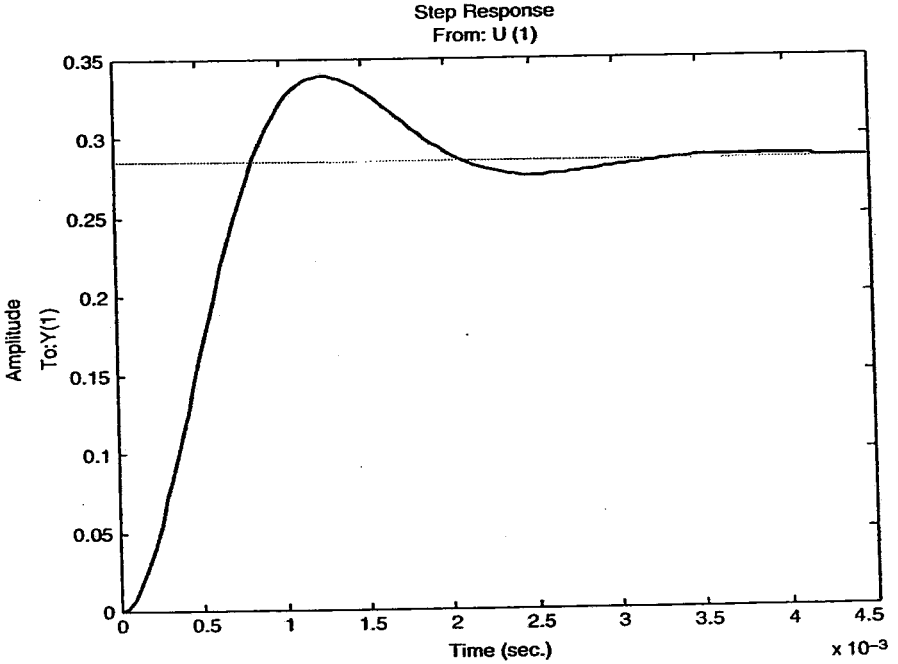


Figure 9.54 Step response of the linearized buck converter.

Notice the notation for the complex numbers. The "i" is placed right after the imaginary part. The apostrophe represents the transpose operation.

Now by using the place() command, the feedback gains can be defined as:

```
Bf = gamma*(D/Vref);
F = place(A,Bf,P)
```

The place command computes a state-feedback matrix F such that the eigenvalues of $A - Bf*F$ are those specified in vector P. No eigenvalue should have a multiplicity greater than the number of inputs.

9.9 SWITCHING CONVERTER SIMULATION USING SIMULINK

Simulink [11] is a graphical input interface for MATLAB. This section introduces its use in the simulation of the switching converters by simulating the previous transfer function and state–space examples worked using MATLAB.

9.9.1 Transfer Function Example Using Simulink

There are two different ways to describe a transfer function in Simulink, as a ratio of polynomials and as a ratio of zeroes and poles. For the previous example, the transfer function is

$$\text{sysTF} = \frac{-5.317\text{e}-8\,\text{s}\text{\^{}}2 - 0.05648\text{s} + 82.32}{4.913\text{e}-6\,\text{s}\text{\^{}}2 + 0.01343\,\text{s} + 1}$$

The numerator and denominator may be recovered from the transfer function by

```
[NUM,DEN] = TFDATA(sysTF,'v')
```

The contents of the variables NUM and DEN are then used in the Transfer Fcn block (Figure 9.55). To evaluate the step response of the system, connect a Step block from the source library and a Scope block from the sink library. Then setup the simulation parameters for a stop time of 50e–3 s and the step time at zero for the Step block. Save and run the simulation. Double-clicking on the Scope block will open the scope window and the trace of the step response will be displayed (Figure 9.56).

The To Workspace blocks make the selected Simulink variables available from the MATLAB command window. The step response can be plotted in a MATLAB figure by the plot(time, output) command.

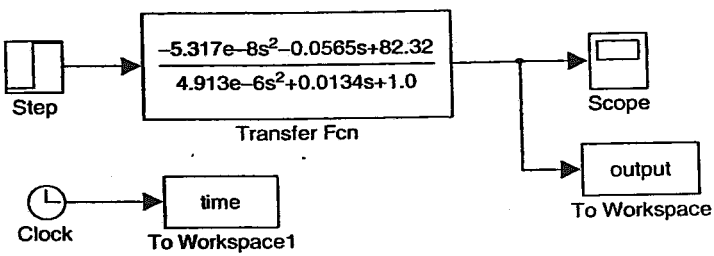


Figure 9.55 Simulink polynomial representation of a transfer function.

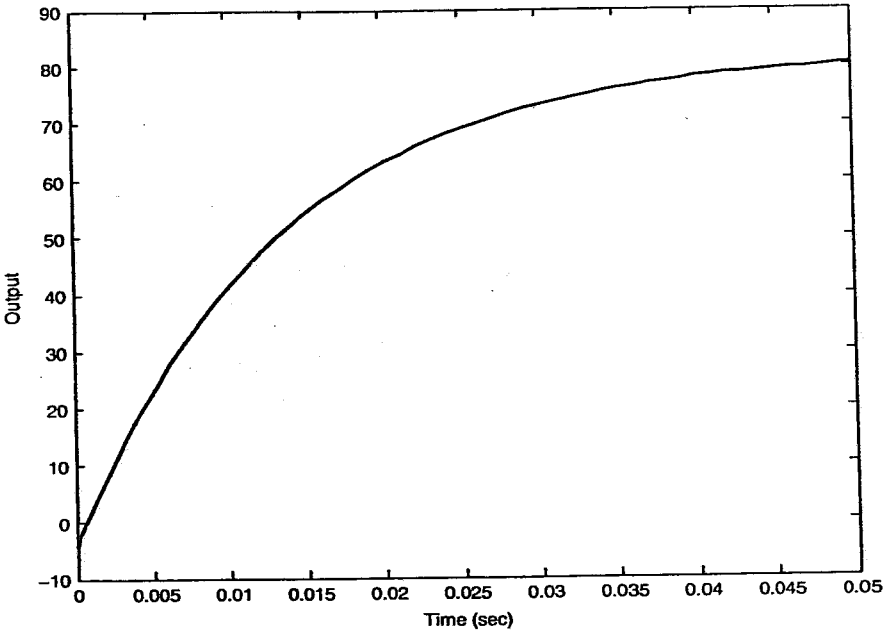


Figure 9.56 Step response.

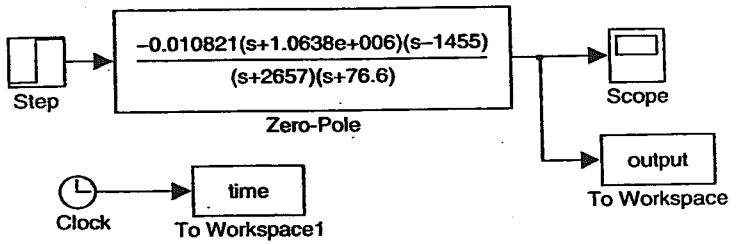


Figure 9.57 Simulink ZPG representation of the transfer function.

The zero-pole-gain form of the transfer function can be obtained using (Figure 9.57):

```
sysZPK = zpk(sysTF)
```

which yields:
Zero/pole/gain:

$$\text{sysZPK} = \frac{-0.010821(s + 1.064e006)(s - 1455)}{(s + 2657)(s + 76.6)}$$

Then, the parameters of the zero-pole block are entered as follows:

zeroes: [−1.0638e+006 +1455]
poles: [−2657 −76.6]
gain: [−0.010821]

9.9.2 State–Space Example Using Simulink

The switching converter of Equation (9.18) has the following state–space matrices:

$$A = \begin{bmatrix} 0 & 752 \\ 10638 & -2660 \end{bmatrix}$$
$$B = [214.82 \quad 0]' \tag{9.19}$$
$$C = [0 \quad 1]'$$
$$D = 0.$$

The averaged model of the switching converter using the state–space representation is shown in Figure 9.58. The parameters of the state–space block are entered as shown in Equation (9.19).

PROBLEMS

9.1. Using PSpice simulation, determine the harmonic contents of a boost converter having the following parameters: $V_s = 9\,\text{V}$, $V_a = 12\,\text{V}$, $R_L = 12\,\Omega$, $L = 1\,\text{mH}$, $C_o = 100\,\mu\text{F}$, $f_s = 1\,\text{kHz}$. Use the TIP41 BJT vendor model for the switching transistor. Comment on the harmonic contents when the switching frequency increases to 10 kHz.

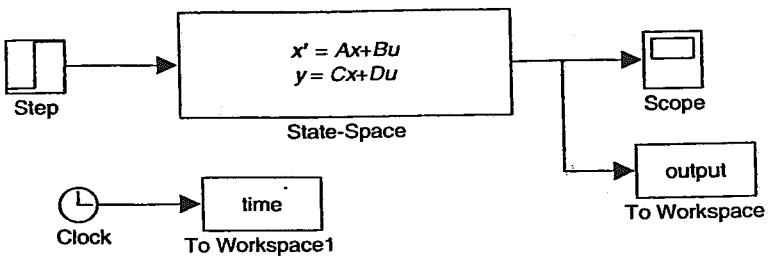


Figure 9.58 State-space representation of the switching converter.

9.2. The parameters for the flyback converter shown in Figure 4.10 are: $L_s = 500\,\mu H$, $N_p = N_s$, $k_{ps} = 0.999$, $V_s = 100\,V$, $f_s = 5\,kHz$, $R_L = 10\,\Omega$, and $C_o = 100\,\mu F$. Using PSpice, determine the duty cycle for the onset of the continuous mode of operation.

9.3. Using PSpice, simulate the Cûk converter shown in Figure 2.27 with the following parameters: $L_i = 1\,mH$, $C_t = 100\,\mu F$, $L_o = 10\,mH$, $C_o = 47\,\mu F$, $f_s = 10\,kHz$, $D = 0.4$, and $R_L = 10\,\Omega$. The switching transistor, Q_s, is a TIP41 bipolar transistor. Determine the input ripple current, voltage across the energy-transfer capacitor, and the output ripple voltage from PSpice simulations and compare these values to the calculated values.

9.4. The switching frequency of the voltage-mode PWM boost converter shown in Figure 9.29 is 20 kHz. Determine the compensation network if the unity-gain crossover frequency is 4 kHz and a phase margin of 40° is desired.

9.5. The current-mode PWM quasi-resonant ZCS buck converter from Example 3.1 is designed to have an output voltage of 6 V. Compare the calculated switching frequency to that obtained from PSpice simulation.

9.6. (a) Design an ideal buck–boost converter that would operate with a duty cycle of 60%. Choose the circuit parameters to provide an output power of 10 W. Show all the necessary calculations. (b) Simulate the circuit using ideal components and parts from the ABM library. Evaluate and plot the conversion ratio versus D. (c) Simulate the circuit including component losses and vendor models using the appropriate parts and data sheets. Evaluate and plot the conversion ratio versus D. (d) Evaluate the line and the load regulations by parametric simulations. (e) Design a closed-loop regulator for the circuit in c) using ABM parts for the control and feedback blocks. Evaluate the line and load regulations. Notice how the duty cycle varies to keep the output voltage constant.

9.7. (a) If PSpice stops running due to convergence problems during a transient analysis, explain how you would modify the circuit and the simulation options to aid with convergence. (b) How do you improve the definition of the waveform obtained in a transient simulation? (c) How do you improve the definition of the waveform obtained in an AC simulation?

9.8. Draw a closed-loop synchronous buck converter showing a generic 3-pole 2-zero compensation network. Use components from the ABM library for the error amplifier, feedback network, and PWM modulator. Design the ramp generator to provide with a 100-kHz sawtooth wave-

form swinging from 0 to 1 V. Setup the reference voltage for a 50% nominal duty cycle. Calculate Beta.

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10

Switching Converter Design: Case Studies

10.1 INTRODUCTION

Switching converters find their major application in switching power supplies. The major feature of switching power supplies is their high power packing density resulting from their high conversion efficiency. In general, the power packing density of a switching converter increases with its switching frequency. This is due to a reduction in size and weight of its storage elements as its switching frequency increases. Furthermore, the switching action of the transistor in a switching converter reduces unnecessary power losses.

Switching converters are also used in direct-current (DC) motor drives. They are commonly known as choppers. DC motor drives are widely used in applications requiring adjustable speed control, good speed regulation, and frequent starting, braking, and reversing. Some important applications are rolling mills, paper mills, battery-operated forklift trucks, battery-operated trolleys, and machine tools. Recently, induction and synchronous motors are also becoming popular in variable speed applications due to advances in their inverter speed drives.

The other lesser known application of the switching converter is in the pulse-width modulator (PWM) switching audio amplifier. PWM switching audio amplifiers have been in existence for many years. The major advantage of the PWM switching audio amplifier is in the power conversion efficiency. Class AB amplifiers, commonly used in audio amplifiers, have a maximum theoretical power conversion efficiency of less than 78.5%. However, the practical power conversion efficiency of a typical class AB amplifier is between 35% and 40% [1]. On the other hand, practical PWM switching audio amplifier offers a power conversion efficiency higher than 80%.

Even though dedicated integrated circuit controllers remain the workhorse of controllers for switching converters, microprocessor and digital-signal-processors are finding their niches as controllers for some switching converter applications. Digital-signal-processor (DSP) allows the implementation of flexible digital control, monitoring, and communication functions required in the new generation of digital power supplies. By changing the controller algorithm, a totally digital power supply platform can be achieved without changing the switching converter topology. In addition, more efficient switching converter topologies, which take advantage of advanced nonlinear digital control techniques, may be used to obtain optimum performance over the complete operating range of the power supply. Furthermore, current-mode control of switching converters can be enhanced by replacing the compensation ramp for state feedback control, thus simplifying the design of feedback gains for the desired transient response. The use of microprocessor or DSP adds signal processing capability and, therefore, makes such switching converter smarter and more versatile than those with conventional integrated-circuit controllers. Furthermore, the microprocessor- or DSP-based controller can be easily adapted to changing requirements of the switching converter through software revision. In chopper applications, microprocessor or DSP controllers allow the use of complex control algorithms to shape the responses of DC motors.

Several design examples of switching converters are presented in this chapter. The design of a simple TL594-based buck converter is first discussed. This is followed by a brief discussion on the design of a DSP-based synchronous buck converter. By changing the software, the same hardware can be re-configured to work in current-mode and in voltage-mode with the desired dynamics. This example shows the versatility of the digitally controlled switching converters. The design of a flyback converter using three different controllers is then presented. Finally, this chapter concludes with a discussion of the design and evaluation of a practical PWM switching audio amplifier. It should be noted that these designs do not include any system optimization.

10.2 VOLTAGE-MODE DISCONTINUOUS-CONDUCTION-MODE BUCK CONVERTER DESIGN

A voltage-mode, discontinuous-conduction-mode, buck converter using a TL594 pulse-width modulator [2] will be designed and evaluated. The nominal input voltage is 19 V, but fluctuates between 17 and 21 V. The output voltage for this converter is specified to be 5 V ± 5%, the load current may change from 30 mA to 0.5 A. Thus, the power rating for this buck converter is 2.5 W. A linear voltage regulator such as the UA7805CKC can be used for this application, although the power loss would be higher than that of the buck converter. The switching frequency is chosen to be 10 kHz. A phase margin of 35° is selected as a compromise between the allowable overshoot and desired rise time.

For an average output current of 265 mA, the average load resistance is

$$R_{L_{avg}} = \frac{5\text{ V}}{265\text{ mA}} = 18.8\,\Omega \tag{10.1}$$

and the maximum load (or minimum load resistance) is

$$R_{L_{min}} = \frac{V_a}{I_a} = \frac{5\text{ V}}{0.5\text{ A}} = 10\,\Omega. \tag{10.2}$$

The inductor will next be determined to guarantee the discontinuous mode of operation. Its inductance should be smaller than the critical inductance at the highest load current:

$$L \leq \frac{R_{L_{min}}(1-D)^2}{2 \cdot f_s} = \frac{10(1-0.263)^2}{2 \cdot 10000}$$
$$= 0.272 \times 10^{-3}\text{H} = 0.272\text{ mH}, \tag{10.3}$$

where D is the duty cycle of the buck converter operating in the continuous conduction mode:

$$D = \frac{V_a}{V_s} = \frac{5\text{ V}}{19\text{ V}} = 26.3\%. \tag{10.4}$$

We choose a smaller inductance value of 0.2 mH. The peak-to-peak ideal inductor ripple current is

$$\Delta I = \frac{V_s D}{f_s L} = \frac{19(0.6)}{10000(0.2 \times 10^{-3})} = 5.7\text{ A}. \tag{10.5}$$

The output capacitor should be calculated to satisfy the output voltage ripple requirements at full load, i.e., at $I_a = 0.5\,A$:

$$\frac{\Delta v_a}{V_a} \leq 5\% \quad \text{or} \quad \frac{I_a D}{f_s C V_a} \leq 5\% \tag{10.6}$$

then

$$C \geq \frac{I_a D}{f_s V_a 0.05} = 52.6\,\mu F. \tag{10.7}$$

Experimentally, we choose: $C = 3 \times 470\,\mu F$. This output capacitance is much larger than the calculated value due to a large ESR on the capacitors. As such, the ripple has to be reduced by increasing the capacitance and paralleling three capacitors. The peak-to-peak ideal capacitor ripple voltage is

$$\Delta v_c = \frac{I_a D}{f_s C} = \frac{0.5 \times 0.263}{10000 \times 1.41 \times 10^{-3}} = 0.0093\,V. \tag{10.8}$$

For a voltage-mode discontinuous-conduction-mode buck converter, the voltage conversion ratio, M, is defined as:

$$M = \frac{V_a}{V_s} = \frac{2}{1 + \sqrt{1 + (8L/RT_s D^2)}} = 0.263. \tag{10.9}$$

With a nominal input voltage of 19 V and an average output voltage of 5 V, the nominal duty cycle for a load resistance of 10 Ω is

$$D = \sqrt{\frac{8L}{RT_s\left(\left(\frac{2V_s}{V_a} - 1\right)^2 - 1\right)}} = 0.194. \tag{10.10}$$

10.2.1 Controller Design

The switching frequency of the PWM is determined by C_t and R_t. For a C_t of 0.01 μF, the required R_t for a switching frequency of 10 kHz is 10 kΩ. Due to the discontinuous-conduction-mode of operation, the buck converter yields a first-order response with a corner frequency at

$$f_p = \frac{2 - M}{2\pi(1 - M)RC} = \frac{2 - 0.263}{2\pi(1 - 0.263)10 \times 3 \times 470 \times 10^{-6}} = 15.3\,Hz. \tag{10.11}$$

Assuming an effective R_{esr} of 100 mΩ, the output capacitors introduce a zero at

$$f_{zesr} = \frac{1}{2\pi R_{esr} C} = \frac{1}{2\pi 100 \times 10^{-3} \times 3 \times 470 \times 10^{-6}}$$
$$= 1129\,\text{Hz}. \tag{10.12}$$

A reference voltage of 3 V is fed to the noninverting input of the error amplifier through a voltage divider from the on-chip 5-V reference voltage of the TL594. The sampled voltage from the output of the buck converter is fed to the inverting input of the error amplifier. Consequently, the sampling network contributes an attenuation of −4.43 dB to the open-loop magnitude response of the buck converter. Neglecting the open-loop gain of the comparator, the PWM contributes a gain of 20 $\log_{10}$ (V_s/V_p), where V_p is the peak amplitude of the sawtooth voltage. Since the peak amplitude of the sawtooth voltage is 10 V, the pulse-width modulator contributes a gain of

$$20 \log_{10} \left(\frac{19}{10}\right) = 5.57\,\text{dB}. \tag{10.13}$$

Thus, the low-frequency gain of the open-loop buck converter is 1.14 dB. Simulations of the voltage-mode discontinuous-conduction-mode buck converter were performed to verify the design. Figure 10.1 shows the schematic circuit of the open-loop buck converter using vendor models of the chosen components. The PWM modulator is modeled by ABM blocks.

The series resistance of the inductor is $R_s = 0.696\,\Omega$ and the ESR of the capacitor is $R_{esr} = 0.1\,\Omega$. The ABM2 block models an ideal PWM modulator that generates the 30% duty cycle by comparing the 10-V sawtooth signal provided by V_p with the reference voltage, V_{ref}, of 3 V. A larger duty cycle was used to compensate for the circuit losses. Figure 10.2 and Figure 10.3 show the simulated output voltage and the output voltage ripple waveforms. It can be seen that the output voltage is close to the desired value of 5 V and the ripple voltage is bounded within 0.25 V (5% of 5 V).

The simulated inductor current waveform is plotted in Figure 10.4. The inductor current is zero for a certain amount of time in one switching cycle, thus verifying that the circuit is operating in the discontinuous-conduction mode.

10.2.2 Small-Signal Model

The small-signal model of the switching converter is shown in Figure 10.5. The parameters of the error amplifier were found using the information

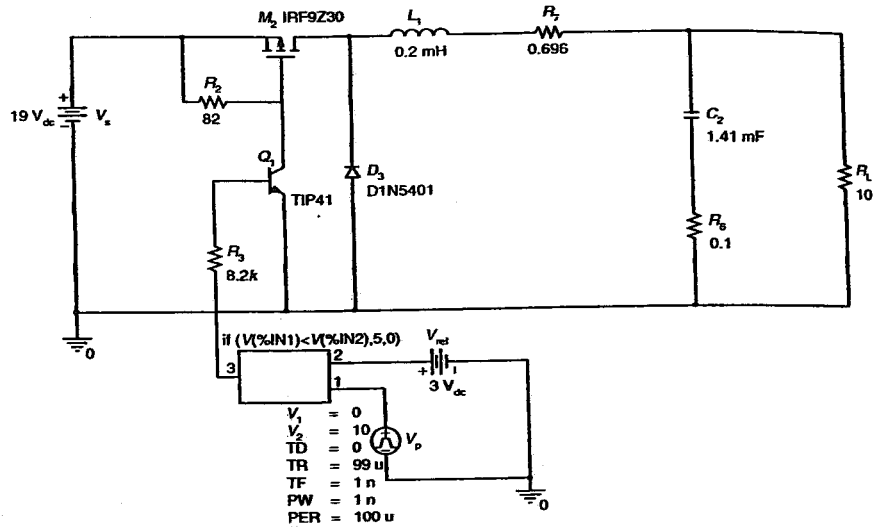

Figure 10.1 Open-loop buck converter circuit.

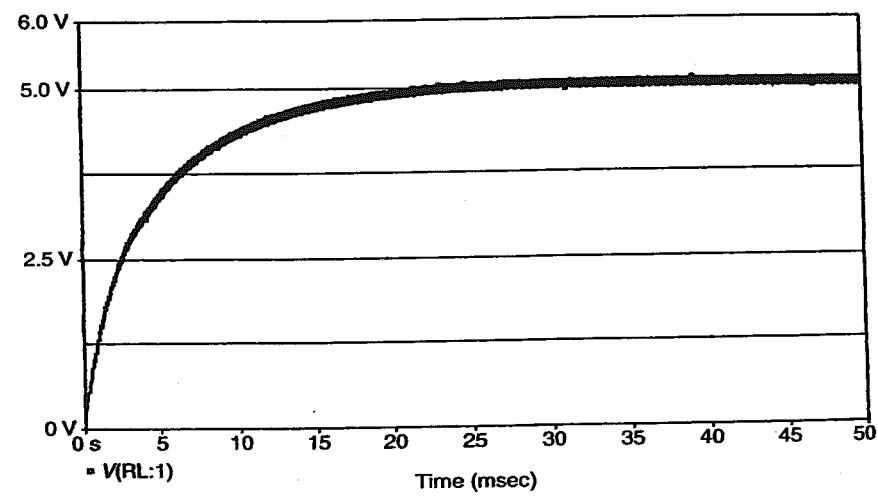

Figure 10.2 Output voltage of the open-loop buck converter.

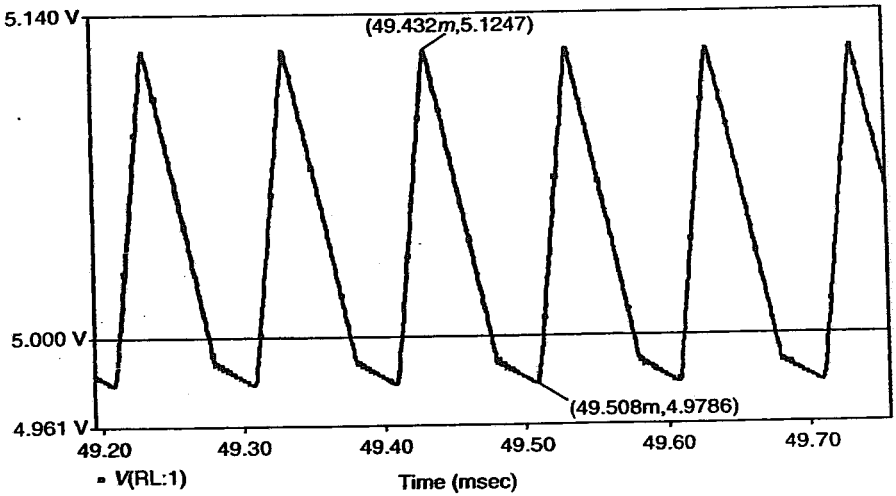

Figure 10.3 Output voltage ripple.

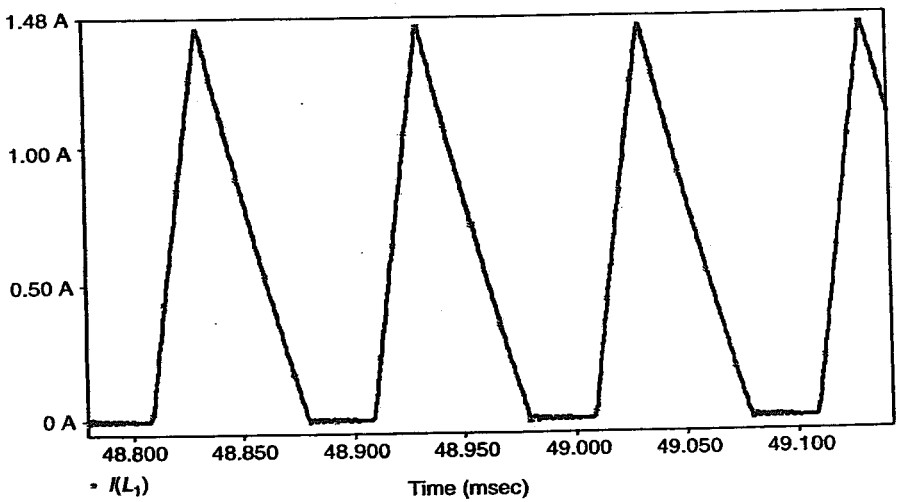

Figure 10.4 Inductor current of the open-loop buck converter.

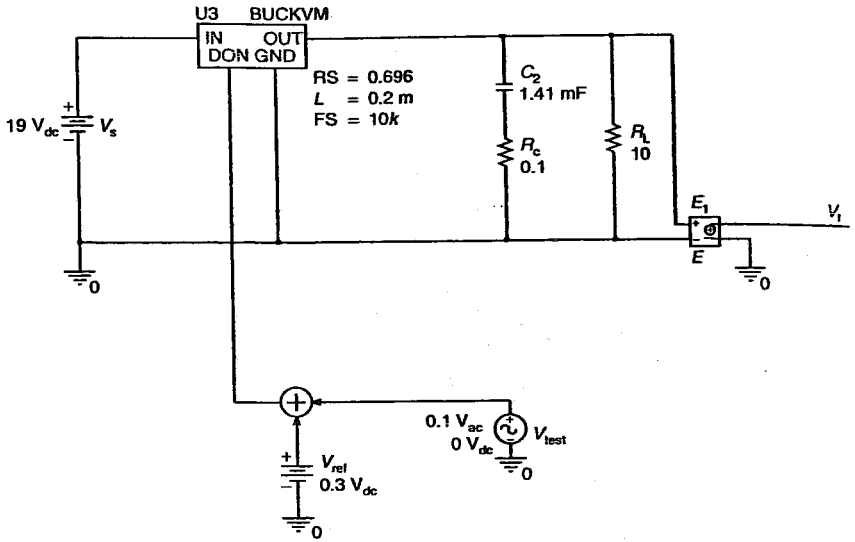

Figure 10.5 Averaged-inductor small-signal model for the loop gain.

provided in the data sheet of the TL594 controller [2]. The Bode plot of the loop gain is given in Figure 10.6.

10.2.3 Design of the Compensation Network and Error Amplifier

The unity-gain crossover frequency, f_1, was chosen to be one-tenth of the switching frequency, f_s, or 1 kHz. From the Bode plot of Figure 10.6, the magnitude of the loop gain at f_1 can be found to be -13.8 dB at a phase of $-103°$. Therefore, the compensation network should provide a gain of 13.8 dB and a phase of $-42°$ at f_1 to yield a 35° phase margin. A 2-zero and 3-pole PID compensator, as shown in Figure 10.7, was chosen as the compensation network.

The magnitude and phase of the compensation network are shown in Figure 10.8 and Figure 10.9, respectively. k_1 is the magnitude at the frequency of the double-zero (f_{zd}) and k_2 is the magnitude at the frequency of the double-pole (f_{pd}).

The phase required from the compensation network is

$$-43° = 2\tan^{-1}\left(\frac{f_1}{f_{zd}}\right) - 2\tan^{-1}\left(\frac{f_1}{f_{pd}}\right). \tag{10.14}$$

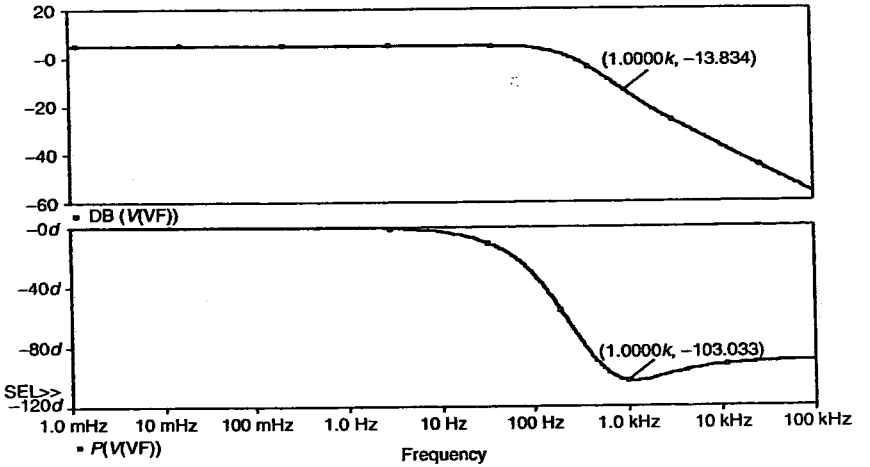

Figure 10.6 Bode plot of the loop gain, magnitude, and phase.

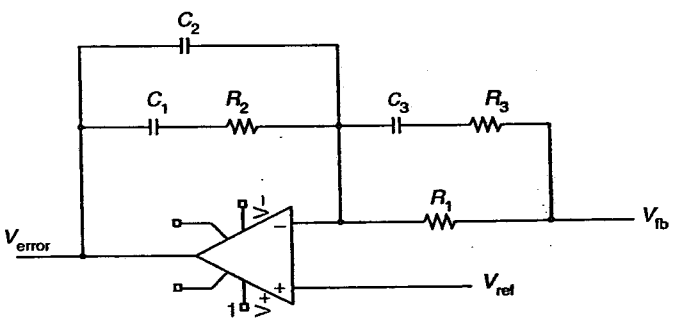

Figure 10.7 Compensation network with two zeros and three poles.

The frequency of the double pole can be written as

$$f_{pd} = \tan\left(\frac{2\tan^{-1}(f_1/f_{zd}) + 43^\circ}{2}\right). \tag{10.15}$$

From a circuit analysis of the error amplifier, we have

$$K_1 = \frac{R_2}{R_1}, \quad K_2 = \frac{R_2(R_1 + R_3)}{R_1 R_3},$$

$$f_{pd} = \frac{1}{2\pi R_3 C_3} = \frac{(C_1 + C_2)}{2\pi R_2 C_1 C_2), \quad f_{zd} = \frac{1}{2\pi R_2 C_1} = \frac{1}{2\pi(R_1 + R_3)C_3}.$$

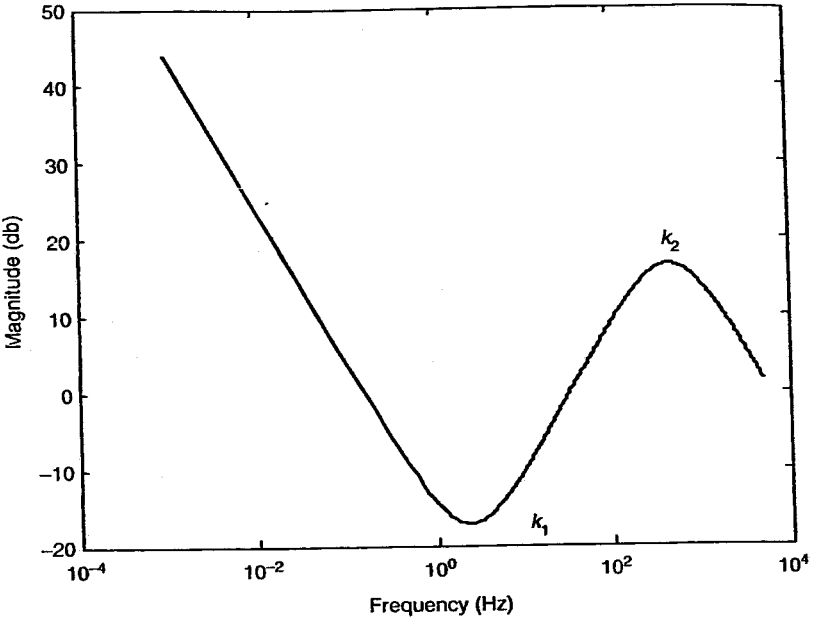

Figure 10.8 Magnitude of the compensation network.

The MATLAB program listed below calculates the pole and zero locations using a brute-force algorithm and returns the values of the network components using the following equations:

$$R_2 = k_1 R_1, \quad R_3 = \frac{R_1}{(f_{pd}/f_{zd}) - 1},$$

$$C_1 = \frac{1}{2\pi f_{zd} R_2}, \quad C_2 = \frac{C_1}{(f_{pd}/f_{zd}) - 1}, \quad C_3 = \frac{1}{2\pi f_{pd} R_3}, \tag{10.16}$$

where R_1 is previously chosen as $10\,\text{k}\Omega$.

10.2.3.1 MATLAB Program to Calculate the Compensation Networ

```
% iteratively solve for pole location on a
% 3-pole 2-zeros (PID) compensation network
PhaseBoost = −42; %needed phase boost at f1 (comp network
  phase at f1)
GainBoost = 13.8; %needed gain boost at f1 in dB
f1 = 1000; %defined by designer, has to be <(fs/2) in Hz
```

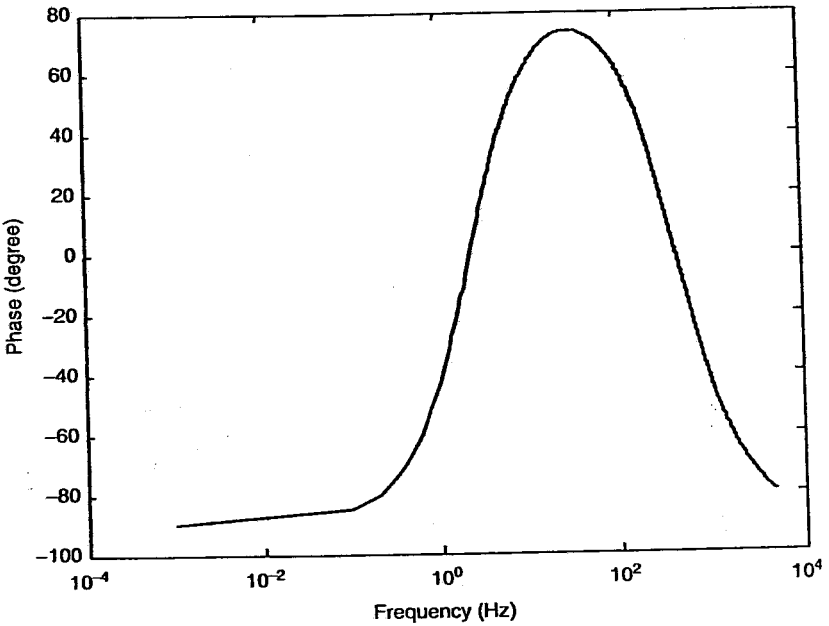

Figure 10.9 Phase of the compensation network.

```
d2r=pi/180; % degree to radian conversion
fpd=10*f1; %initial guess
m=1; %-keeps the while going
while(m),
f1z=tan( (PhaseBoost* d2r+90*d2r+ 2*atan(f1/fpd))/2); f1/fz
f1z=abs(f1z);
fzd=f1/abs(f1z);
% Mag_comp_f1 is the Magnitude of the comp. network at f1
Mag_comp_f1=−20*log10(2* pi*f1)+20*log10 (1+(f1z)^2)−20*log
   10 (1 + (f1/fpd)^2)
Ph_comp=−90 + 2*atan(f1/fzd)/d2r − 2*atan(f1/fpd)/d2r
if ((Mag_comp_f1-GainBoost) >1)
   df=2;% frequency resolution
   fpd=fpd+df;
elseif ((Mag_comp_f1-GainBoost) >0.1)
   df=0.01;
   fpd=fpd+df;
```

```
elseif ((Mag_comp_f1-GainBoost) <-1)
  df=2;
  fpd=fpd-df;
elseif ((Mag_comp_f1-GainBoost) <-0.1)
  df=0.01;
  fpd=fpd-df;
  else
  m=0; % stop the while
  end
end
% check phase
Ph_comp=-90 + 2*atan(f1/fzd)/d2r - 2*atan(f1/fpd)/d2r;
% calculate k1 and k2
% k1 is the gain of the comp net at fzd
k1_db=-20*log10(2*pi*fzd)+20*log10(1+(fzd/fzd)^2)-20*log10
  (1 + (fzd/fpd)^2)
k1=power(10, k1_db/20)
% k2 is the gain of the comp net at fpd
k2_db=-20*log10(2*pi*fpd)+20*log10(1+(fpd/fzd)^2)-
  20*log10(1+ (fpd/fpd)^2)
k2=power(10, k2_db/20)
% calculate components
R1=10e3; %selected by designer
R2=k1*R1
R3=R1/((fpd/fzd)-1)
C1=1/(2*pi* R2*fzd)
C2=C1/((fpd/fzd) -1)
C3=1/(2*pi* R3*fpd)
```

From the MATLAB simulation, the double zeros are located at 2.31 Hz with a gain of $k_1 = -17.24$ dB and double poles are located at 448 Hz with a gain of $k_2 = 16.43$ dB.

The components for the compensation network are:

$R_1 = 10\,\text{k}\Omega$, $R_2 = 1.37\,\text{k}\Omega$, $R_3 = 52\,\Omega$, $C_1 = 50\,\mu\text{F}$, $C_2 = 0.26\,\mu\text{F}$, and $C_3 = 6.8\,\mu\text{F}$.

The simulated magnitude and phase of the compensated loop gain are shown in Figure 10.10. The simulated results are slightly off from the design specifications. For example, the magnitude and phase are 4.3 dB and 139°, respectively, at 1 kHz. The zero crossing occurs at $f_1 = 1.25$ kHz, with a phase of −147°; therefore, the phase margin is 33°, which is in good agreement with the design specifications. The small-signal model of the frequency compensated buck converter is shown in Figure 10.11.

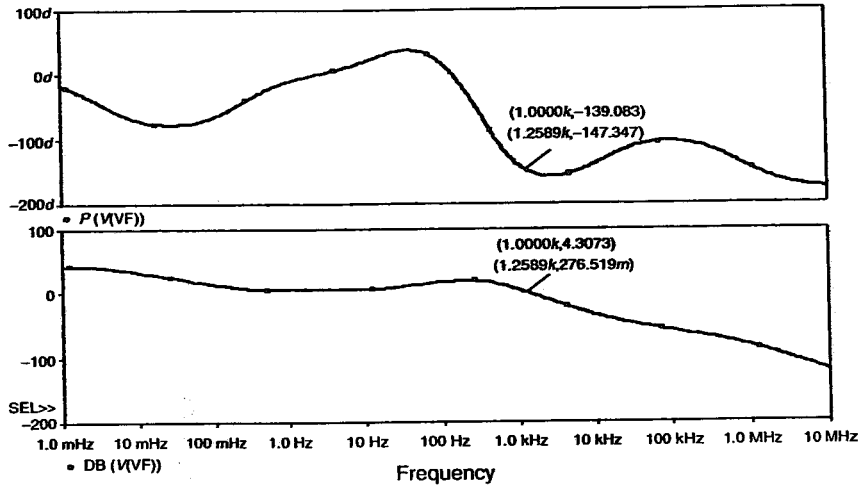

Figure 10.10 Magnitude and phase of the loop gain of the compensated circuit.

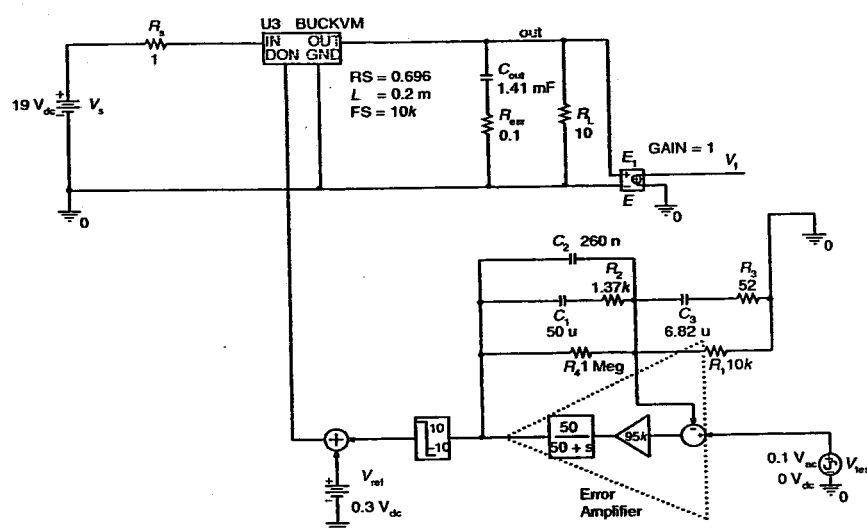

Figure 10.11 Small-signal model of the frequency-compensated buck converter

10.2.4 The Closed-Loop Buck Converter

Figure 10.12 shows the circuit schematic of the closed-loop buck converter. Components with the closest commercially available values were used. This section presents the simulation and experimental results obtained using this circuit, including line regulation, load regulation, and the characteristics of output voltage and output current versus the duty cycle.

10.2.5 Simulation Results

Simulations were performed on the closed-loop buck converter using vendor models to validate the design. Figure 10.13 shows the inductor current and output voltage waveforms. As can be seen, the inductor current is discontinuous, having an average output current of 0.5 A. The average output voltage is 5.05 V, which is in good agreement with the specifications.

As shown in Figure 10.14, the line regulation of the closed-loop converter is very good. The input voltage can change from 12 to 30 V and still can achieve the desired output voltage regulation of 5 V ± 5%. Figure 10.15 predicts that the load regulation of the closed-loop converter will degrade at a light loading, below 50 mA.

10.2.6 Experimental Results

This section summarizes the open-loop and closed-loop measurements taken on a laboratory prototype. Open-loop measurements such as the voltage

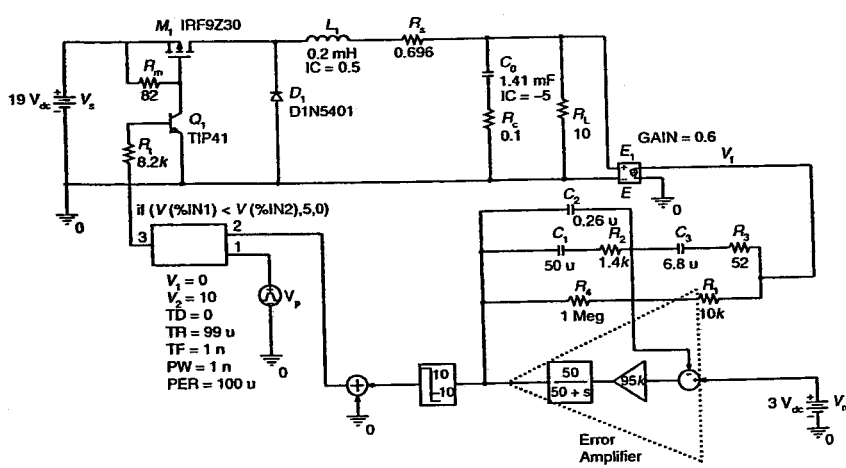

Figure 10.12 Closed-loop buck converter.

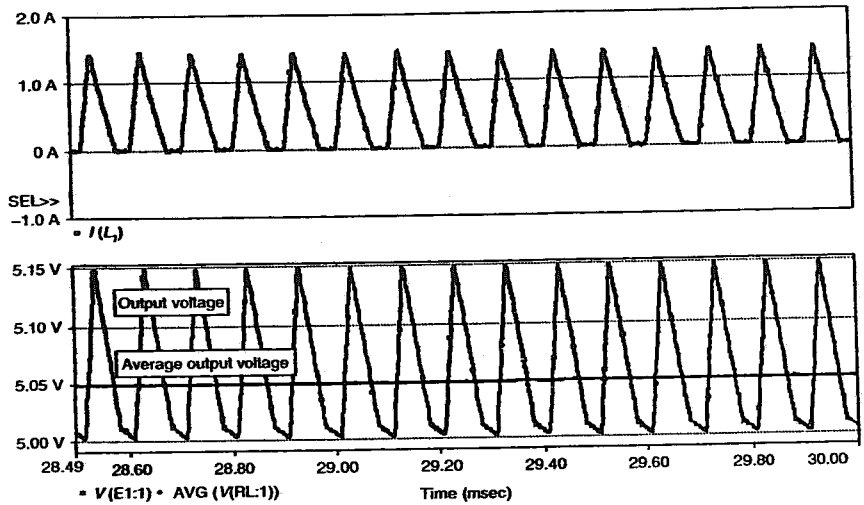

Figure 10.13 Current and voltage waveforms of the closed-loop buck converter.

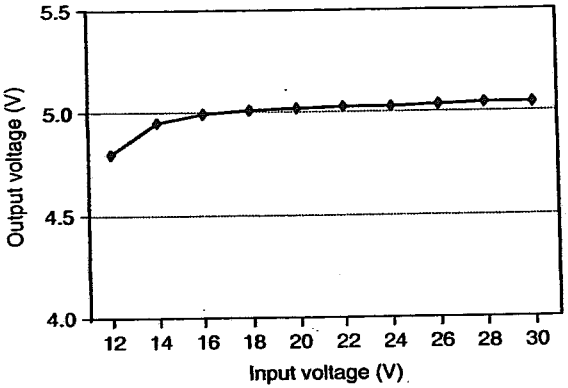

Figure 10.14 Line regulation of the closed-loop buck converter.

conversion ratio versus the duty cycle and the duty cycle versus the control voltage are important indications for the range of performance of the converter. The open-loop line and load regulations can be used to determine the performance of the converter by comparing them to their closed-loop counterparts.

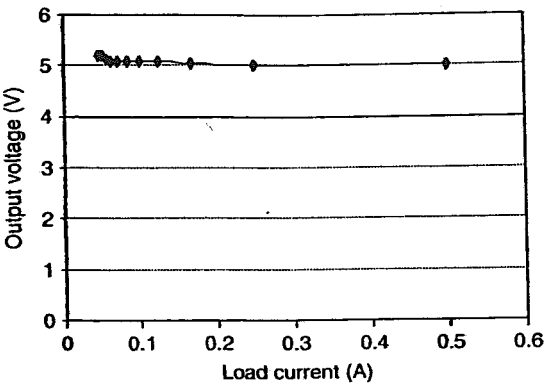

Figure 10.15 Load regulation of the closed-loop buck converter.

10.2.6.1 Open-Loop Experimental Data

The switching transistor was switched on and off by a variable duty cycle 5 V voltage pulse from a pulse generator. The measured duty cycle versus voltage conversion ratio of the open-loop converter is shown in Figure 10.16. The conversion ratio increases almost linearly with the duty cycle up to 31%. Due to circuit losses, the conversion ratio flattens for a duty cycle range between 31% and 37%; beyond this point, the conversion ratio decreases with an increasing duty cycle. From this plot, the usable range for the duty cycle is between 10% and 31%. Thus, the maximum closed-loop duty cycle should be limited to 31% to achieve good regulation. The nominal duty cycle ($D = 19.4\%$) is in the middle of the operating range.

10.2.6.2 Open-Loop Load Regulation

The load regulation for the open-loop buck converter under nominal duty cycle and constant average input voltage is shown in Figure 10.17. The output voltage changes almost linearly with the applied load, varying from 5 to 5.5 V for a load variation of 10 to 40 Ω. The open-loop line regulation, shown in Figure 10.18, reveals a linear variation of the output voltage with the input voltage, V_s.

The linearity of the TL594 PWM modulator was tested by injecting a variable DC voltage at the feedback input, using the test circuit given for parameter measurement in the TL594 data sheets [2]. The control voltage was varied and the duty cycle was measured at the output of the controller, yielding the PWM modulator gain plot of Figure 10.19. The duty cycle changes almost linearly with the input voltage.

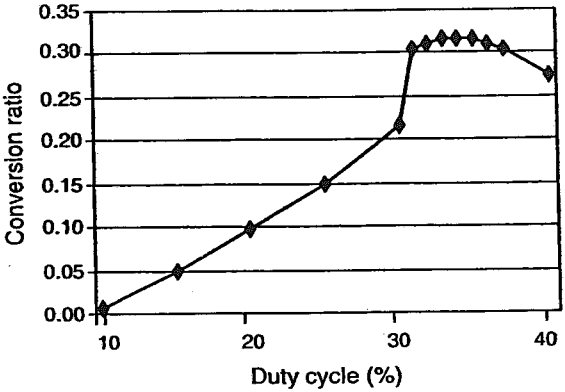

Figure 10.16 Voltage conversion ratio versus duty cycle of the open-loop buck converter at full load ($V_s = 19$ V, $I_a = 0.5$ A).

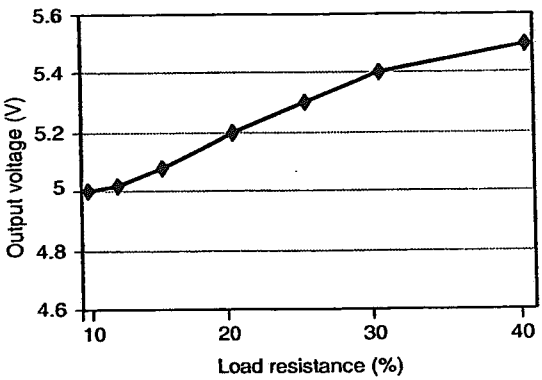

Figure 10.17 Open loop load regulation at duty cycle 26% and $V_s = 19$ V.

10.2.6.3 Bode Plot of the Loop Gain

The loop gain was measured by injecting a sine wave into the PWM modulator, in addition to the DC reference voltage, V_{ref}. The amplitude of the sine wave was kept small to satisfy the small signal variations in the duty cycle. A passive low-pass filter was connected at the output of the buck converter to filter out the high-frequency ripple from the output voltage. The experimental data corresponding to the loop gain using the low-pass filter is shown in Figure 10.20. To obtain the loop gain of the converter, the transfer function of the added low-pass filter (Figure 10.21) needs to be subtracted

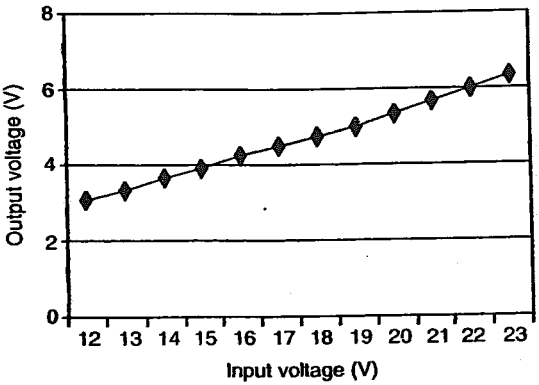

Figure 10.18 Open loop line regulation at duty cycle 26%.

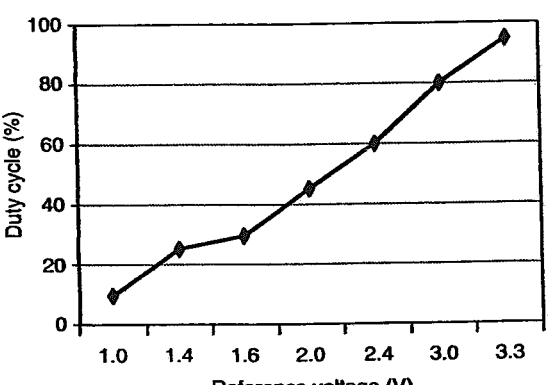

Figure 10.19 PWM modulator gain of the TL594 controller.

from the total response. Subtracting the low-pass filter response from the total response, the loop gain was obtained, as shown in Figure 10.22, which is very similar to the simulated data.

10.2.6.4 Closed-Loop Experimental Results

Figure 10.23 shows the output voltage, inductor current, and duty cycle waveforms of the TL594-based buck converter with a nominal input voltage of 19 V and a load current of 0.5 A, captured using a digital storage oscilloscope. Channel 3 displays the output voltage waveform. The average output voltage is 5 V with an output ripple voltage of 0.5 V. This is most likely due to

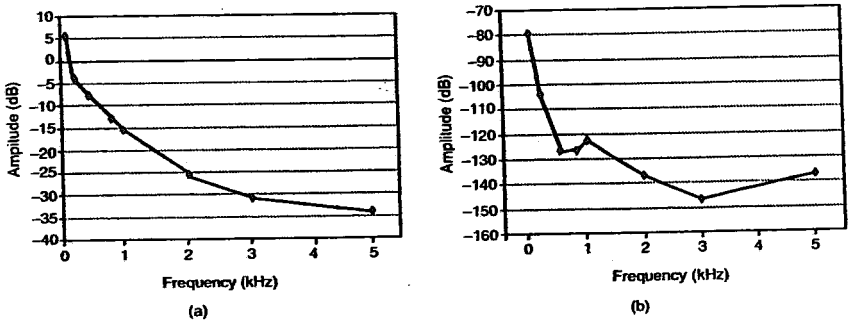

Figure 10.20 Bode plot of the loop gain including the low-pass filter: (a) amplitude of the loop-gain with low-pass filter; (b) phase response of the loop-gain with low-pass filter.

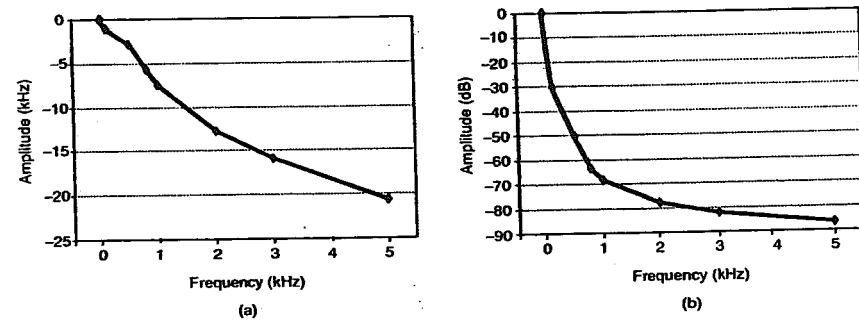

Figure 10.21 Frequency response of the low-pass filter: (a) amplitude of the low-pass filter; (b) phase response of the low-pass filter.

the equivalent series resistance associated with the output capacitor. Channel 2 displays the inductor current. It is obvious that the buck converter is operating in the discontinuous mode. Channel 1 shows the duty cycle output of the TL594 that drives the base of the switching transistor, TIP41. The switching frequency is measured to be 10 kHz with a duty cycle of 30%.

10.2.6.5 Closed-Loop Line and the Load Regulations

The line and load regulations were measured by sweeping the input voltage and output current, respectively. From Figure 10.24, it is clear that the closed-loop converter has a much better line regulation than its open-loop counterpart. For an input voltage range of 13.5 up to 30 V, the output voltage is between 4.77 and 5.15 V, which is within the 5% line regulation.

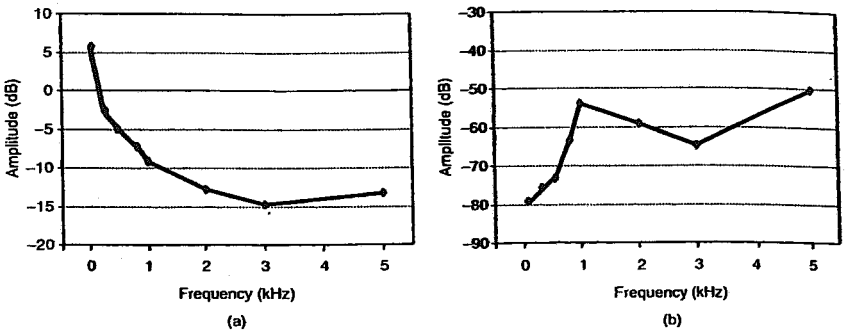

Figure 10.22 Bode plots of the loop-gain: (a) amplitude of the loop-gain without low-pass filter; (b) phase response of the loop-gain without low-pass filter.

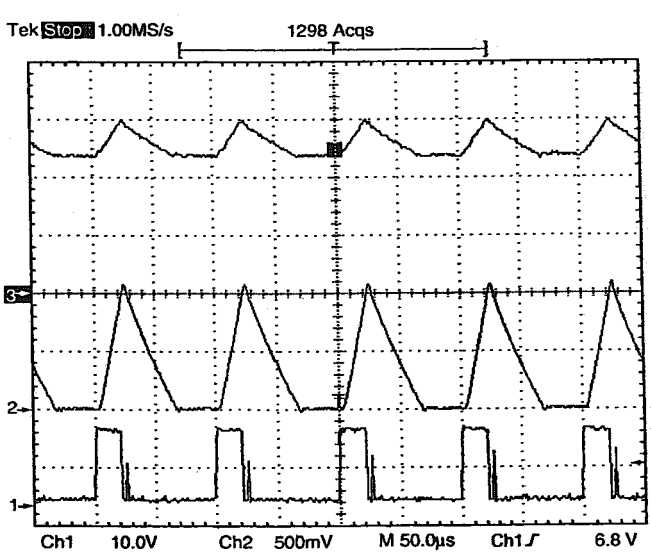

Figure 10.23 Output voltage, inductor current, and duty cycle from TL594.

The load regulation measured on the closed-loop buck converter, shown in Figure 10.25, is quite good. With output load current changes from 0.4 to 3 A, output voltages from 5.2 to 4.76 V were measured. Figure 10.26 shows the circuit schematic of the TL594-based buck converter. The internal 5-V reference voltage is used to obtain the 3-V reference, $+3V\_V_{ref}$, in combination with the resistor divider, $R_{a1} - R_{b1}$. Only error amplifier 1 is

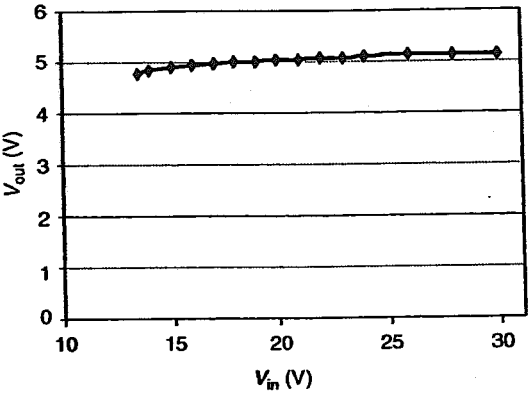

Figure 10.24 Experimental line regulation data.

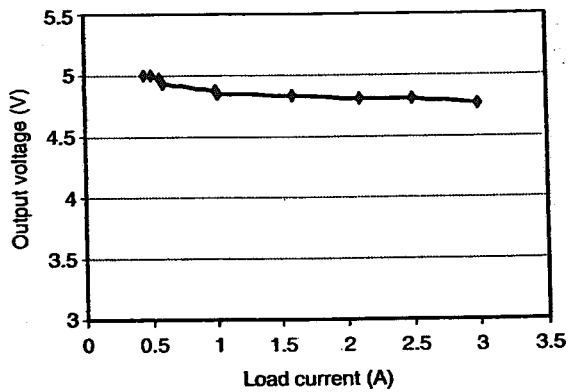

Figure 10.25 Experimental load regulation data.

used. The output of error amplifier 2 is saturated to a low voltage by connecting pin 15 to V_s and pin 16 to ground. This forces the internal diode connected in series with the output of error amplifier 2 to be reversed-biased; therefore, the control signal depends only on the output of the active error amplifier. If the two diodes at the outputs of the error amplifiers are reversed-biased by saturating both error amplifiers to a low level, pin 3 can be used to have a direct control of the duty cycle. This technique was used to measure some of the open-loop parameters, like the PWM modulator linearity, for instance.

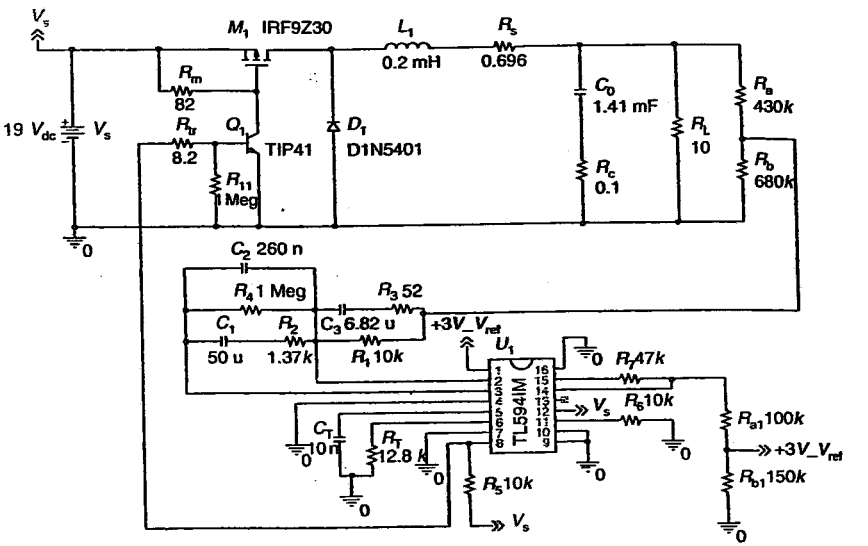

Figure 10.26 Schematic diagram of the TL594-based buck converter.

Figure 10.27 shows the output voltage and load current waveforms for the TL595-based buck converter during a load transient. The output current and output voltage of the buck converter change in response to a load variation. The current increases from 0.5 to 1 A, when the load resistor is decreased from 20 to 10 Ω. As can be seen, the output voltage drops to a lower steady-state level, according to the load regulation shown in Figure 10.25. The output ripple voltage does not show a significant change. The switching converter takes 4 ms to complete the transition.

10.3 DIGITAL CONTROL OF A VOLTAGE-MODE SYNCHRONOUS BUCK CONVERTER

This section discusses the design, simulations, and experimental results of a digital voltage-mode controller for a synchronous buck converter. First, the discrete-time model of the converter is derived from its continuous-time model. Additional dynamics are then added to achieve a zero steady-state output voltage error. Then, the closed-loop poles of the switching converter are chosen to satisfy a desired transient response using a state feedback technique. A synchronous buck converter was constructed to test the control algorithm. The feedback-gain vector L was calculated using MATLAB, and

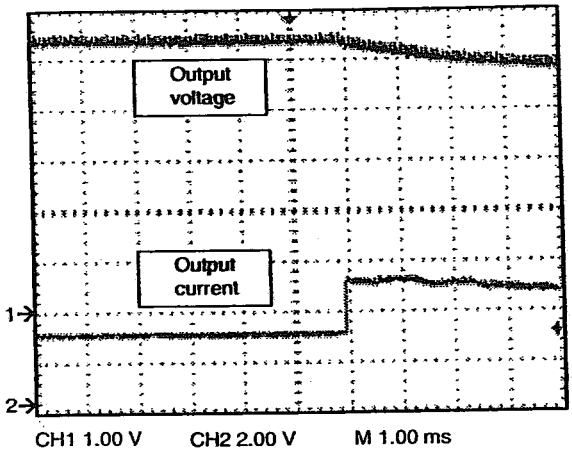

Figure 10.27 Output voltage and load current waveforms during a load transient.

Spice simulations were performed to verify the design. Finally, the control algorithm was programmed into a Texas Instruments' TI320F240 DSP that was used to drive the switching converter. It was found that the simulations and experimental results closely matched those from the experiments.

10.3.1 Circuit Parameters

The synchronous buck converter comprises of an output inductor of $L = 1.33\,\text{mH}$, an output capacitor of $C = 94\,\mu\text{F}$, a load resistor of $R = 4\,\Omega$, and two MOSFETS, with an ON resistance of $R_{on} = 0.8\,\Omega$. The combined resistance of the winding of the inductor and the current-sensing resistor is $R_L = 1.34\,\Omega$. The unregulated input DC voltage is $V_d = 7\,\text{V}$, and the regulated output voltage is $V_c = 3.3\,\text{V}$. The switching period was chosen as $T_s = 100\,\mu\text{s}$ for a switching frequency $f_s = 10\,\text{kHz}$. The amplitude of the sawtooth is set to 10 V. A steady-state duty cycle of $D = 72\%$ for the synchronous buck converter was found by open-loop measurements to yield a nominal output voltage of $V_o = 3.3\,\text{V}$. The steady-state duty cycle is larger than the ideal duty cycle of $D_i = (3.3\,\text{V}/7\,\text{V})100 = 47\%$ due to circuit losses. The continuous-time model was calculated using the above circuit parameters, resulting in:

$$A = \begin{bmatrix} -(R_{on} + R_L)/L & -1/L \\ 1/C & -1/(R^* C) \end{bmatrix} = \begin{bmatrix} -1609 & -752 \\ 10638 & -2660 \end{bmatrix}, \qquad (10.17)$$

$$B_1 = \begin{bmatrix} 1/L \\ 0 \end{bmatrix} = \begin{bmatrix} 752 \\ 0 \end{bmatrix}, \quad B_2 = \begin{bmatrix} 0 \\ 0 \end{bmatrix} \tag{10.18}$$

10.3.2 Closed-Loop Pole Selection

One way of choosing the closed-loop poles is to select the transfer function an nth-order low-pass Bessel filter, where n is the order of the system that is designed. In the present case, $n=3$ because an extended model with additional dynamics is used, the order of the system is increased from 2 to 3. The step response of a Bessel filter has no overshoot, thus it is suitable for a voltage regulator. The desired filter can then be selected for a step response that meets a specified settling time. The limit for the minimum settling time is that the control variable does not saturate. The closed-loop poles were chosen by using the following criteria: $n=3$, settling time <0.5 ms. Figure 10.28 shows the transient response of the low-pass Bessel filter. The settling time is nearly 0.4 ms without overshooting.

The magnitude component of the frequency response is displayed in Figure 10.29, where the corner frequency is 3 kHz. The S-plane location of the poles of the selected third-order Bessel filter is $P_s = \{-2.449\text{E}3 \pm j2.337\text{E}3, -3.093\text{E}3\}$. The desired closed-loop poles were mapped onto the Z plane by $p_z = e^{p_s T_s}$, resulting in $P_z = \{0.7615 \pm j0.1813, 0.7340\}$.

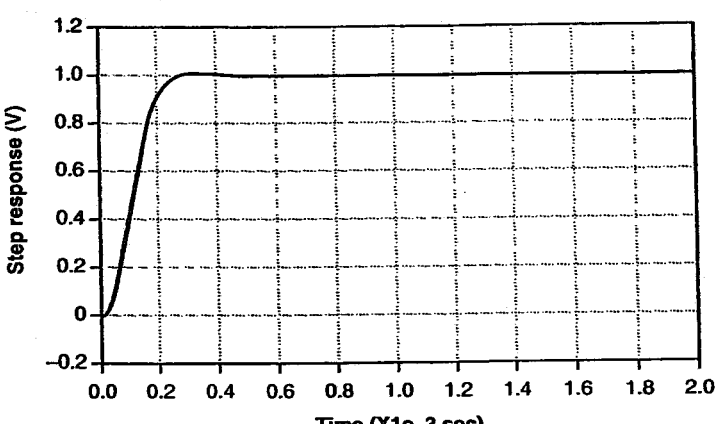

Figure 10.28 Step response of the third-order Bessel filter.

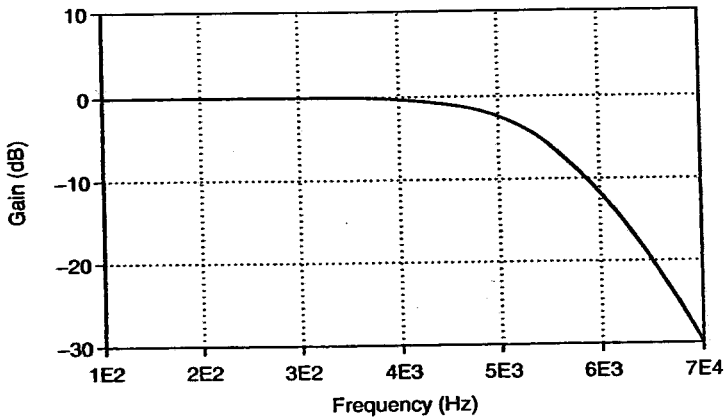

Figure 10.29 Frequency response of the third-order Bessel filter.

10.3.3 Discrete-Time Model

A small-signal discrete-time model for the voltage-mode synchronous buck converter was introduced in Chapter 6. The discrete-time model equation for a voltage-mode synchronous buck converter was found to be:

$$\hat{x}[(n+1)T_s] = \Phi_{VM}\hat{x}[nT_s] + \Gamma\frac{D}{V_{ref}}\hat{v}_{ref}. \tag{10.19}$$

The numerical expressions for the model components are:

$$\Phi_{VM} = e^{AT_s} = \begin{bmatrix} 0.8187 & -0.0600 \\ 0.8484 & 0.7349 \end{bmatrix}, \tag{10.20}$$

$$K = (B_1 - B_2)U = 5263.2, \tag{10.21}$$

$$\Gamma = e^{A(1-D)T_s}KT_s = \begin{bmatrix} 0.5016 \\ 0.1475 \end{bmatrix}, \tag{10.22}$$

$$\frac{D}{V_{ref}} = \frac{0.72}{3.3\,V} = 0.1818\frac{1}{V}. \tag{10.23}$$

Then, the numerical expression for Equation (10.19) becomes

$$\hat{x}[(n+1)T_s] = \begin{bmatrix} 0.8187 & -0.0600 \\ 0.8484 & 0.7349 \end{bmatrix} \hat{x}[nT_s] + \begin{bmatrix} 0.1094 \\ 0.0322 \end{bmatrix} \hat{v}_{ref}. \tag{10.24}$$

If full-state feedback is applied and the system is controllable, then the closed-loop poles can be arbitrarily placed to obtain a desired transient response. The voltage regulator should have the ability to track the reference voltage even under load variations. Thus, additional dynamics are added. The additional dynamics, represented by Φ_a, Γ_a, L_2, can be obtained by defining a composite state vector:

$$x_d[k] = \begin{bmatrix} i_L[k] \\ v_c[k] \\ x_a[k] \end{bmatrix}, \tag{10.25}$$

where x_a is the state vector of the added dynamics. Then, using the formula for the cascade connection of two state–space systems, the state–space description of the design plant is

$$\Phi_d = \begin{bmatrix} \Phi_{VM} & 0 \\ \Gamma_a c & \Phi_a \end{bmatrix}, \Gamma_d = \begin{bmatrix} \Gamma \\ 0 \end{bmatrix}, \tag{10.26}$$

where c relates the output to the states through $y = cx$.

A regulator for (Φ_d, Γ_d) can be designed and the vector of feedback gains can be partitioned as

$$L = [L_1 \; L_2], \tag{10.27}$$

where L_1 consists of the first n elements of L, n being the order of the system to be controlled (for a synchronous buck converter $n = 2$). L_2 is the remainder of L that relates the output to the states through $y_a = L_2 x_a$. L can be found by pole placement of the desired closed-loop poles of the regulator. The main advantage of this configuration is that if the actual closed-loop system is stable, the actual system will track the reference input with a zero steady-state error. For the present case,

$$c = [0 \quad 1] \tag{10.28}$$

and

$$\Phi_a = 1, \quad \Gamma_a = 1. \tag{10.29}$$

Refer to Vaccaro [3] for a detailed explanation on how to calculate Φ_a and Γ_a. Φ_d and Γ_d can be found to be:

$$\Phi_d = \begin{bmatrix} 0.8187 & -0.0600 & 0 \\ 0.8484 & 0.7349 & 0 \\ 0 & 1 & 1 \end{bmatrix}, \tag{10.30}$$

$$\Gamma_d = \begin{bmatrix} 0.1094 \\ 0.0322 \\ 0 \end{bmatrix}. \tag{10.31}$$

10.3.4 Feedback Gains

The values for the elements of the feedback vector L were obtained by pole placement, for the desired transient response. The resultant gain vector is:

$$L = [2.5925, 0.4027, 0.2420]. \tag{10.32}$$

The following MATLAB program was used to design the controller:

```
% Continuous time model for the synchronous buck converter
clear all
R=4;
L=1.33e-3;
C=94e-6;
Ron=0.8;
RL=1.34;
Ts=1.e-4;
Vg=7;
Vref=3.3;
A=[-(Ron+RL)/L -1/L
  1/C -1/(R*C)]
B1=[ 1/L
0 ]%during Ton
B2=[0
  0]%during Toff
% Discrete time model for the synchronous buck converter
fiVM=expm(A*Ts)
pol=eig(fiVM)
Un=Vg;
K=(B1-B2)*Un
D=0.72;
```

```
fiB = expm(A*(1-D)*Ts);% transition matrix for GamaA
GamaA = fiB*K*Ts
GamaB = GamaA*D/Vref
%tracking regulator
%
fiComp = 1;
GamaComp = 1;
c = [0 1];
fiDesign = [fiVM[0 0]'
GamaComp*c fiComp]
GamaDesign = [GamaB
  0]
% continuous-time closed-loop poles
Ps = [-2.449E3+2.337E3j-2.449E3-2.337E3j-3.093E3]
% discrete-time closed-loop poles
Pz = (exp(Ps*Ts))
% Calculate the Feedback gains
L = place(fiDesign,GamaDesign,Pz)
```

The program first calculates the continuous-time state–space matrices of the switching converter (i.e., A, B_1, and B_2). The discrete model is then calculated, based on the continuous model, yielding the discrete-time model matrices given in Equations (10.20) and (10.22). The extended model from Equation (10.26) is calculated after the comment %tracking regulator, yielding the numerical results shown in Equations (10.30) and (10.31). The desired continuous-time poles are loaded into the variable P_s and then mapped into the Z plane, obtaining P_Z. Finally, the feedback gain vector is calculated by pole placement.

10.3.5 Control Strategy

The control variable, v_{ref}, comprises of a steady-state term and a perturbation term:

$$v_{ref} = V_{ref} + \hat{v}_{ref}, \tag{10.33}$$

where v_{ref} is calculated at the beginning of the kth switching cycle as:

$$v_{ref}(k) = V_{ref}(k) - L_1\hat{x}(k) + y_a(k), \tag{10.34}$$

where

$$y_a(k) = L_2 x_a(k), \tag{10.35}$$

$$x_a(k) = \Phi_a x_a(k-1) + \Gamma_a u_a(k), \tag{10.36}$$

$$u_a(k) = V_{ref} - x_2(k). \tag{10.37}$$

10.3.6 Analog Model for PSpice Simulations

An interesting by-product of this digital control method is the analog implementation used in SPICE to test the algorithm. This analog version, shown in Figure 10.30, could be built into an integrated circuit to yield a very accurate regulator. The main drawback of the analog implementation is the need for sample and hold circuits. The inductor current, I_L, is sensed by the F1 block (a current to voltage converter), that produces an output voltage proportional to the inductor current, I_L. This current is sampled at t_{on}, the sampled value is held during one switching period at the output of the sample and hold circuit. The nominal value of the minimum value of the current through the inductor is subtracted from the sampled current to produce the state variable x_1, i.e., the small-signal perturbation of the inductor current at the sampling time. Then, x_1 is multiplied by the corresponding feedback gain, L_1.

The output voltage is also sampled at t_{on}, and the sample is held at the output of the sample and for an entire switching period. The reference voltage is subtracted from the voltage sample to produce the state variable x_2, i.e., the small-signal perturbation of the capacitor voltage at the sampling time. Then, x_2 is multiplied by the corresponding feedback gain, L_2. x_2 is also connected to the discrete compensator that produces the variable y_a. The state variables are added to y_a and the result of this operation is added to the nominal value of the control voltage, to determine the variations of the duty cycle.

The PSpice model for the sample and hold circuit is shown in Figure 10.31. C_1 is charged to the input voltage when the switch closes. When the switch opens, the voltage across the capacitor is held until the next sampling time. The E block acts as a voltage follower, providing impedance transformation. The discrete compensator, shown in Figure 10.32, calculates y_a according to Equations (10.29) to (10.35).

The MOSFET driver was designed as shown in Figure 10.33. A dead time of 100 ns is modeled with a delay block and logic gates. The E blocks provide the necessary voltage gain to boost the voltage of the 5-V logic to 15 V in order to drive the MOSFETs. E1 is the upper MOSFET driver that develops a differential output voltage. "outHi" connects to the gate and "outHiL" connects to the source, while "outLo" connects to the gate of the lower MOSFET.

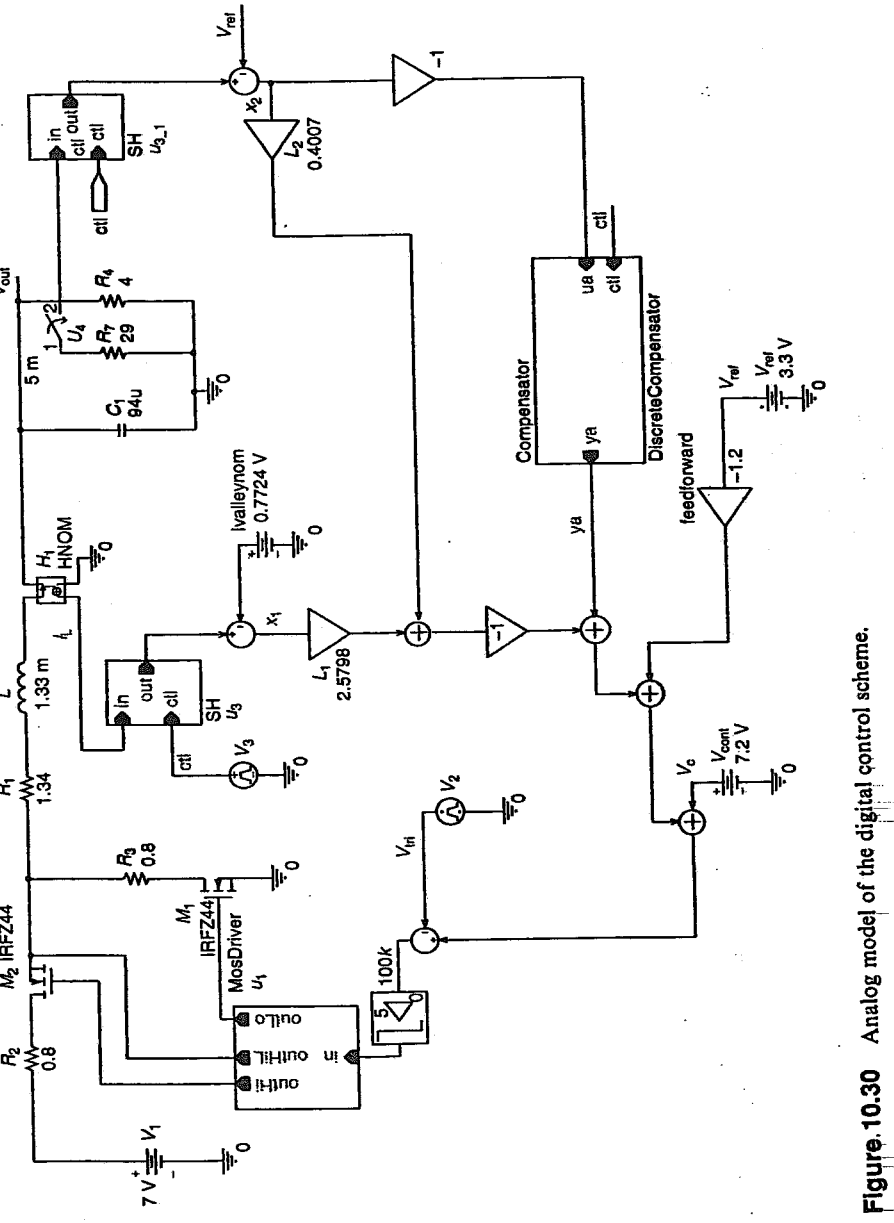

Figure 10.30 Analog model of the digital control scheme.

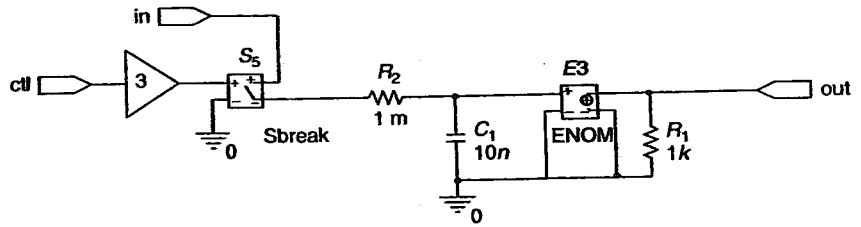

Figure 10.31 Sample and hold.

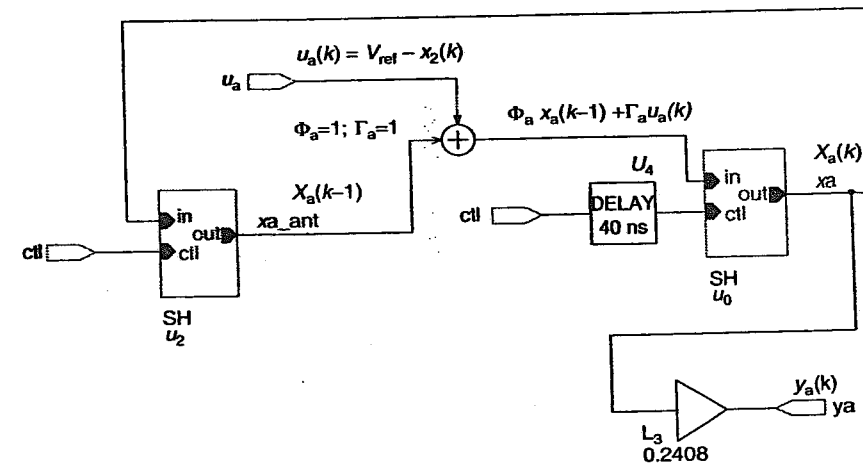

Figure 10.32 Discrete compensator.

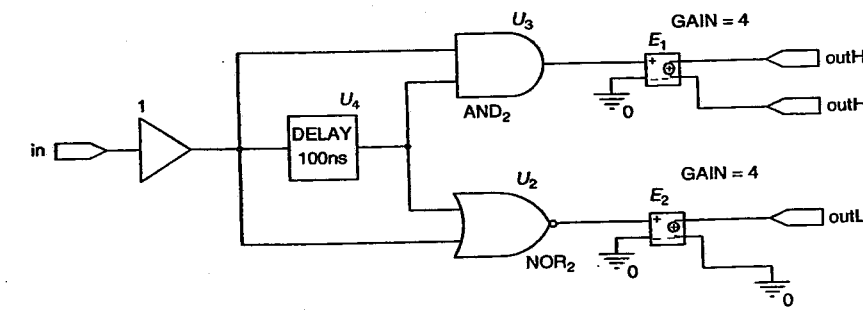

Figure 10.33 MOSFET driver.

10.3.7 Simulation Results

Simulations were performed using SPICE and MATLAB to verify the design. Figure 10.34 displays the result of a parametric simulation where the load resistor was set to 4 and 8 Ω, respectively. The output voltage converges to the nominal voltage of 3.3 V due to the tracking effect included in the additional dynamics. Notice that no overshoot is present during the start-up for $R = 4\,\Omega$. A feedforward gain (empirically adjusted to −1.2) was added to improve the start-up transient. Figure 10.35 shows a magnified view of the inductor current waveforms corresponding to the two selected load resistors. The current reaches different steady-state values according to the load resistance.

Notice that the waveforms repeat every 100 μs without subharmonic oscillations and that the duty cycle changes to maintain the output voltage under different loading conditions. The transient response due to a load change from 4 to 3.48 Ω at 5 ms is shown in Figure 10.36. Observe that after the initial transient, the output voltage returns to the nominal value with a zero steady-state error. In conclusion, the simulations show that the voltage-mode regulator is able to track the reference voltage with zero steady-state error.

10.3.8 Sensitivity of the Closed-Loop Poles Due to Load Variations

The load resistance was changed in MATLAB simulations to test the sensitivity of the closed-loop poles of the discrete-time model due to load variations.

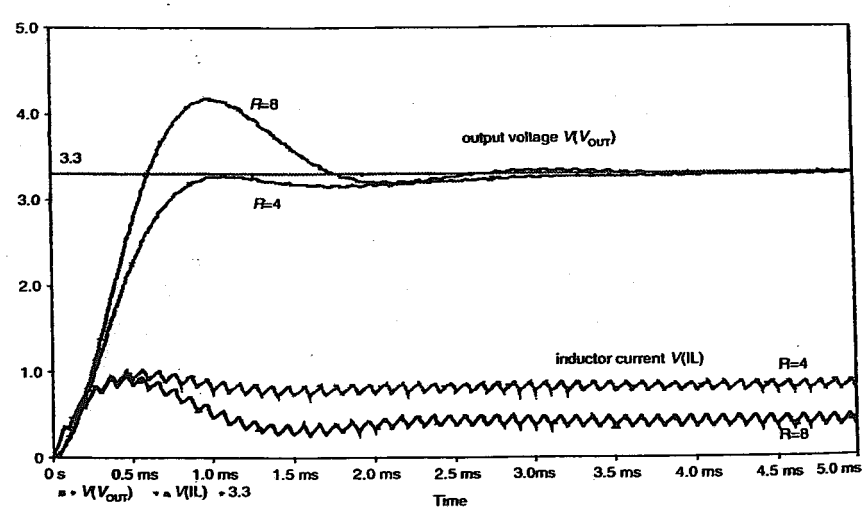

Figure 10.34 Parametric simulation with different loading.

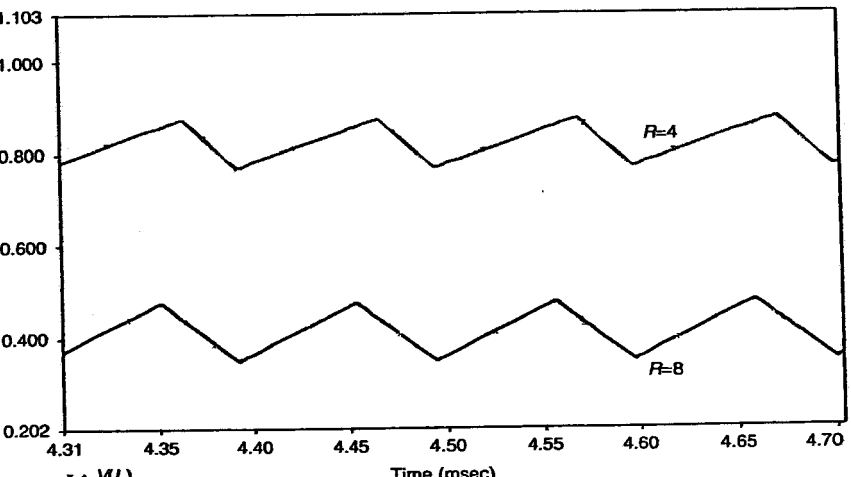

Figure 10.35 Inductor current for different loading.

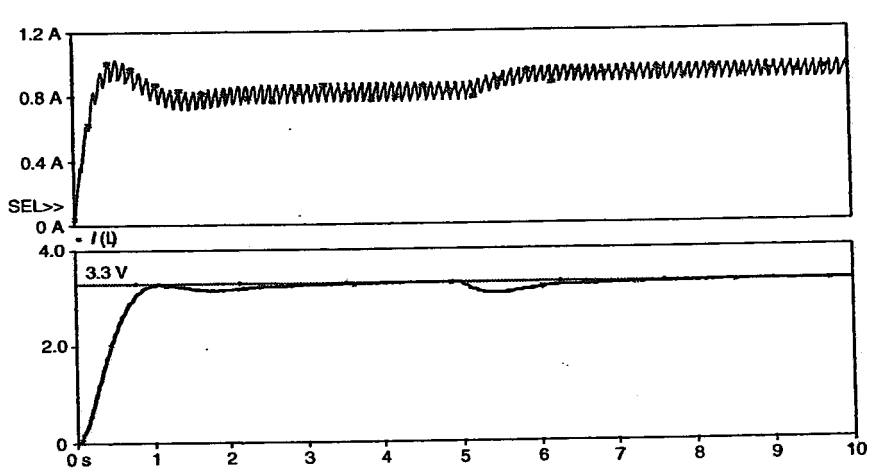

Figure 10.36 Transient response due to a load change at time = 5 msec.

The feedback gains were calculated to set the closed-loop poles at: $poles = \{0.7615 \pm j0.1813, 0.7340\}$ for a nominal load resistance of $4\,\Omega$. Without changing the feedback gains, the load was varied and the poles were recalculated. Figure 10.37 displays the pole locations for a load variation

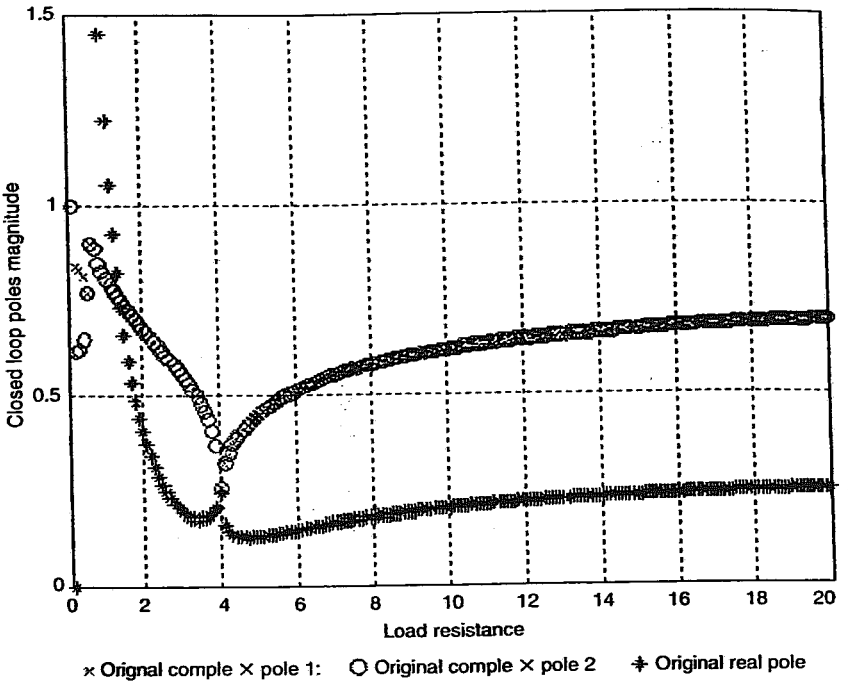

Figure 10.37 Closed-loop pole dependency versus load resistance.

from 0.1 to 20 Ω. Notice that the system remains stable at a load resistance from 0.7 to 20 Ω. For a load resistance smaller than 0.7 Ω, one of the poles moves outside the unit circle. At this load value, the voltage-mode synchronous buck converter becomes unstable. For the nominal resistor value, the poles are located at $\{0.7615 \pm j0.1813, 0.7340\}$. Finally, for a load resistance greater than 4 Ω, the system is always stable and the pole locations do not change significantly.

10.3.9 Experimental Results

The control algorithm was implemented in a Texas Instruments' TI320F240 DSP to drive the converter circuit. The internal PWM circuitry was set to emulate the external sawtooth and turn off the switch when the PWM counter reaches the value determined by v_{ref}. An internal timer was set to 100 μs. The analog-to-digital converter (ADC) is activated for each period, during which the inductor current and the output voltage are sampled. The

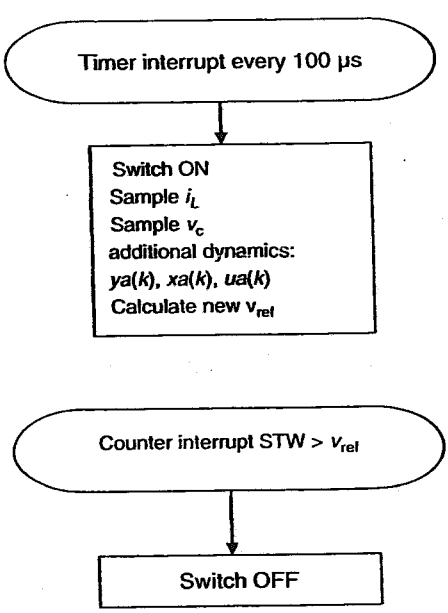

Figure 10.38 Block diagram of the algorithm implemented in the DSP.

end of the conversion activates an ADC interrupt, where a new v_{ref} value is calculated. The block diagrams of the interrupts are shown in Figure 10.38.

Figure 10.39 displays the steady-state waveforms obtained under a nominal load condition. The trace on *ch*2 is the v_{ref} used as the control variable, *ch*1 shows the inductor current, and *ch*3 is the output voltage. Notice that the duty cycle is actually 72% and the switching period is fixed at 100 μs. The transient response of the DSP-controlled synchronous buck converter under a small load variation is shown in Figure 10.40. It can be seen that when the load changes to a smaller resistance (i.e., 3.75 Ω), v_{ref} adjusts the duty cycle to a new value, leading to a new steady-state duty cycle of nearly 90%.

10.4 DIGITAL CONTROL OF A CURRENT-MODE SYNCHRONOUS BUCK CONVERTER

In Section 10.3, we discussed the design of a DSP-based voltage-mode synchronous buck converter. The same hardware is also used, without modifications, to implement a current-mode synchronous buck converter. This is accomplished by changing the DSP software. This section discusses the design and experimental results obtained from the current-mode synchronous buck converter.

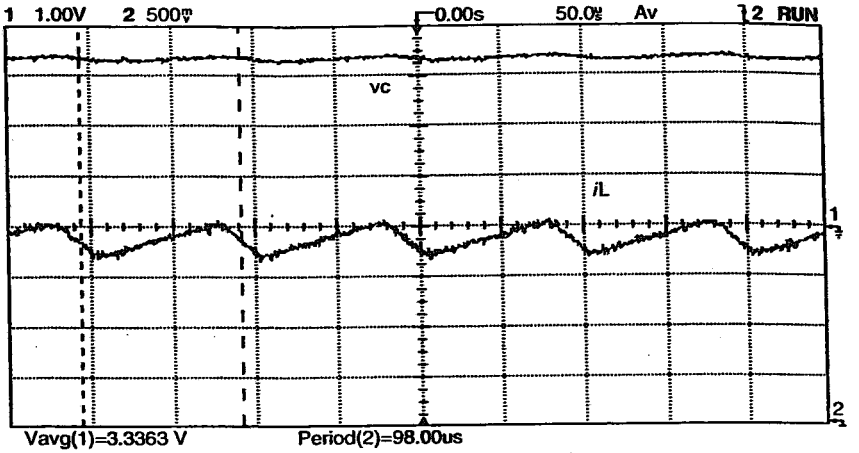

Figure 10.39 Steady-state response of the DSP-controlled VM synchronous buck converter.

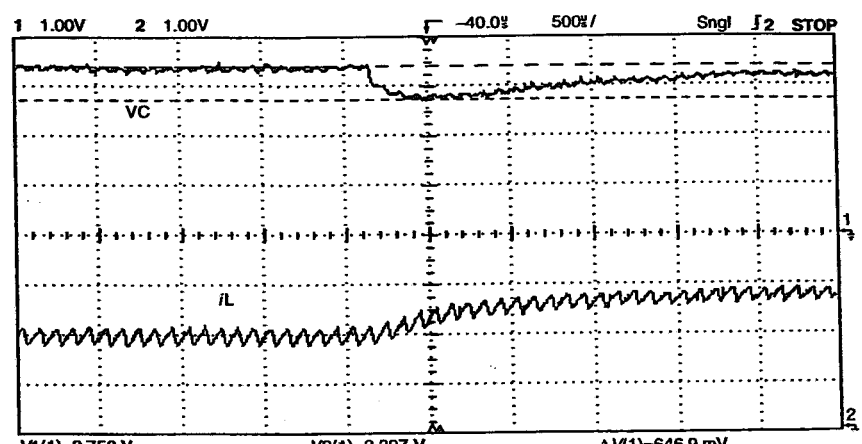

Figure 10.40 Transient response of the DSP-controlled synchronous buck converter under load variation.

10.4.1 Continuous-Time State Model

The continuous-time model for the synchronous buck converter is the same as in Equations (10.17) and (10.18). For an open loop converter,

$$A = \begin{bmatrix} -(R_{on} + R_L)/L & -1/L \\ 1/C & -1/(R^* C) \end{bmatrix} = \begin{bmatrix} -1609 & -752 \\ 10638 & -2660 \end{bmatrix}, \tag{10.38}$$

$$B_1 = \begin{bmatrix} 1/L \\ 0 \end{bmatrix} = \begin{bmatrix} 752 \\ 0 \end{bmatrix}, \quad B_2 = \begin{bmatrix} 0 \\ 0 \end{bmatrix}. \tag{10.39}$$

10.4.2 Obtaining the Discrete-Time Model

The discrete-time model for the current-mode switching converter was calculated in Chapter 6 as

$$\hat{x}[(n+1)T_s] = \Phi_{CM}\hat{x}[nT_s] + \Gamma\omega_3\hat{I}_p, \tag{10.40}$$

where the expression for the model components and their numerical values are:

$$\Phi_{CM} = \Phi + \Gamma\Omega = \begin{bmatrix} -1.7525 & 0.0799 \\ 0.0921 & 0.7761 \end{bmatrix}, \tag{10.41}$$

$$\Gamma_{CM} = \Gamma\omega_3 = \begin{bmatrix} 3.4507 \\ 1.0019 \end{bmatrix}, \tag{10.42}$$

$$\Phi = \Phi_{VM} = e^{AT_s} = \begin{bmatrix} 0.8187 & -0.0600 \\ 0.8484 & 0.7349 \end{bmatrix}, \tag{10.43}$$

$$K = (B_1 - B_2)U = 5263.2, \tag{10.44}$$

$$\Gamma = e^{A(1-D)T_s} KT_s = \begin{bmatrix} 0.5016 \\ 0.1475 \end{bmatrix}, \tag{10.45}$$

$$\Omega = [\omega_1 \quad \omega_2], \tag{10.46}$$

$$\omega_1 = \frac{\partial d_n}{\partial x_1} = \frac{\hat{d}_n}{\hat{i}_L} = -\frac{L}{(V_d - V_c)T_s} = -6.3748, \tag{10.47}$$

$$\omega_2 = \frac{\partial d_n}{\partial x_2} = \frac{\hat{d}_n}{\hat{v}_c} = \left[\frac{D}{V_d - V_c}\right] = 0.3385, \tag{10.48}$$

$$\omega_3 = \frac{\partial \hat{d}_n}{\partial I_p} = \frac{\hat{d}_n}{\hat{I}_p} = \frac{1}{T_s}\frac{L}{V_d - V_c} = 6.3748. \tag{10.49}$$

10.4.3 Current-Mode Instability

The poles of the transition matrix in current-mode, Φ_{CM}, were found from Equation (10.41) at $\{-2.3776, 0.7815\}$. Clearly, one pole lies outside the unit circle, predicting an unstable behavior for $D = 0.72$. The design technique used in this example permits the closed-loop poles to be located in any desired location, overcoming this problem. The practical limitation for choosing the closed-loop poles is that the control variable should not saturate.

10.4.4 Extended-State Model for a Tracking Regulator

Additional dynamics, represented by Φ_a, Γ_a, L_2, are added to yield a zero steady-state error. The extended-state model for a tracking regulator with additional dynamics implementing a digital tracking system that uses full-state feedback is given in Equation (10.50)

$$\Phi_d = \begin{bmatrix} \Phi_{CM} & 0 \\ \Gamma_a c & \Phi_a \end{bmatrix}, \quad \Gamma_d = \begin{bmatrix} \Gamma \\ 0 \end{bmatrix}, \tag{10.50}$$

where c relates the output to the states through $y = cx$; L_2 relates the output of the additional block to its states through $y_a = L_2 x_a$. x_a is the state vector of the added dynamics. In this example, only one state is added. A regulator for (Φ_d, Γ_d) can be designed and the vector of feedback gains can be partitioned as

$$L = [L_1 \quad L_2], \tag{10.51}$$

where L_1 consists of the first n elements of L, n being the order of the system to be controlled (for a synchronous buck converter $n = 2$). L_2 is the remainder of L. L can be found by pole placement of the desired closed-loop poles of the regulator. The procedure to find (Φ_a, Γ_a) is covered in detail in Vaccaro [3], but for this case $\Phi_a = \Gamma_a = 1$.

The extended model for the current-mode synchronous buck converter becomes

$$\Phi_d = \begin{bmatrix} -2.3804 & 0.1099 & 0 \\ -0.0805 & 0.7843 & 0 \\ 0 & 1 & 1 \end{bmatrix}, \tag{10.52}$$

$$\Gamma_d = \begin{bmatrix} 3.4507 \\ 1.0019 \\ 0 \end{bmatrix}. \tag{10.53}$$

10.4.5 Feedback Gains

The values for the elements of the feedback vector L were obtained by pole placement for an arbitrary desired transient response. The closed-loop poles were arbitrarily chosen to lie in the following locations of the Z plane: $\{-0.66, 0.66, 0.9\}$

The resulting gain vector is:

$$L = [-0.4709 \quad 0.1340 \quad 0.0183]. \tag{10.54}$$

10.4.5.1 MATLAB Design File

The MATLAB command file used to design the current-mode controller is:

```
clear all
Rs = 0.8; %Ron
RD = Rs;
RL = 1.34;
R = 4;
L = 1.3302e-3;
cap = 94.e-6;
Ts = 1.e-4;
Vg = 7;
Vref = 3.3;
Vd = 0.0; % diode voltage drop
IM = Vref/R
D = (Vref+Vd+IM*(RL+RD) )/(Vg+Vd)% duty cycle with losses
Vdrop = Vg-IM*(Rs+RL)-Vref
deltaI = (Vdrop*D*Ts)/L
Ivalle = IM-deltaI/2
Ipnom = IM+deltaI/2;
A = [-(Rs+RL)/L -1/L
   1/cap -1/(R*cap)]
fiA = expm(A*Ts)
fiA;
pol = eig(fiA)
B1 = [1/L
   0] %during Ton
B2 = [0
   0 ];%during Toff
Un = Vg; %input vector
%discrete model
K = (B1-B2)*Un
fiB = expm(A*(1-D)* Ts)% transition matrix for GamaA
GamaA = fiB*K*Ts
```

```
%sensitivities
fiD = expm(A*D*Ts);
deltafiD = A*fiD;
deltaGamaD = fiD*B1;
x10 = IM-deltal/2; %Ivalle nominal
x20 = Vref; %Vc nominal
w1 = -fiD(1,1)/((deltafiD(1,1)*x10+deltafiD(1,2)*x20+deltaGamaD
  (1,:)*Un)*Ts);
w2 = -fiD(1,2)/((deltafiD(1,1)*x10+deltafiD(1,2)*x20+deltaGamaD
  (1,:)*Un)*Ts);
Omega = [w1 w2] %vector sensitivities
% sensitivities alternative
Omegaalt = [-L/(Vdrop*Ts) D/Vdrop 0 0]
%w1 = -L/(Vdrop*Ts);
%w2 = D/Vdrop;
GamaB = (L/(Vdrop*Ts) )*GamaA
% current mode
fiCM = fiA+GamaA*Omega
GamaCM = GamaB
cCM = eye(2);
dCM = zeros(2,1);
pcm = eig(fiCM)
% closed loop without compensator
% complete state feedback
% closed loop poles
P = [-0.6626 0.857]'
F = place(fiCM,GamaB,P)
fiCL = fiCM-GamaB*F;
pcl = eig(fiCL)
% closed loop with compensator
% compensator design
fiComp = 1;
  GamaComp = 1;
c = [0 1];
fiDesign = [fiCM [0 0]'
  GamaComp*c fiComp];
GamaDesign = [GamaCM
  0];
P = [-0.6626 0.657 0.90]' % closed loop poles as tracking_regulator
Ld = place(fiDesign,GamaDesign,P)
fiCL = fiDesign-GamaDesign*Ld;
pcl = eig(fiCL)
```

10.4.6 Control Strategy

The same control strategy used for the voltage-mode synchronous buck converter was used here, except that the control variable is the peak current flowing through the inductor I_p. Like the others, this variable comprises of a steady-state term and a perturbation term. Then, we can write:

$$I_p = \bar{I}_p + \hat{I}_p, \tag{10.55}$$

where I_p is calculated at the beginning of the kth switching cycle as

$$I_p(k) = \bar{I}_p(k) - L_1\hat{x}(k) + y_a(k), \tag{10.56}$$

where

$$y_a(k) = L_2 x_a(k), \tag{10.57}$$

$$x_a(k) = \Phi_a x_a(k-1) + \Gamma_a u_a(k), \tag{10.58}$$

$$u_a(k) = V_{ref} - x_2(k). \tag{10.59}$$

10.4.7 Simulation Results

Simulations were performed in SPICE to verify the design. The PSpice schematic of the test circuit is shown in Figure 10.41. Figure 10.42 displays the result of a load transient simulation where the load resistance was changed from 4 to 3.75 Ω and back again to its original value. The smaller value of 3.75 Ω was selected because it is very close to make the switching converter unstable by driving one of the closed-loop poles outside the unit circle. The output voltage converges to the nominal voltage of 3.3 V due to the tracking effect included in the additional dynamics. Notice that no overshoot in the voltage waveform is present during the start-up. A feed-forward gain (empirically chosen as −0.1) was added to improve the start-up transient. Figure 10.42 also shows the inductor current waveforms corresponding to the two selected load resistors. The current reaches different steady-state values, according to the load resistance. The signal I_hold represents the samples of the inductor current taken at the turn on of the main switch. Notice that the waveforms repeat every 100 μs without any sub-harmonic oscillation. Also notice that the duty cycle for $R = 4\,\Omega$ is 72%. In conclusion, the simulations show that the current-mode regulator is able to track the reference voltage while showing a stable behavior for a duty cycle greater than 50%.

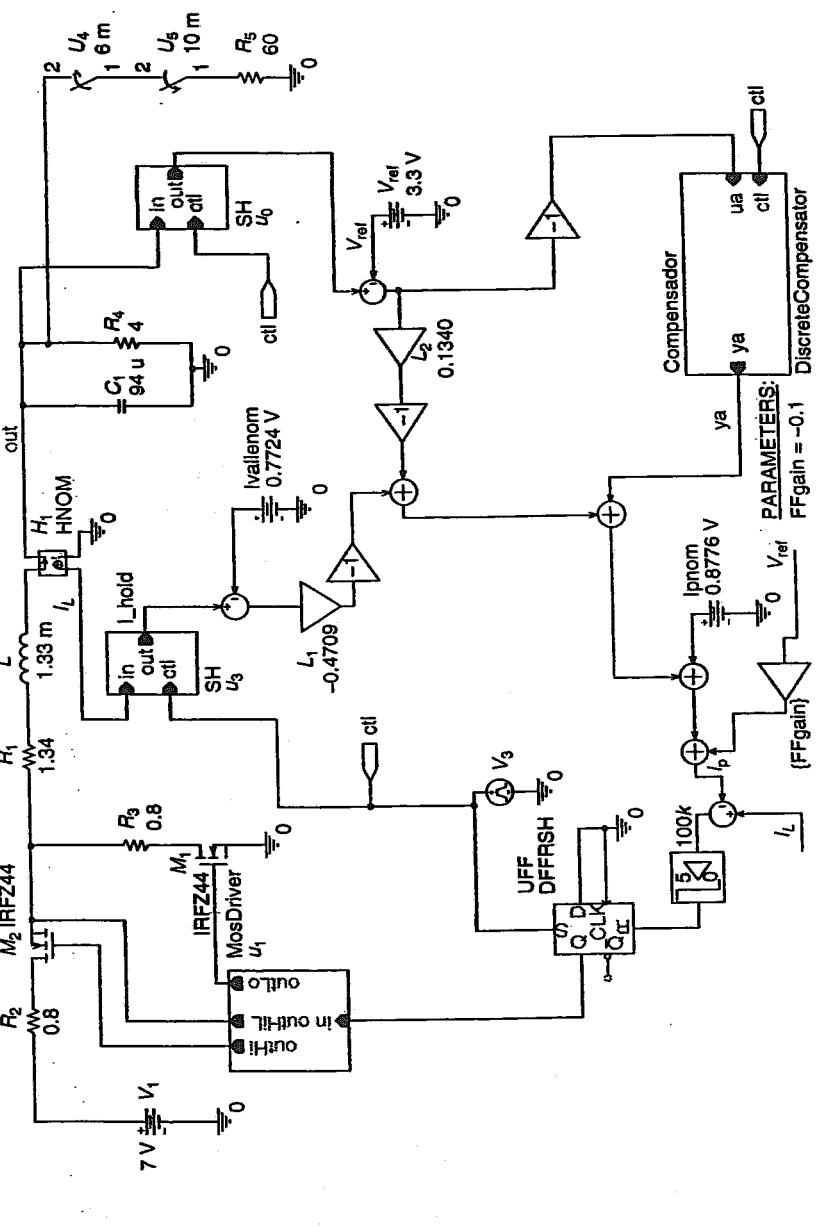

Figure 10.41 PSpice model of the current-mode synchronous buck converter.

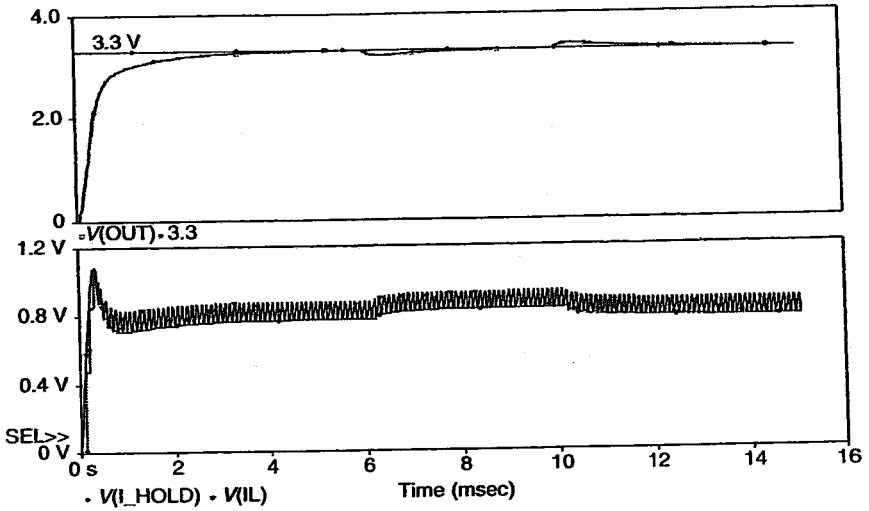

Figure 10.42 PSpice simulation of a load transient.

10.4.8 Sensitivity of the Closed-Loop Poles Due to Load Variations

The load resistance was changed to test the sensitivity of the closed-loop poles due to load variations. The feedback gains were calculated to set the closed-loop poles at: {0.66, − 0.66, 0.9} for a nominal load resistance of 4 Ω. The resulting feedback gains are: $L = [-0.4709, 0.1340, 0.0183]$. Then the load was changed and the poles were recalculated. Figure 10.43 displays the pole locations for a load resistance change from 0.1 to 20 Ω. Notice that the system remains stable at load resistances from 3.4 to 20 Ω. For a load resistance smaller than 3.4 Ω, one of the poles moves outside the unit circle. At this load resistance value, the synchronous buck converter becomes unstable. For the nominal resistor value, the poles are located at {0.66, −0.66, 0.9}. Finally, for a load resistance value greater than 4 Ω, the system is always stable.

10.4.9 Experimental Results

The control algorithm was programmed into a Texas Instruments' TI320F240 DSP to drive the converter. An external voltage comparator was used to trigger an external interrupt when the inductor current reaches the value determined by I_p. An internal timer was set to 100 μs. At each timer period, the ADC is activated, and the inductor current and the output

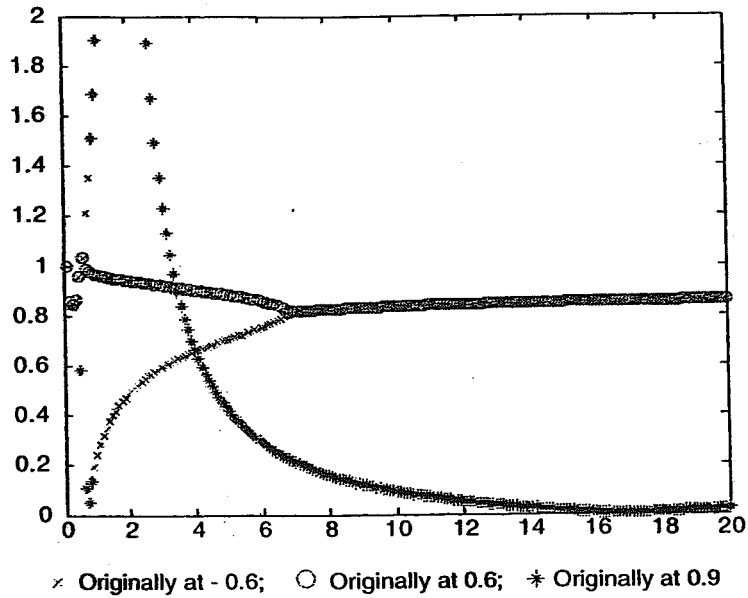

Figure 10.43 Magnitude of the closed-loop poles versus load resistance.

voltage are sampled. The end of conversion activates an ADC interrupt, when a new I_p value is calculated. The block diagrams of the interrupts are shown in Figure 10.44.

Figure 10.45 displays the steady-state waveforms obtained under a nominal load condition. The trace on *ch*2 is the I_p used as the control variable, *ch*1 shows the inductor current and *ch*3 is the output voltage. Notice that the duty cycle is actually 72% and the switching period is fixed at 100 μs, without any suboscillations. This proves that the closed-loop system is stable as predicted.

The transient response of the DSP-controlled synchronous buck converter under a small load perturbation is shown in Figure 10.46. It can be seen that when the load resistance changes to a smaller value (i.e., 3.75 Ω), I_p adjusts the duty cycle to a new value, leading to a new steady-state duty cycle of nearly 90%. Even under this condition, the converter remains stable.

10.4.10 DSP Program

The complete listing of the main TMS320C-240 DSP program is shown below. After completing all the initializations, the main program goes into

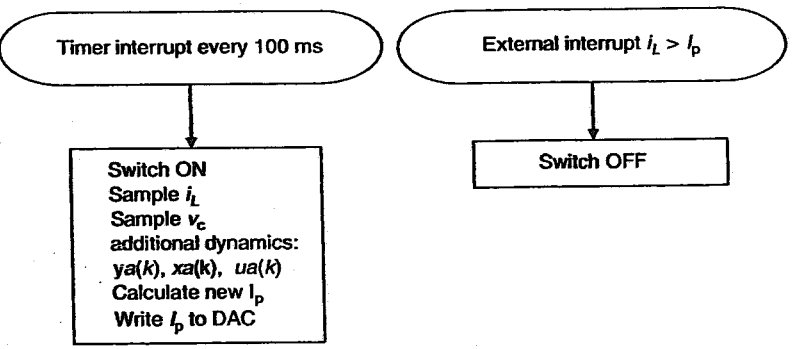

Figure 10.44 Flow diagram of the interrupt routines.

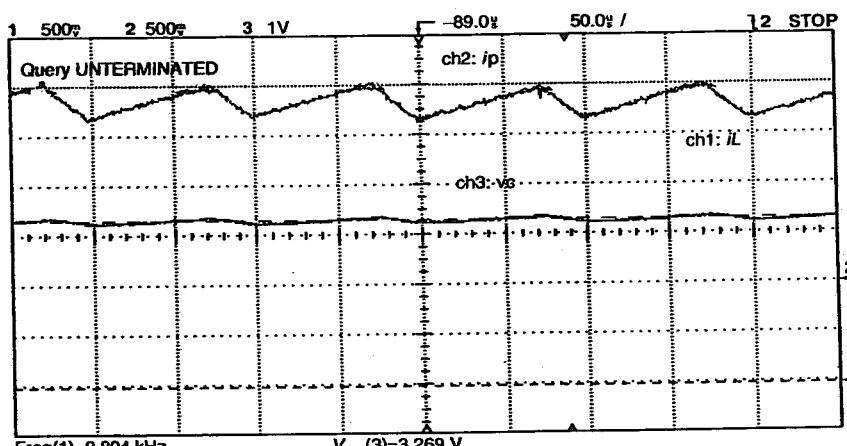

Figure 10.45 Steady-state waveforms of the current-mode synchronous buck converter.

an infinite loop, waiting for the interrupts to occur. Once the external interrupt is triggered when the inductor current reaches the programmed peak value, the main switch is switched off. The second interrupt is activated by the internal timer at every switching period. The inductor current and the output voltage are sampled and the main switch is switched on. The control algorithm calculates the additional dynamics and the new value for the inductor's peak current is calculated.

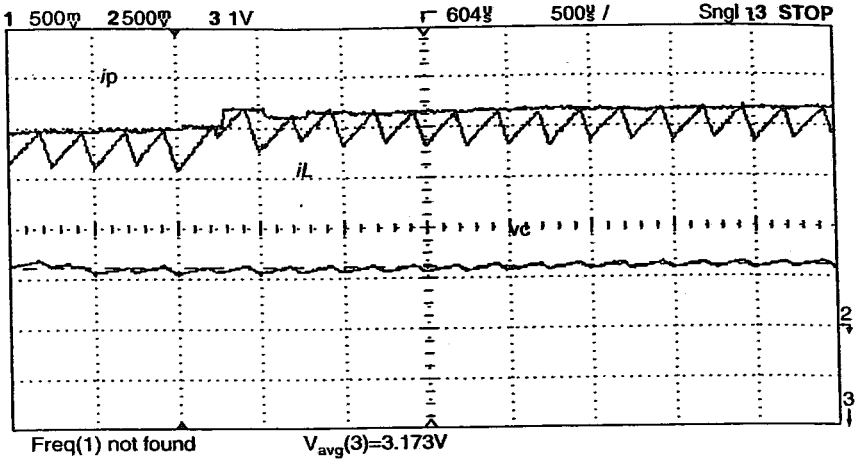

Figure 10.46 Transient response of the current-mode synchronous buck converter under a load step.

```
#include "Perip240.h"
#include "Inter240.h"
#include "Reg_C.h"
/* constants */
/*
*ADC gains:
*   ch2(pin 5) for IL and ch10(pin 13) for Vc

*   Ianalog          ADC hexa     ADC dec     Amplifier output
*   A                0×3FF        1023        5V
*   1A               412          2.187V
*
*                    IanalogMax = 620mA
*
*   Vanalog          ADC hexa     ADC dec     Amplifier output
*   5V               0×1FB        507
*
*
*/
#define ADCgain      (2.075/418)  /* ADC gain (DAC_input_volt
                                     age/ADC_count) */
```

```
#define Ki_F          (1.0/412)      /* 0.43/0×2B3 multiply DAC
                                        reading by Ki to obtain the
                                        current value */
#define Kv_F          (5.0/0×1FB)    /* multiply DAC reading by Kv to
                                        obtain the voltage value */
#define DAC_1v25      0×03FF         /* DAC value for 1.25 V output */
#define DAC_2v5       0×07FF         /* DAC value for 2.5 V output */
#define DAC_3v75      0×0BFF         /* DAC value for 1.25 V output */
#define DAC_GAIN
  _F
                      (1023/1.25)    /* new dac value = DAC_GAIN *
                                        volts */
#define I2
  DAC_F               (2.187*
                      1023/1.25)     /* 1789.84 counts/Amp used to
                                        generate Ip on the DAC */
                                     /* floating-point parameters */
#define Rs_F          1.34
#define L_F           1330.2e–6
#define CAP_F         94e–6
#define R_F           4.0
#define Ts_F          100e–6
#define Vg_F          7.0
#define VREF_F        3.3
/* feedback gains */
#define L1_F          –0.4709
#define L2_F          0.1340
#define L3_F          0.0183
#define GF_F          –0.01
/* global variable definition */
int leds;
int Isense_q12;
int Vsense_q12;
int VREF_q12;
unsigned int Ip_q12 = 0;
unsigned int Ipnom_q12;
unsigned int Imean_q12 = 0;
unsigned int Ivalle_q12 = 0;
unsigned int Vc_q12 = 0;
unsigned int Isense = 0;
unsigned int Vsense = 0;
int L1_q15,L2_q15,L3_q15,GF_q15;
```

```
int ua_q12=0;
int xa_q12=0;
int ya_q12=0;
int Ki_q15,Kv_q15;
int DAC_GAIN_q4;
ioport int port0C; /* leds */
unsigned int dac_value;
int I2DAC_q3;
/* function prototypes */
extern void meminit(void);
interrupt void INT1_isr(void);
interrupt void ADC_isr(void);
main()
{
float Imean_F=      VREF_F/R_F;
float Vdrop_F=      (Vg_F-Imean_
                      F*1.94)-
                      VREF_F;  /* inductor voltage drop */
float D_F=          (VREF_F+Imean_F*1.94)/(Vg_F);
float deltaI_F=     (Vdrop_F*D_F*Ts_F)/L_F;
float Ipnom_F=      Imean_F+deltaI_F/2;
meminit();          /* initialize routine in ASM */
/* initialize variables */
                                  /* Q-15 parameters range (-1,1) */
/* to convert to Q15: Z(Q155)=(int)(2^15*Z(Q0)) 2^15=0x8000*/
L1_q15=   (int)(0x8000*L1_F);
L2_q15=   (int)(0x8000*L2_F);
L3_q15=   (int)(0x8000*L3_F);
GF_q15=   (int)(0x8000*GF_F);
Ki_q15=   (int)(0x8000*Ki_F);
Kv_q15=   (int)(0x8000*Kv_F);
                                  /* Q-14 parameters range (-2,2) */
/* to convert to Q14: Z(Q14)=(int)(2^14*Z(Q0)) 2^14=0x4000*/
                                  /* Q-13 parameters range (-4,4) */
/* to convert to Q13: Z(Q13)=(int)((2^13)*Z(Q0)) 2^13=0x2000*/
                                  /* Q-12 parameters range (-8,8) */
/* to convert to Q12: Z(Q12)=(int)((2^12)*Z(Q0)) 2^12=0x1000*/
VREF_q12=         (int)(0x1000*VREF_F);    /* reference
                                                voltage */
Ipnom_q12=        (int)(0x1000*Ipnom_F);
Ivalle_q12=       (int)(0x1000*(Imean_F-(deltaI_F/2)));
                              /* Q-6 parameters range (-512,512)*/
```

```
/* to convert to Q6: Z(Q6) = (int)( (2^6)*Z(Q0) ) 2^6 = 0×40*/
                                        /* Q-4 parameters range () */
/* to convert to Q4: Z(Q4) = (int)( (2^4)*Z(Q0) ) 2^4 = 0×10*/
DAC_GAIN_q4 = (int)(0×010 * DAC_GAIN_F) ;
                                        /* Q-3 parameters range () */
/* to convert to Q4: Z(Q3) = (int)( (2^3)*Z(Q0) ) 2^3 = 0×08*/
I2DAC_q3 = (int)(0×08 * I2DAC_F);
/* large numbers */
/* initialize clock and wait states */
*CKCR1 = 0x00BB;  /* CLKIN (OSC) = 10 MHz, CPUCLK =
                     20 MHz */
*CKCR0 = 0x00C3;  /* CLKMD = PLL Enable, SYSCLK =
                     CPUCLK/2 */
*SYSCR = 0x40C0;  /* CLKOUT = CPUCLK */
WSGR = 0x0004;    /* set wait state generator for:
                  Program space: 0 wait states,
                  Data space: 0 wait states,
                  I/O space:    1 wait state */
/* initialize interrupts */
*XINTA1CR = XINT1_value;          /* set XINT1 */
*IFR = CLEAR_ALL_INT;             /* clear flags */
*IMR = INT_6 | INT_1;             /* unmask ADC int and external
                                     int */
asm("clrc INTM");                 /*Enable unmasked interrupts.*/
/* setup ADC for timer1 driven interrupt */
*ADCTRL1 = ADCTRL1_VALUE;  /* ch2(pin 5) for IL and ch10(pin
                              13) for Vc */
*ADCTRL2 = ADCTRL2_VALUE;
/* empty ADC FIFO */
   Isense = *ADCFIFO1;
   Isense = *ADCFIFO1;
   Isense = *ADCFIFO2;
   Isense = *ADCFIFO2;
/* setup EV timer */
*T1CON = T1CON_VALUE;
*GPTCON = GPTCON_VALUE;
*T1PR = 0x07D0;     /* timer 1 period register 100 us for 10 kHz*/
*T1CNT = 0x0000;    /* timer 1 counter register */
/* T1CMPR */        /* timer 1 compare register */
/* setup portB */
*OCRB = 0x000C;     /* portB is I/O */
*PBDATDIR = 0xFF00;  /* portB is output FF, all outputs low 00 */
```

```
/* main loop */
  leds = 32;
  port0C = leds;
  DAC0 = (int)(DAC_GAIN_F*2.0);/* set dac out to 3 V) */
  DACupdate = UPDATE;
  *PBDATDIR = 0xFFFF;/* switch ON */
for (;;) /* infinite loop */
{
  /* wait until IL>Ip
       this is tested by an external comparator
       that sets the INT1 */
} /* end for              */
}/* end main */
/*****************************
FUNCTIONS
*****************************/
interrupt void INT1_isr(void)        /* external interrupt for IL > Ip */
{
  *PBDATDIR = 0xFF00;/* switch OFF */
}
interrupt void ADC_isr(void)
{
/* switch on */
  *PBDATDIR = 0xFFFF;
/* read ADC */
  Isense = *ADCFIFO1;
  Isense = Isens>>6;   /* shift 10-bit ADC data to low byte */
  Isense_q12 = (int)(
                      (
                        (
                          (long)(Isense) * (long)(Ki_q15)
                          )<<(32–15–10 +6)/* q12*/
                        ) >>(16)
                    );       /* scale input to represent Amps */
  Vsense = *ADCFIFO2;
  Vsense = Vsense>>6;
  Vsense_q12 = (int)(
                      (
                        (
                          (long)(Vsense) * (long)(Kv_q15)
                          )<<(32–15– 10+6) /* q12 */
                        ) >>(16)
                    );   /* scale input to represent Volts */
```

```
  /* calculate additional dynamics */
xa_q12=xa_q12+ua_q12;
ua_q12=VREF_q12-Vsense_q12;
ya_q12=(int)(((long)(L3_q15)* (long)(xa_q12))<<1)>>16);
  /* calculate Ip */
Ip_q12=   Ipnom_q12 + ya_q12
    -(int)(((long)(L1_q15)* (long)(Isense_q12-Ivalle_q12))<<1)
      >>16)
    -(int)(((long)(L2_q15)* (long)(Vsense_q12-VREF_q12))<<1)
      >>m 16)
    +(int)(((long)(GF_q15)* (long)(VREF_q12))<<1)>>16);
  /* set DAC with new Ip value */
  dac_value=(int)(
                    (
                      (
                        (long)(Ip_q12) * (long)(I2DAC_q3)
                          )<<(32-16-15)
                    ) >>(16)
        );  /* scale input to represent Volts */
DAC0 =dac_value;
DACupdate=UPDATE;
}
```

10.5 UC3842-BASED FLYBACK DESIGN

A universal input voltage power supply was designed using a current-mode, discontinuous-conduction-mode, flyback converter, based on the UC3842 PWM controller [4]. The controller was previously discussed in Chapter 5 and the flyback topology was discussed in Chapter 4. Current-mode control has the advantage that an excellent line regulation can be achieved without considering the dynamic range of the error amplifier. Therefore, the error amplifier is dedicated to correcting for load variations. The current-mode, discontinuous-conduction-mode operation was selected because the flyback converter behaves as a first-order system with a left-half-plane zero. The right-half-plane zero, present in the continuous-conduction mode, which contributes to a nonminimal phase response, is shifted to high frequencies in current-mode discontinuous-conduction-mode. Therefore, the current-mode discontinuous-conduction-mode flyback converter is easier to control. The main drawback of this configuration is that the switches are subject to higher stresses than those of an equivalent continuous-conduction mode flyback converter (Figure 10.47).

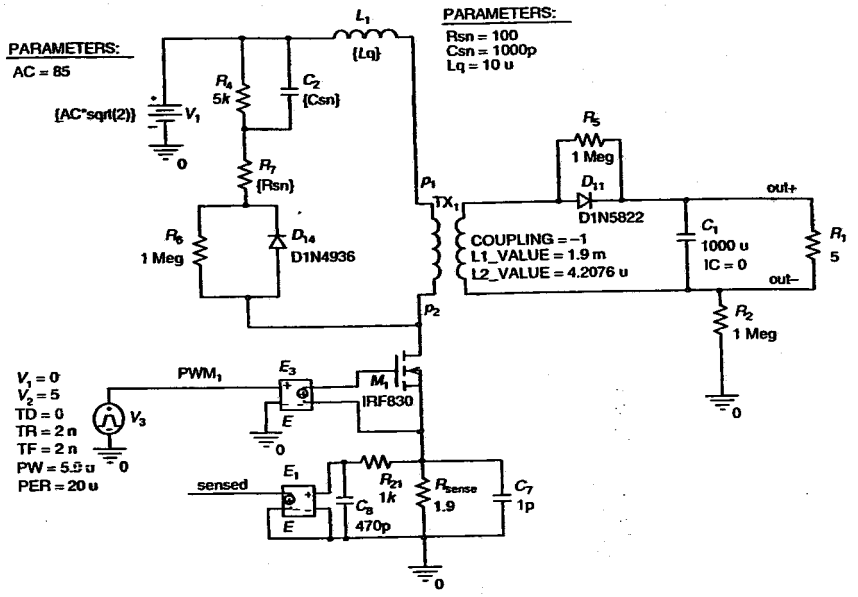

Figure 10.47 Open-loop schematic diagram of the flyback converter.

10.5.1 Design Specifications

The universal power supply should accept any standard AC input voltage between a minimum of $V_{ACmin} = 85\,V_{ac}$ and a maximum of $V_{ACmax} = 265\,V_{ac}$. The input frequency may be either 50 or 60 Hz. The output voltage should be within $5\,V \pm 5\%$. The normal load current is 750 mA, but a maximum current of 1 A is considered for the design. The switching frequency should be selected as 50 kHz. The flyback transformer has a primary of 89 turns with an inductance, L_p, of 1.9 mH. The secondary winding has four turns and the bias winding has 12 turns. The input EMI filter should be designed to provide a stable converter behavior.

10.5.2 Discontinuous Conduction Mode

The voltage conversion ratio can be calculated by evaluating the volt-second balance on the transformer coils. During the interval $0<t<t_{on}$, current flows through the primary inductor, L_p. The voltage across L_p ideally is equal to V_d. During the interval $t_{on}<t<t_2$, current flows through the secondary inductor, L_s. The voltage across L_s, ideally equal to V_o, is reflected to the primary by the transformer ratio, so

$$V_d t_{on} = V_o \frac{N_p}{N_s}(t_2 - t_{on}). \tag{10.60}$$

The current through the primary inductor reaches its maximum value, I_{1pk} at t_{on}

$$V_d = L_p \frac{I_{1pk}}{t_{on}}. \tag{10.61}$$

The average primary current, I_{1avg}, is

$$I_{1avg} = \frac{t_{on} I_{1pk}}{2T}. \tag{10.62}$$

When the primary transistor turns off at t_{on}, the current in the primary inductor drops down to zero instantaneously and the energy is transferred to the secondary inductor. The current of the secondary inductor starts from the peak value, I_{2pk}, and decreases in amplitude until all the energy stored in the magnetic field is released to the load at $t = t_2$. From this point up to the end of the switching period, the current on both inductors are zero. The peak value of the secondary current is

$$I_{2pk} = I_{1pk} \frac{N_p}{N_s}. \tag{10.63}$$

The average value of the secondary current is equal to the average load current, then

$$I_o = \frac{(t_2 - t_{on})}{T} \frac{N_p}{N_s} \frac{I_{1pk}}{2}. \tag{10.64}$$

The ideal average output voltage is

$$V_o = L_s \frac{N_p}{N_s} \frac{I_{1pk}}{(t_2 - t_{on})}. \tag{10.65}$$

The on-time can be calculated from Equation (10.61) as

$$t_{on} = L_p \frac{I_{1pk}}{V_d} \tag{10.66}$$

and the off-time can be calculated from Equation (10.64) as

$$(t_2 - t_{on}) = 2T \frac{I_o}{I_{1pk}(N_p/N_s)}. \tag{10.67}$$

Substituting Equations (10.66) and (10.67) into Equation (10.60), we obtain an expression for the peak value of the primary current

$$I_{1pk} = \sqrt{\frac{2V_o I_o T}{L_p}}. \tag{10.68}$$

According to Equation (10.68), the peak current on the primary winding is inversely proportional to the primary inductance and the switching frequency.

An expression for the voltage conversion ratio can be obtained by replacing Equation (10.68) into Equation (10.61)

$$\frac{V_o}{V_d} = D\sqrt{\frac{TR}{2L_p}}. \tag{10.69}$$

Therefore, the nominal duty cycle is

$$D = \frac{V_o}{V_d}\sqrt{\frac{2L_p}{TR}}. \tag{10.70}$$

10.5.3 Preliminary Calculations

Preliminary calculations can be performed to estimate the peak current and the duty cycle in the circuit without losses. From Equation (10.68), the peak current flowing through the primary inductor is

$$I_{1pk} = \sqrt{\frac{2(V_o + V_f)I_o T}{L_p}} = \sqrt{\frac{2(5+0.7)\times 1 \times 20 \times 10^{-6}}{1.9 \times 10^{-3}}}$$
$$= 0.346\,\text{A}. \tag{10.71}$$

Since the diode voltage drop is significant in comparison with the output voltage, the voltage drop across the output diode was added in Equation (10.71) to obtain a more accurate result. Using this value for I_{1pk},

$$t_{on} = L_p \frac{I_{1pk}}{V_d} = 1.9 \times 10^{-3}\frac{0.346}{120} = 5.48\,\mu\text{s} \tag{10.72}$$

and the duty cycle is

$$D = \frac{t_{on}}{T} = \frac{5.48}{20} = 0.274. \tag{10.73}$$

The inductances of the secondary and bias windings of the transformer can be calculated from the design specifications as

$$L_s = \frac{L_p}{(N_p/N_s)^2} = \frac{1.9\,\text{mH}}{(85/4)^2} = 4.2076\,\mu\text{H} \tag{10.74}$$

and

$$L_b = \frac{L_p}{(N_p/N_b)^2} = \frac{1.9\,\text{mH}}{(85/12)^2} = 37.869\,\mu\text{H} \tag{10.75}$$

10.5.4 Open-Loop Simulations

Open-loop PSpice simulations were performed to estimate the required duty cycle to maintain the nominal output voltage, $V_o = 5\,\text{V}$, when the component losses were included. Figure 10.48 demonstrates that the switch has to be on for a longer time to compensate for the modeled circuit losses, i.e., $t_{on} = 5.9\,\mu\text{s}$, compared with $5.48\,\mu\text{s}$ obtained previously without considering losses. With this duty cycle, $D = 29.5\%$, the average output voltage is close to 5 V and the voltage ripple, ΔV_o, is less than 15 mV.

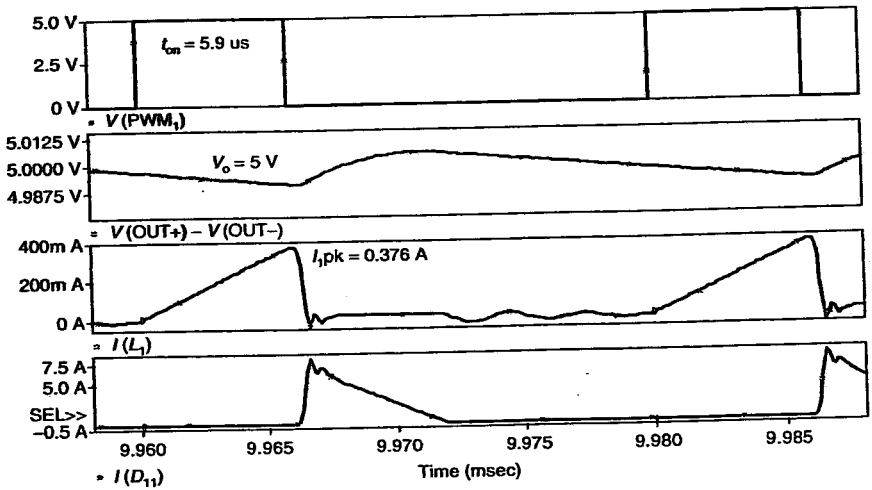

Figure 10.48 Simulated waveforms for the open-loop flyback converter.

In this simulation, the output capacitor's ESR was neglected. If it was considered, the output voltage would have been affected by a larger voltage ripple. The current on the primary side of the flyback transformer increases linearly during t_{on} until it reaches its peak value, $I_{1pk} = 0.376$ A. When the switching transistor is switched off, current starts to flow on the secondary winding and the primary current goes down to zero. The energy stored in the magnetic field is transferred to the load while the secondary current decreases. When the secondary current reaches zero, all the energy stored in the magnetic field has been released and the load current is provided solely by the output capacitor. The output capacitor is charged only when the secondary current is higher than the load current. This explains the output ripple voltage waveform.

This simulation also shows that the flyback converter operates in the discontinuous-conduction mode even under the worst-case condition, i.e., during smallest input voltage and largest output current. The secondary current becomes zero before the end of the switching period.

10.5.5 Current Loop

The internal current loop produces the current-mode control. For current-mode control, the duty cycle is controlled by the peak current of the primary inductor, according to

$$D = I_{1pk} \frac{L_p}{V_d T}. \tag{10.76}$$

Therefore, by changing I_{1pk}, the output voltage can be controlled:

$$V_o = I_{1pk} \sqrt{\frac{RL_p}{2T}}. \tag{10.77}$$

10.5.6 Voltage Loop

The external voltage loop transforms the current-mode controller into a voltage regulator. The error amplifier of the UC3842 calculates the necessary primary peak current as

$$I_{cont} = \{[V_{ref} + (V_{ref} A_1 - V_f A_2)] - 1.4\,V\} \frac{R}{3R} \tag{10.78}$$

or

$$I_{cont} = \frac{V_{EAO} - 1.4V}{3}. \tag{10.79}$$

This value is saturated at 1 V by having the Zener diode connected at the inverting input of the comparator.

10.5.6.1 Current-Sensing Resistor and Filtering

The current-sensing resistor, R_{sense}, was calculated for the worst-case condition that would generate the maximum duty cycle. This condition occurs when the minimum input voltage, $V_i = 85 V_{ac}$, and the maximum output current, $I_o = 1$ A, are met simultaneously. The current-sensing resistor is calculated so that the maximum dynamic range of the PWM modulator is used. For the worst-case condition, the voltage across R_{sense} should be 1 V. Hence

$$R_{sense} = \frac{1\text{ V}}{0.36\text{ A}} = 2.7\,\Omega. \tag{10.80}$$

The previous value was obtained based on 100% efficiency. A more realistic value can be obtained by estimating the typical efficiency of a flyback converter at 75%. Therefore, the input current would be 43% larger than the ideal value. Thus

$$R_{sense} = \frac{1\text{ V}}{1.43(0.36\text{ A})} = 1.9\,\Omega. \tag{10.81}$$

The maximum average input current $I_{d\,max}$ is

$$I_{d\,max} = \frac{V_o I_{o\,max}}{0.7\,V_{i\,min}} = \frac{5\text{ V} \times 1\text{ A}}{0.7 \times 120\text{ V}} \approx 60\text{ mA}. \tag{10.82}$$

Consequently, the maximum average power dissipated in the current-sensing resistor is

$$P_s = I_{d\,max}^2 R_{sense} = 6.84\text{ mW}. \tag{10.83}$$

A noninductive metallic resistor of 1/4 W is chosen as the current-sensing resistor.

There is a fast transient at the turn on of the switching transistor due to the rectifier recovery and the interwinding capacitance of the flyback transformer. The amplitude of this spike may be larger than I_{1pk} and it has to be filtered, otherwise it may prematurely terminate the conduction of the switching transistor. A simple R–C filter is usually sufficient to attenuate this spike. The time constant of the filter is calculated to be equal the duration of the spike. R was chosen to be 1 kΩ and C was calculated to be 470 pF for a time constant $RC = 470$ ns. Figure 10.49 shows the waveforms corresponding to the current flowing through the primary inductor, the voltage across the current-sensing

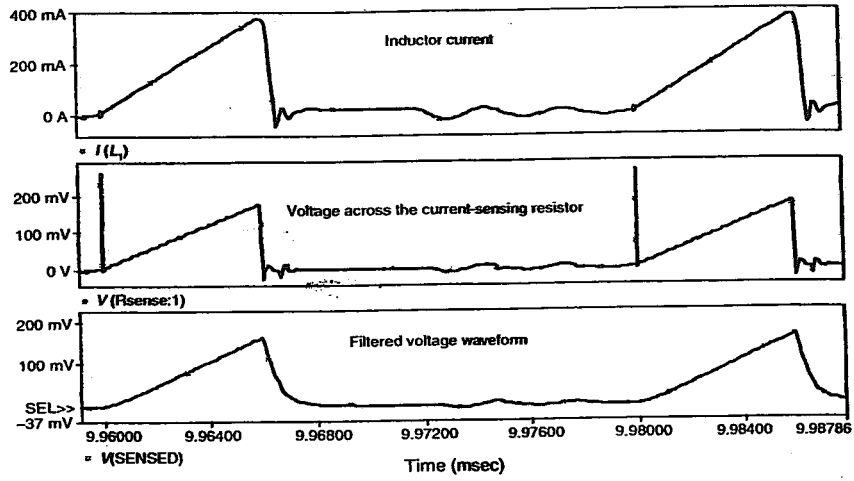

Figure 10.49 Conditioning the current sample.

resistor and the same voltage after passing through the low-pass filter to attenuate the spike. Originally, the spike was larger than the peak current. After passing through the RC filter, the spike has been completely removed.

10.5.6.2 Dissipative Snubber

A dissipative snubber, shown in Figure 10.50, is usually connected across the primary winding to alleviate the voltage stress of the switching transistor. When the transistor turns off, the primary inductor produces an inductive kick that increases the voltage at the drain of the transistor above the DC bus voltage level. When this happens, D_{14} is forward-biased and charges C_2 through R_7, transferring the energy from the inductive kick to the capacitor. The inductive effect disappears when the diode connected to the secondary winding becomes forward bias. The energy stored in C_2 is dissipated into R_4 during t_{off}. The time constant R_7–C_2 should be smaller than the time taken by the output rectifier to achieve full conduction. The time constant R_4–C_2 should be smaller than t_{off}. The values of C_2 and R_7 should be adjusted by parametric transient simulations to yield an acceptable transient on the drain of the transistor. The final values for these components are $R_7 = 100\ \Omega$ and $C_2 = 1000$ pF.

10.5.6.3 The Error Amplifier

The schematic diagram of the error amplifier is shown in Figure 10.51 and the voltage conversion ratio is shown in Figure 10.52. The error amp-

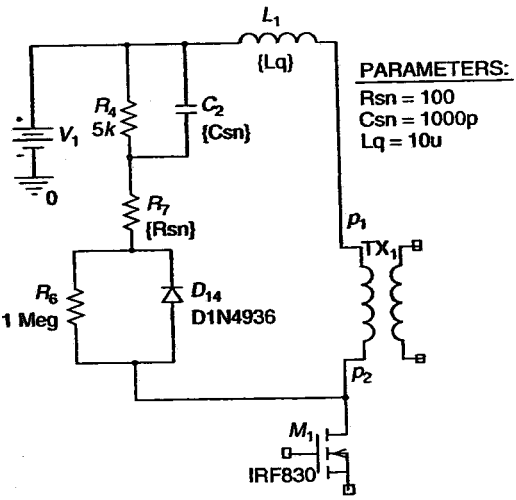

Figure 10.50 Dissipative snubber.

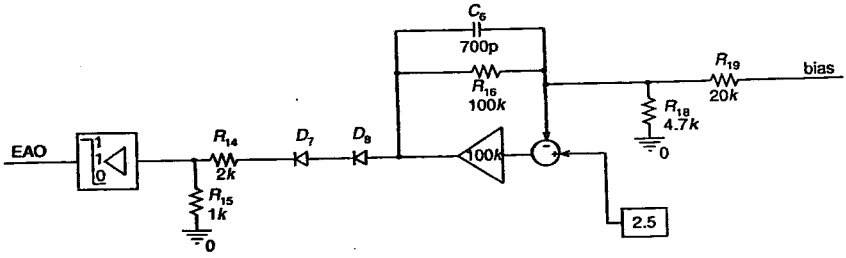

Figure 10.51 Schematic diagram of the error amplifier.

lifier output, EAO, reaches 1 V when the feedback voltage $V_f = 12.8$ V and it decreases linearly to 0 V for $V_f = 13.4$ V. Therefore, V_f has to be constrained between these two values to achieve full regulation. EAO is the control voltage that determines the peak value of the primary current and the duty cycle. This voltage must be equal to 1 V for $V_d = 120$ V and $I_o = 1$ A to generate the necessary duty cycle to regulate the output voltage to 5 V.

10.5.6.4 The Bias Circuit

The UC3842 is initially powered from the input mains through a resistor divider. After a few switching cycles, the output voltage builds up and charges the bias capacitor C_4, which continues supplying the power to

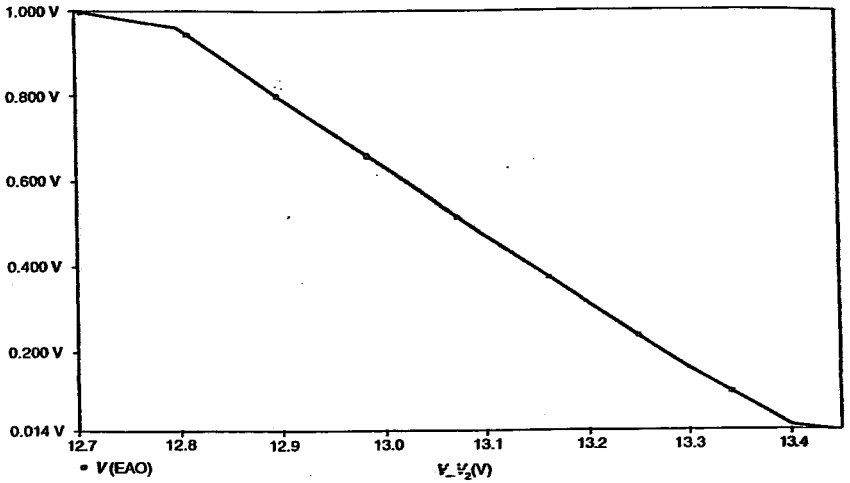

Figure 10.52 Voltage conversion ratio of the error amplifier.

the controller. The schematic diagram for the bias circuit is shown in Figure 10.53. The resistors in parallel with the diodes are used to improve convergence in the simulations. A zener diode, modeled with a DC voltage source, is connected in series with the bias winding to reduce the voltage to within the operating range of the controller. This was necessary because the available transformer had a larger bias voltage than is needed.

10.5.7 Small Signal Model

The current-mode flyback converter operating in the discontinuous-conduction-mode behaves as a first-order system. The first-order pole is located at

$$f_p = \frac{1}{\pi R C_o} = \frac{1}{\pi \times 5 \times 1000 \times 10^{-6}} = 64\,\text{Hz} \tag{10.84}$$

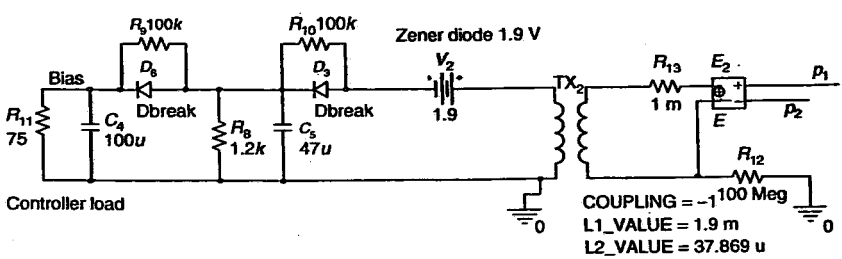

Figure 10.53 Bias circuit.

and the left-half-plane zero is located at

$$f_{zesr} = \frac{1}{2\pi R_{esr} C_o} = \frac{1}{2\pi \times 0.1 \times 1000 \times 10^{-6}} = 1592\,\text{Hz}. \tag{10.85}$$

There is a right-half-plane zero, but it is located at high frequencies and can be neglected.

The component Flyback_current-mode [5] (see Figure 10.54) is based on the averaged inductor model [6] and is used to perform PSpice simulations. The control voltage comprises of a DC value, which sets the operating point, and an AC value that yields the small-signal variations.

10.5.8 Frequency Compensation

The frequency compensation was calculated based on small-signal PSpice simulations. The small-signal model, based on Ref. [5], used to measure the loop response, is shown in Figure 10.54. The transformer ratio is equal to N_2/N_1. The small-signal gain from the output to the bias voltage was obtained as the incremental gain for two different output voltages, as

$$\frac{\Delta V_{BIAS}}{\Delta V_o} = \frac{13.097 - 13.020}{5.1253 - 5.0094} = 0.6643\frac{V}{V}. \tag{10.86}$$

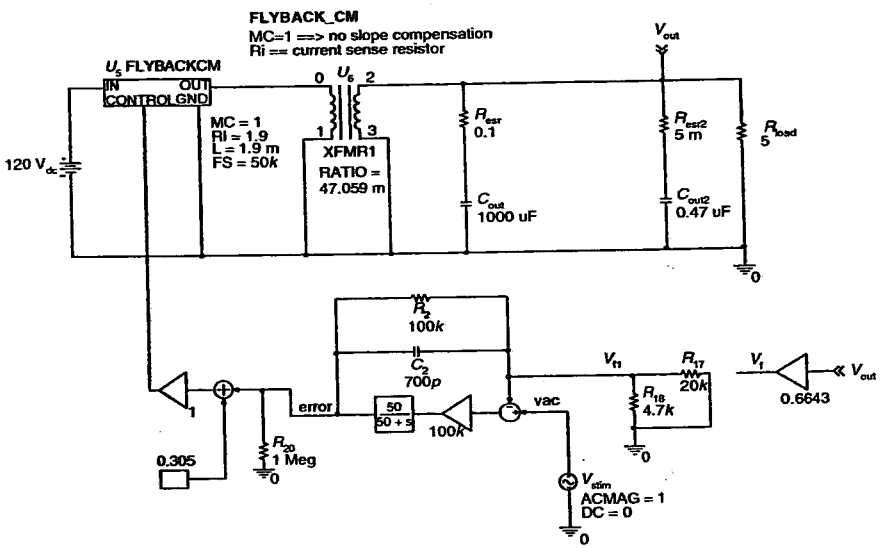

Figure 10.54 Small-signal model used to measure the loop gain.

The transfer function of the proportional compensation network is

$$\mathrm{TF} = \frac{R_2}{R_{16}//R_{17}} \frac{1}{sC_2R_2 + 1}. \tag{10.87}$$

Thus, the frequency of the pole of the compensation network is

$$f_p = \frac{1}{2\pi R_2 C_2}. \tag{10.88}$$

Choosing f_p to cancel the zero of the transfer function of the flyback converter, C_2 can be calculated as

$$C_2 = \frac{1}{2\pi R_2 f_p} = \frac{1}{2\pi \times 150k \times 1.5k} = 700\mathrm{pF}. \tag{10.89}$$

An AC analysis was performed to obtain the Bode plot of the loop gain shown in Figure 10.55. As shown, the magnitude of the loop gain decreases at −20 dB/dec after the pole frequency. The zero was cancelled by the pole of the compensation network and the best phase margin that can be obtained (with this compensation network) is 90°. The 0 dB crossover frequency is 12.3 kHz, which is close to one fifth of the switching frequency.

10.5.8.1 Closed-Loop Simulations

Transient simulations were performed using the schematic circuit shown in Figure 10.56 to verify the design. Figure 10.57 shows the start-up transient

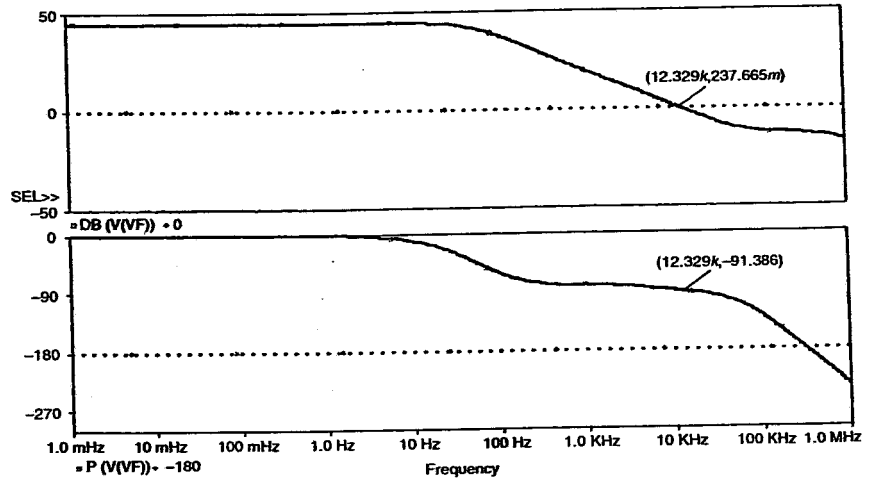

Figure 10.55 Bode plot of the loop gain.

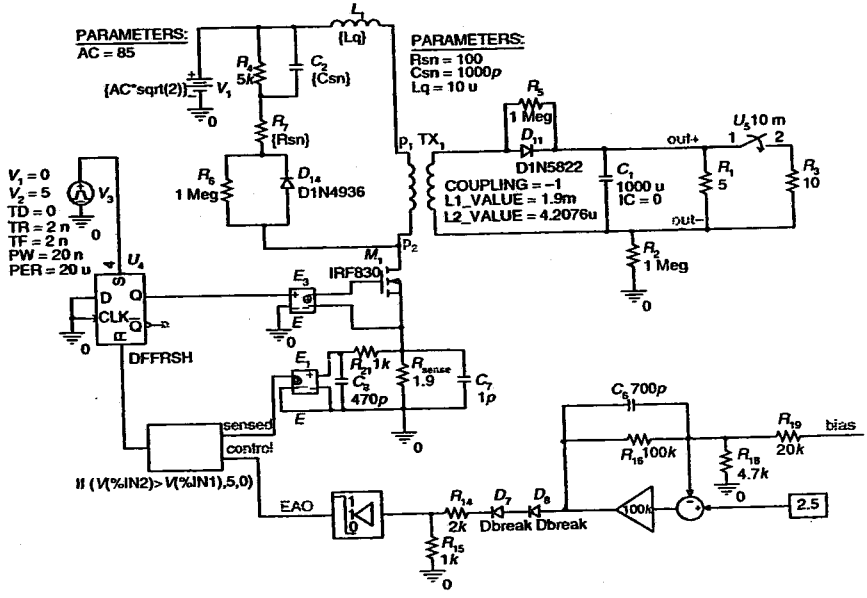

Figure 10.56 Closed-loop converter schematic for transient analysis.

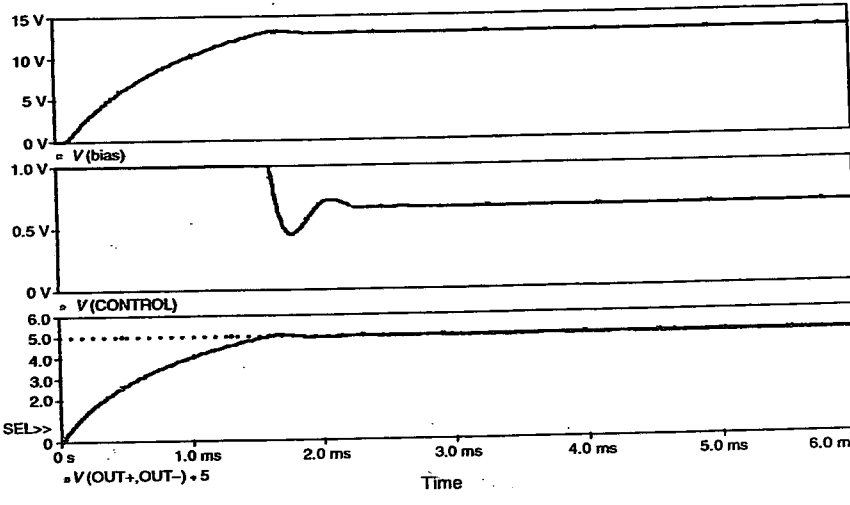

Figure 10.57 Transient response with the calculated frequency compensation.

of the flyback converter using the calculated compensation. The control voltage saturates at the beginning and then decreases to the calculated nominal value. The output voltage shows the response of a first-order system and finally settles to 5 V. Note that the bias voltage is within the calculated range.

Figure 10.58 displays the transient response of the closed-loop flyback converter due to a load change. The load initially started at 10 Ω, and at 10 ms, the load was changed to 5 Ω. For a 10-Ω load resistor, the output voltage is 5.13 V. A steady-state error was expected due to the use of the proportional control. For the 5-Ω load, the steady-state error goes to zero because this was the nominal load value used for the calculations. Nevertheless, the regulation is within the specified 5%.

10.5.9 EMI Filter Design

The EMI filter should prevent conducted EMI originated at the switching converter to reach the AC mains (Figure 10.59). The EMI filter was calculated according to the guidelines given in Chapter 6. Therefore, the cutoff frequency of the filter was chosen to be at least one decade below the switching frequency and the output impedance of the EMI filter was designed to be much smaller than the input impedance of the closed-loop flyback converter. PSpice simulations based on the small signal model of the flyback converter were used to improve the design and verify its performance. Figure 10.60 shows the output impedance of the EMI filter, calculated using a corner frequency $f_c = 2.5$ kHz.

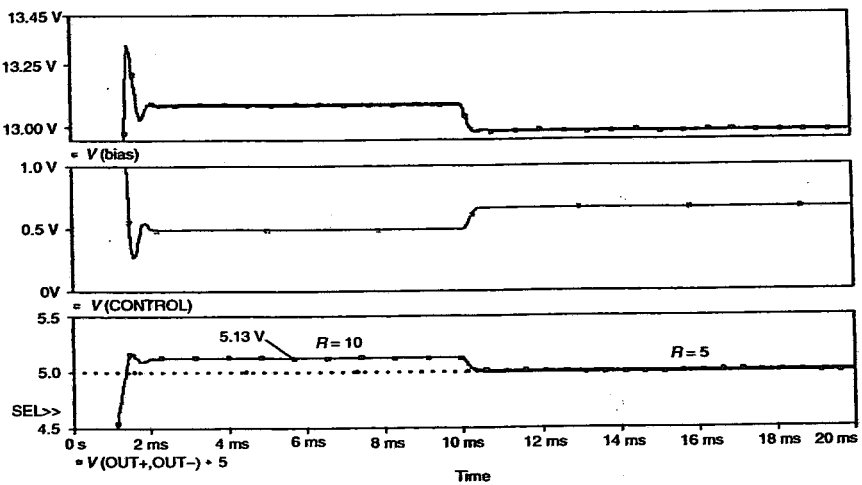

Figure 10.58 Transient response to a load step at 10 ms.

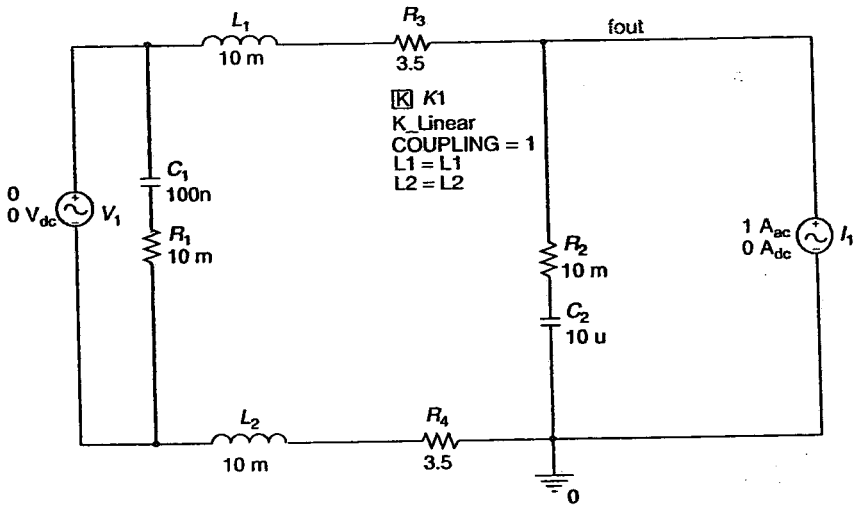

Figure 10.59 EMI filter.

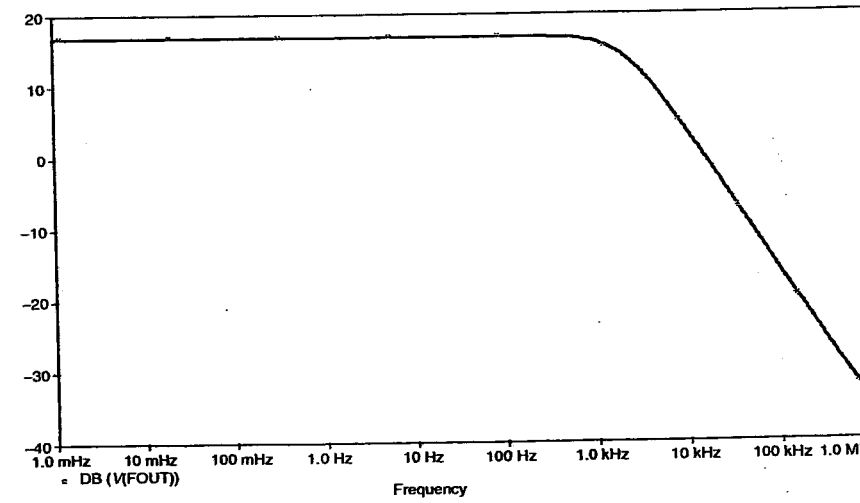

Figure 10.60 Output impedance of the EMI filter.

The PSpice small-signal model for the flyback converter, including the EMI filter is shown in Figure 10.61 and the simulation results of an AC analysis are displayed in Figure 10.62. These figures show that the cutoff

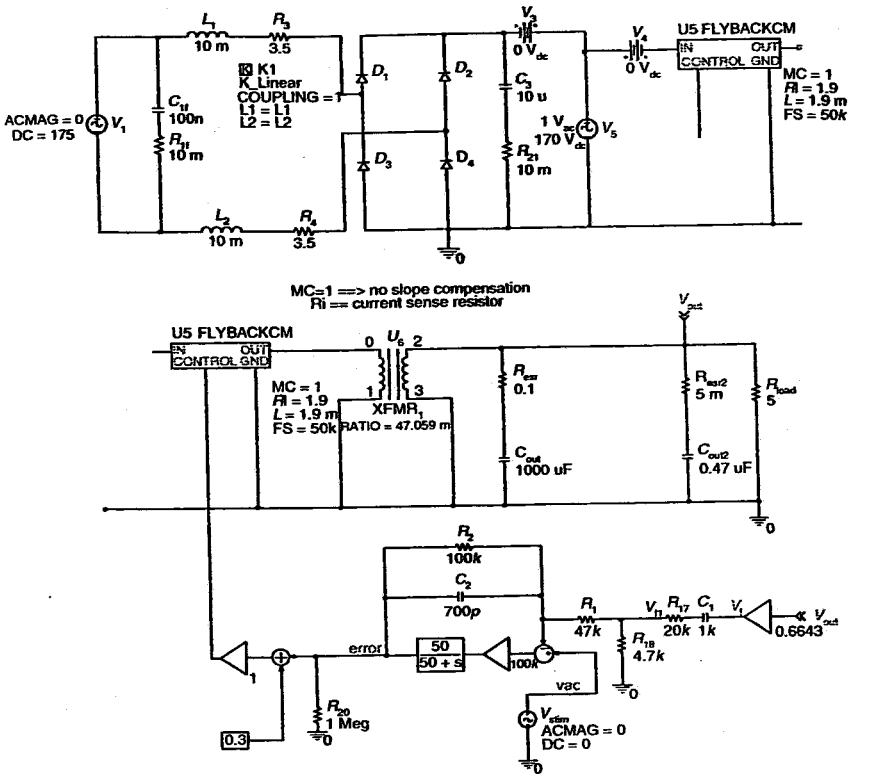

Figure 10.61 Small-signal model used to measure the impedances.

frequency of the filter is 2.2 kHz and that the output impedance of the EMI filter is much smaller than the input impedance of the flyback converter, as desired. Thus, the presence of the EMI filter should not compromise the stability of the flyback converter.

10.5.10 Printed Circuit Board Design

Figure 10.63 shows the printed circuit board layout of the universal power supply. The bottom layer is displayed on the left and the top layer on the right. The top layer is used only for the ground plane. The plane is divided into two current paths. The left portion carries high switching currents, while the right portion carries low-level currents used for control signals. The ground plane does not reach the bottom part of the board to avoid interaction with the input AC voltage. The MOSFET is surrounded by the

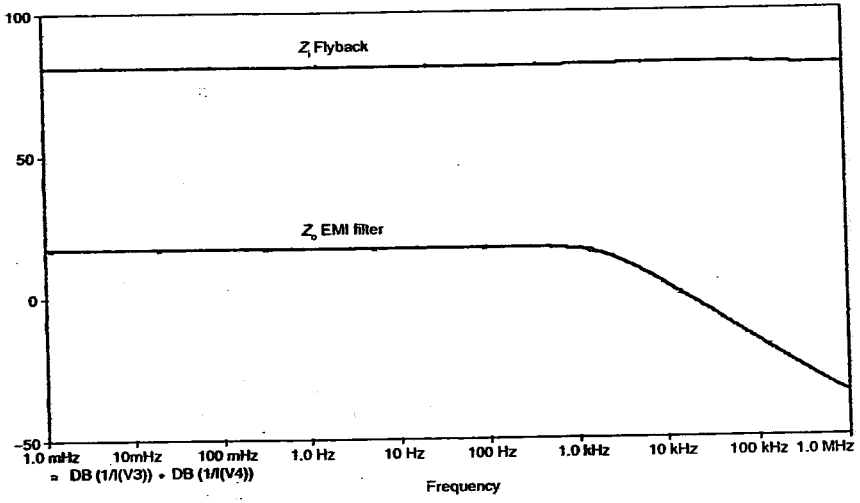

Figure 10.62 Output impedance of the EMI filter and input impedance of the flyback converter.

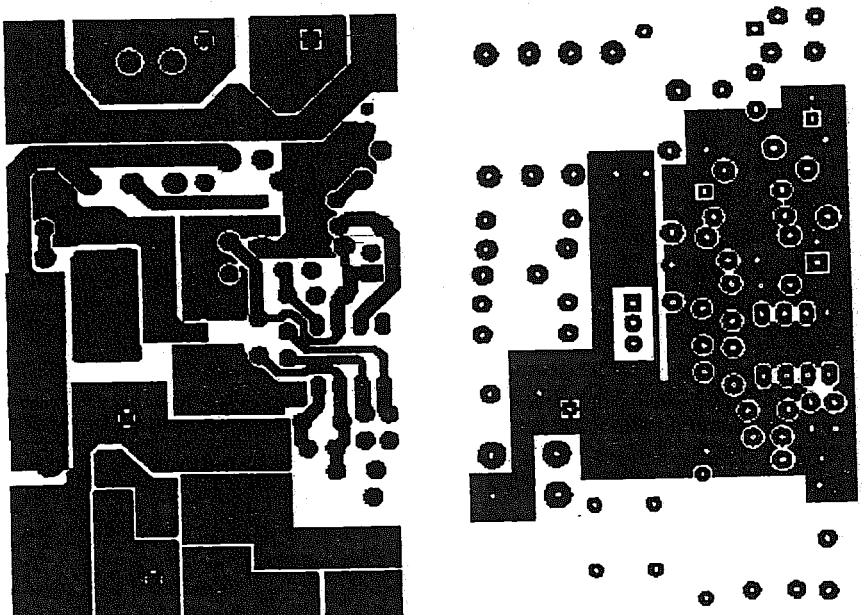

Figure 10.63 PCB layout of the universal power supply.

ground plane that acts as a short-circuited coil to attenuate the radiation of noise to other circuit components. The bottom layer carries the rest of the connections, which are not tied to ground. The tracks are as short and wide as possible. The components are laid out in such a way that interaction between sensitive signals (e.g., control signals) and noisy signals (e.g., high voltage, high current, fast transients) are minimized. The output circuitry is located in the top portion of the board. The middle sector is reserved for the control and components of the primary side of the converter. The AC input, EMI filter, and the voltage rectifier are placed at the bottom of the board. The silk screen is shown in Figure 10.64 and a photograph of the prototype of the universal power supply is shown in Figure 10.65.

10.5.11 Experimental Results

The primary current (as measured at the sensing resistor) and drain voltage waveforms of the flyback converter are shown in Figure 10.66. When the MOSFET is switched on, the current flowing through the primary inductor increases linearly until it reaches the peak value set by the controller. When the MOSFET is switched off, the current decreases rapidly to zero, transferring the conduction to the secondary winding. The drain voltage increases to a

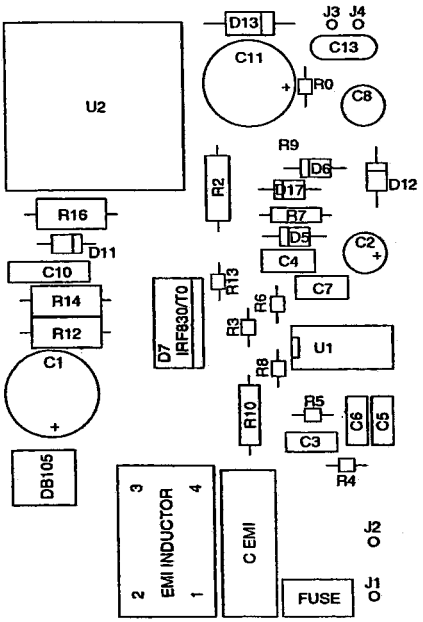

Figure 10.64 Silk screen of the PCB of the universal power supply.

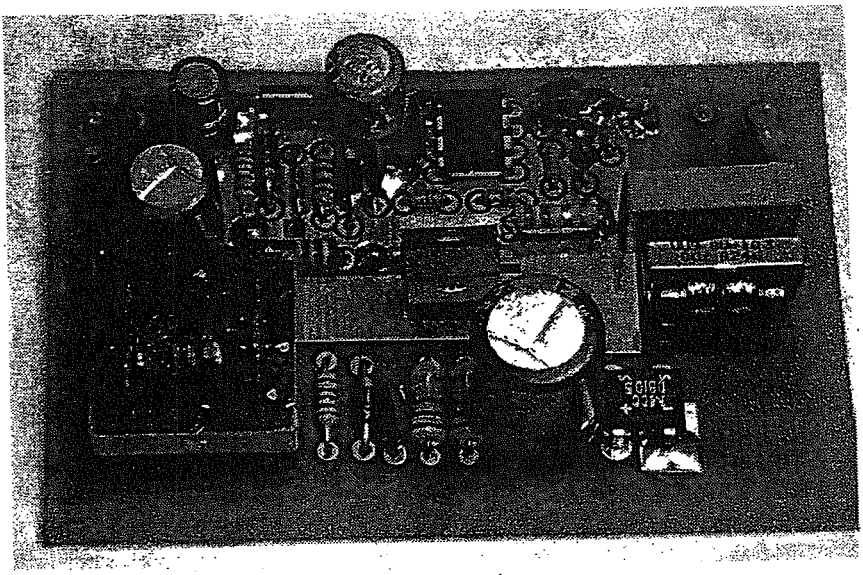

Figure 10.65 Photo of the universal power supply.

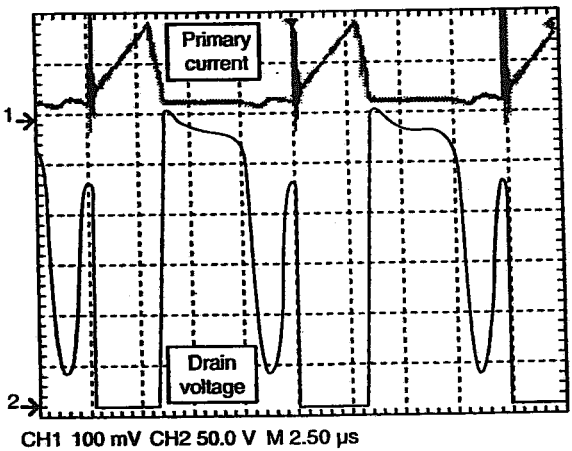

Figure 10.66 Primary current and drain voltage waveforms of the flyback converter.

voltage larger than the input DC voltage. When all the energy stored in the magnetic field has been transferred to the output, the conduction on the secondary side ceases and an oscillatory drain voltage can be seen. Notice

the large spike present on the current waveform at turn-on. This transient must be filtered using a low-pass filter before feeding to the PWM modulator.

The measured output voltage ripple, with an amplitude of 146 mV_{pp}, is shown in Figure 10.67. The output voltage ripple may be reduced by replacing the output capacitor with an LC low-pass filter or by using an output capacitor with a lower ESR.

The output voltage and current waveforms of the flyback converter during a load transient are shown in Figure 10.68. The load resistance was reduced from 10 to 5 Ω. As can be seen, the output voltage drops to 150 mV (which is a 3% variation from the nominal voltage) before recovering to its steady-state value after 300 ns.

10.6 TOPSWITCH-BASED FLYBACK DESIGN

A universal input voltage power supply was designed using a current-mode discontinuous-conduction-mode flyback converter, based on the TopSwitch PWM controller [7]. The controller was previously discussed in Chapter 5 and the flyback topology in Chapter 4. This controller has a unique current-mode control scheme using variable switching frequency that skips pulses, when necessary, to achieve regulation. In contrast to the UC3842-based flyback design, which uses a primary-side regulation scheme (as shown in Section 10.5), this design uses a secondary-side regulation scheme. This means that the output voltage on the secondary side of the power transformer is sensed and fed back to the controller through an opto-coupler.

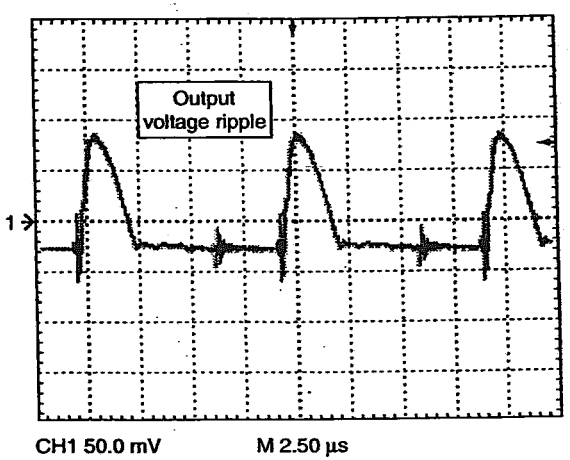

Figure 10.67 Output voltage ripple of the flyback converter.

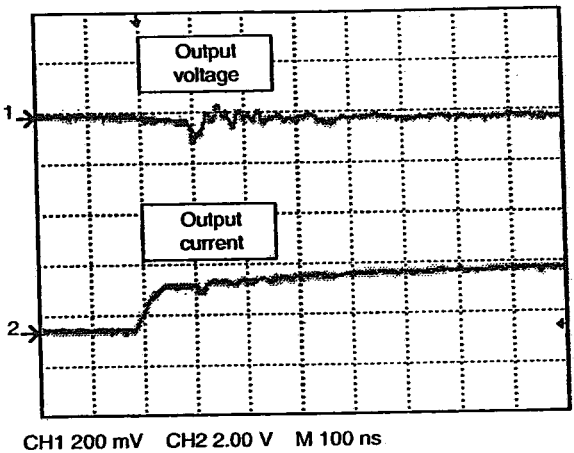

Figure 10.68 Output voltage ripple and current of the flyback converter during a load transient.

This type of regulation scheme usually achieves a better regulation than that of the primary-side regulation.

10.6.1 Design Specifications

The universal power supply should accept any standard AC input voltage between a minimum of $V_{ACmin} = 85\,V_{ac}$ and a maximum of $V_{ACmax} = 265\,V_{ac}$. The input frequency may be either 50 or 60 Hz. The output voltage should be within 5 V ± 5%. The output power is 20 W. The nominal switching frequency is 135 kHz. The flyback transformer has 36 turns with a primary inductance of 490 μH. The secondary winding has four turns and the bias winding has five turns. The input EMI filter should provide a stable converter behavior. A design efficiency of $\eta = 0.8$ is adopted. The estimated loss allocation factor, $Z = 0.5$, assigns an even distribution of the losses between the primary and the secondary sides of the converter.

10.6.2 Preliminary Calculations

As shown below, the flyback converter operates in the discontinuous-conduction mode; therefore, the design parameters will be evaluated using the discontinuous-conduction mode equations. The output voltage reflected back to the primary winding can be estimated as $V_{or} = 135$ V; therefore, the clamping voltage of the zener diode is chosen to be 200 V. The maximum duty cycle can be estimated as

$$D_{max} = \frac{V_{or}}{K_p(V_{min} - V_{ds}) + V_{or}} = \frac{135}{1(90-10)+135} = 0.63, \quad (10.90)$$

where $V_{ds} = 10\,V$ for the TopSwitch. The primary peak current is

$$I_p = \frac{2P_o}{D_{max}\eta V_{min}} = \frac{2 \times 20}{0.63 \times 0.8 \times 90} = 0.88\,A. \quad (10.91)$$

Thus, the primary RMS current is

$$I_{RMS} = \sqrt{D_{max}\frac{I_p^2}{3}} = \sqrt{0.63\frac{0.88^2}{3}} = 0.4\,A. \quad (10.92)$$

The calculated primary inductance is similar to the primary inductance of the transformer

$$\begin{aligned} L_p &= \frac{10^6 P_o}{I_p^2 0.5 f_{smin}} \frac{Z(1-\eta)+\eta}{\eta} \\ &= \frac{10^6 \times 20}{(0.88^2)(0.5)(130000)} \frac{0.5(1-0.8)+\eta}{0.8} \\ &= 447\,\mu H. \end{aligned} \quad (10.93)$$

The secondary RMS current is

$$I_{RMS} = I_{sp}\sqrt{\frac{1-D_{max}}{3K_p}} = I_{sp}\sqrt{\frac{1-0.63}{3}} = 4.7\,A, \quad (10.94)$$

where K_p is the primary current waveform parameter. It is equal to one for discontinuous mode.

Figure 10.69 shows the schematic diagram of the universal power supply implemented using the TopSwitch controller. The EMI filter, $Cx1 - L1$, attenuates conducted EMI from the converter from going to the mains. The voltage-clamping circuit, $D_1 - D_6$, prevents the drain voltage on pin 7 of the controller to overshoot above $V_{DC} + V_d + V_z$. The secondary-side regulation is achieved by sensing the output voltage through the opto-coupler. The bias winding provides the supply power to the controller. The output voltage may be changed by adjusting the variable resistor, V_R, which sets the voltage on the shunt voltage regulator, TL431.

10.6.3 Experimental Results

A prototype was built following the instructions provided in the data sheets.

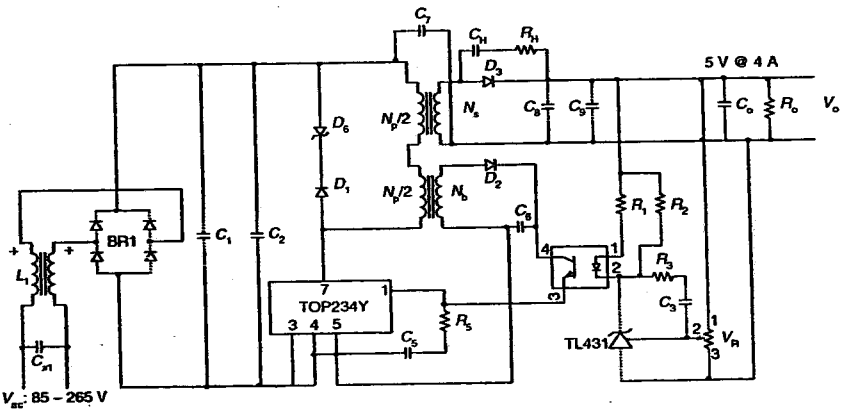

Figure 10.69 Universal power supply implemented with the TopSwitch.

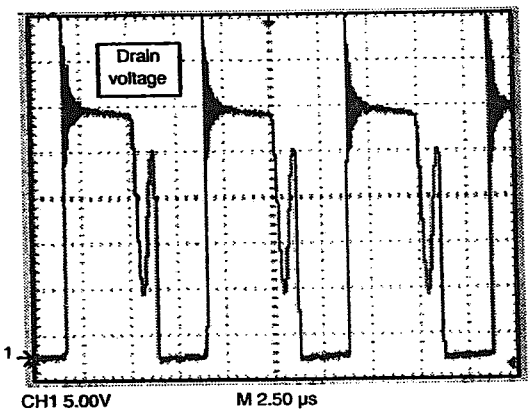

Figure 10.70 Drain voltage waveform of the TopSwitch-based converter.

Figure 10.70 shows the measured drain voltage waveform using a 10× voltage probe. This is the typical waveform of a flyback converter. The average value is 158 V and the overshoot is approximately 100 V. The switching frequency was measured to be at 133 kHz.

The frequency of the output voltage ripple, shown in Figure 10.71, was measured to be 135.2 kHz, in good agreement with the design. The measured amplitude of output voltage ripple was 112 mV_{pp}. It should be noted that the output capacitor is charged during the off-time of the switching transistor.

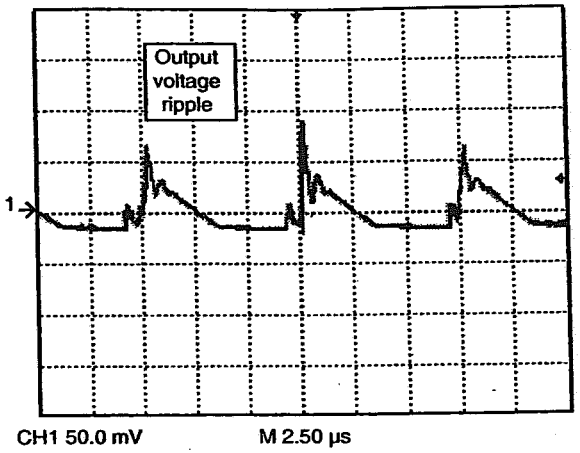

Figure 10.71 Output voltage ripple of the TopSwitch-based converter.

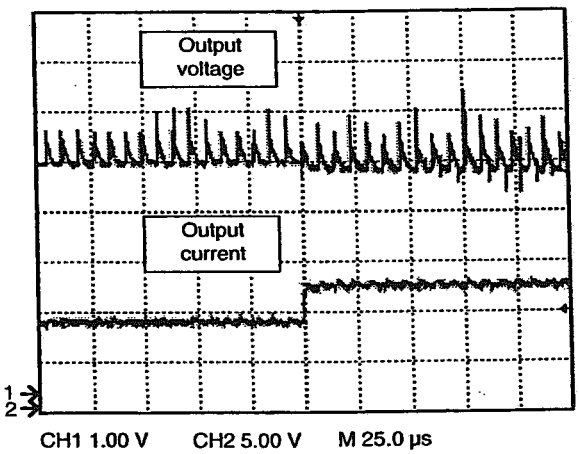

Figure 10.72 Output voltage and current of the TopSwitch-based converter during a load transient.

Figure 10.72 shows the output voltage and current waveforms during a load transient from 10 to 5 Ω. For the larger load current the average output voltage decreases and the switching ripple increases. As can be seen, the output voltage reaches its steady-state value after three switching cycles.

10.6.3.1 Line Regulation

The line regulation was evaluated for a constant load of 5 Ω. The experimental results are summarized in **Table 10.1**, as expected from a current-mode flyback converter, the line regulation is excellent, below 2%.

10.6.3.2 Load Regulation

The load regulation was evaluated under a constant input voltage of 110 V_{ac}. The measured load regulation is better than 1% within the testing range of load (i.e., for the output resistance changing from 4.5 to 24 Ω). Table 10.2 shows the measured data.

10.7 TINYSWITCH-BASED FLYBACK DESIGN

A third universal power supply was built based on a TinySwitch controller [8]. The power rating of this power supply is 5 W. The circuit, shown in Figure 10.73, is based on the typical application circuit given in the controller's data sheet. The rectified DC voltage is obtained from the mains through fuse R_1 and bridge rectifier U_3. The low-pass filter comprises L_1–L_2–C_1–C_2 and has the dual function of filtering the rectified voltage as well as acting as the EMI filter. The TinySwitch, TNY266P, is connected in the primary side of the flyback transformer. The clamping snubber circuit, formed by R_4–C_7–R_3–D_5, is connected in parallel with the primary winding to suppress the oscillations of the voltage across the MOSFET transistor of the TinySwitch. The output rectifier, D_6, is connected in series with the secondary winding of the flyback transformer. A ceramic capacitor, C_8, is added in parallel with the output capacitor, C_4, to compensate for the inductive response of the electrolytic capacitor. A bleeding resistor, R_8, ensures that a minimum current is drawn from the output, thus leading to the normal operation of the circuit. The output voltage can be varied by adjusting the

Table 10.1 Measured line regulation of the TopSwitch-based converter

V_{AC}	85	90	100	110	120	130	140
V_{DC}	11.75	11.85	11.98	11.87	11.86	11.85	11.84

Table 10.2 Measured load regulation of the TopSwitch-based converter

Load (Ω)	4.5	5	7.5	9.5	14.5	19.5	20	24
V_{DC} (V)	11.93	11.9	11.93	11.93	11.96	11.96	11.93	11.97

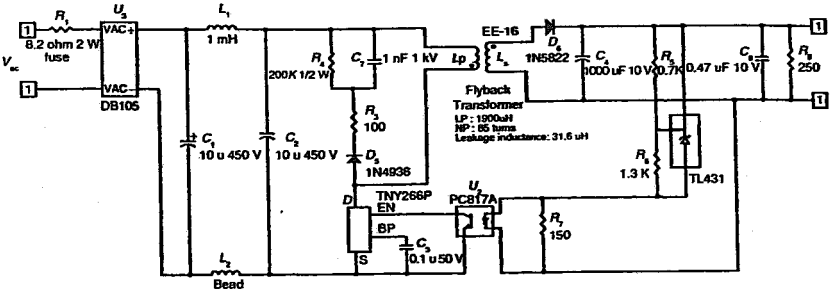

Figure 10.73 TinySwitch-based, 5 V, 1 A, 5 W power supply.

variable resistor connected to the TL431. This changes the programmable reference voltage that is subtracted from the output voltage before it is fed back to the controller.

10.7.1 Experimental Results

10.7.1.1 Waveforms

Figure 10.74 shows the voltage waveform measured at the drain of the TinySwitch, which is a typical waveform of a flyback converter. The overshoot of 75 V is clamped by the snubber circuit. The average value is 165 V. Figure 10.75 shows the measured output voltage ripple waveform. The amplitude is $1.13V_{pp}$.

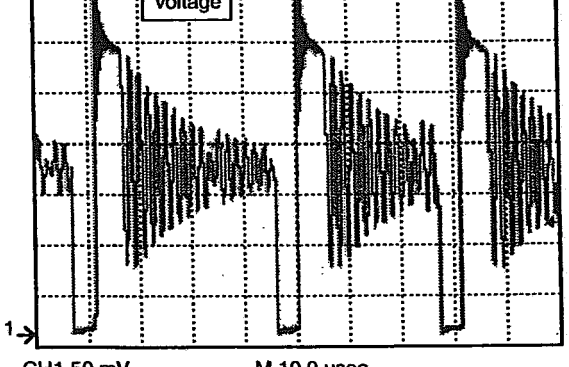

Figure 10.74 Drain voltage waveform of the TinySwitch-based converter.

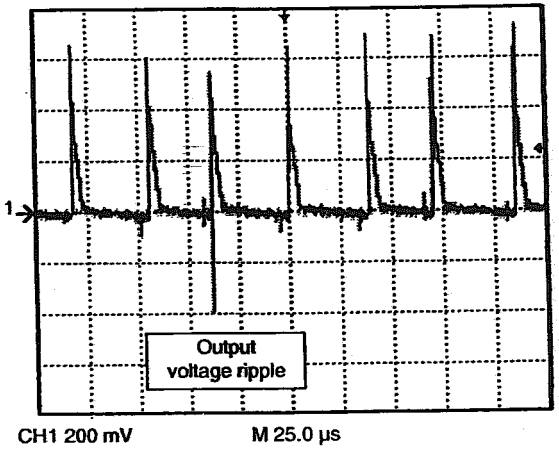

Figure 10.75 Output voltage ripple of the TinySwitch-based converter.

To evaluate the transient response of the converter, the load was changed from 10 to 5 Ω. Figure 10.76 shows the output voltage and current waveforms of the TinySwitch-based converter during the load transient. As the current increases, the switching frequency also increases to improve regulation. The controller recovers after one switching cycle. The average output voltage after the load transient is slightly smaller than that before the transient.

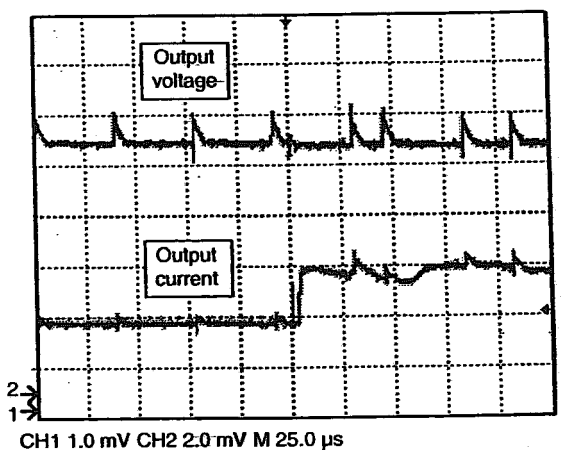

Figure 10.76 Output voltage and current of the TinySwitch-based converter during a load transient.

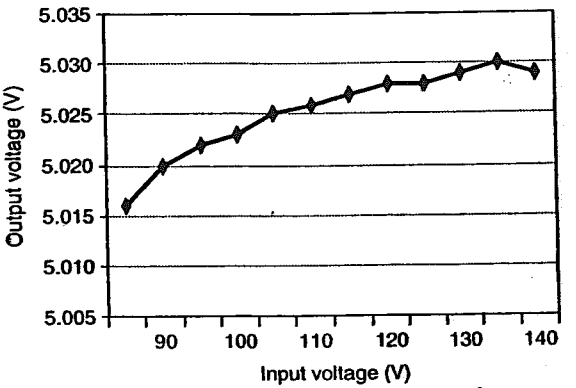

Figure 10.77 Line regulation of the TinySwitch-based converter.

10.7.1.2 Line Regulation

The line regulation was evaluated using a constant load resistance of 10 Ω. As can be seen from the measurements shown in Figure 10.77, the line regulation is excellent, i.e., better than 1%.

10.7.1.3 Load Regulation

The load regulation was evaluated using a constant input voltage of $110V_{ac}$. The measurement results are shown in Figure 10.78. As can be seen, the load regulation is within the 3% specification.

10.8 SWITCHING AUDIO AMPLIFIER

A different application of switching converters is described in this section. PWM switching audio amplifiers are more efficient than their class AB counterparts since their switching transistors are operating either in the saturation region or in the cutoff region. Output transistors in class AB audio amplifiers continuously dissipate power since they are operating in the active mode. Power dissipation in switching audio amplifier is a function of the transistor saturation voltage, its switching time, and parasitic resistances of the output filter. Distortion in switching audio amplifier is a function of the switching frequency, among other parameters. The switching frequency has to be at least one order of magnitude higher than the audio signal frequency to avoid overlapping sidebands in the PWM signal. On the

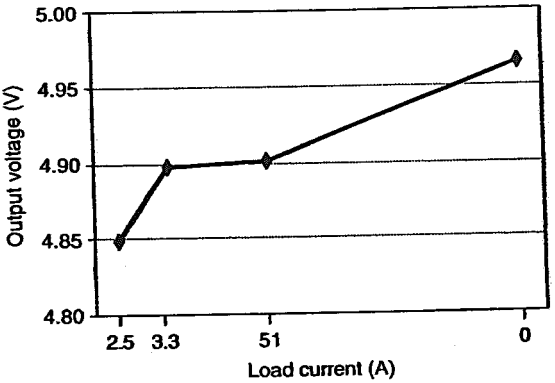

Figure 10.78 Load regulation of the TinySwitch-based converter.

other hand, distortion in class AB audio amplifier depends on the linearity of the current–voltage characteristics of the output transistors.

Figure 10.79 shows a block diagram of a basic pulse-width-modulated (PWM) switching audio amplifier. An equivalent ABM implementation in PSpice is shown in Figure 10.80. As shown, there are three main parts to a PWM switching audio amplifier. The front-end is the pre-amplifier that

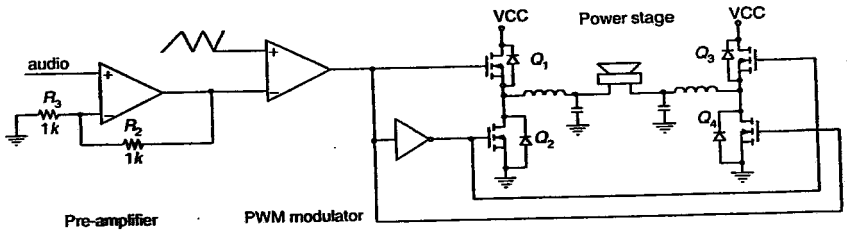

Figure 10.79 Basic block diagram of a PWM switching audio amplifier.

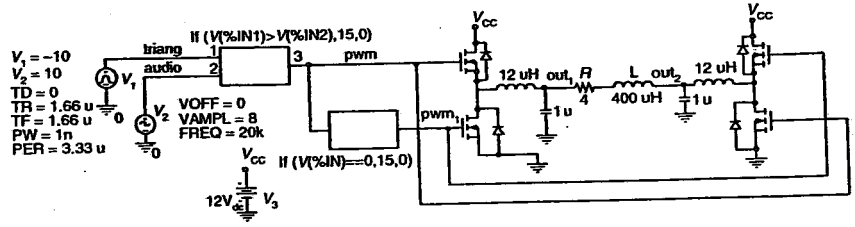

Figure 10.80 ABM schematic of a Class-D amplifier.

conditions the signal level to be compatible with the next stage. In a closed-loop configuration, the pre-amplifier may be used as the error amplifier. Any compensation for the feedback loop can be added to this stage. The output of the error amplifier is fed to a comparator that compares the error signal to a fixed-frequency sawtooth or triangular signal to achieve pulse-width modulation. The on-time of the pulse is proportional to the amplitude of the input signal. In other words, when the amplitude of the input signal is greater than the mean value of the repetitive signal, the on-time will be greater than the off-time. Conversely, if the amplitude of the input signal is less than the mean value of the repetitive signal, then the on-time will be less than the off-time. Also, if no signal is applied, the on-time will be equal to the off-time. In the case of a sinusoidal input, the duty cycle is greater than 50% when the sinusoidal is positive going, and increases with the amplitude. Likewise, when the sinusoidal signal is negative, the duty cycle is less than 50%, as shown in Figure 10.81. If there is no input signal, the duty cycle is 50% giving a net output of zero volt.

The load is an inductive speaker, represented by the inductor in series with the resistor. The speaker is connected between the differential outputs of the power stage. The output stage consists of two symmetrical halves, usually called half-bridge configuration. Each half-bridge is actually a synchronous buck converter. The topology formed by the two half-bridges is also known as a full bridge configuration. When the reference signal applied

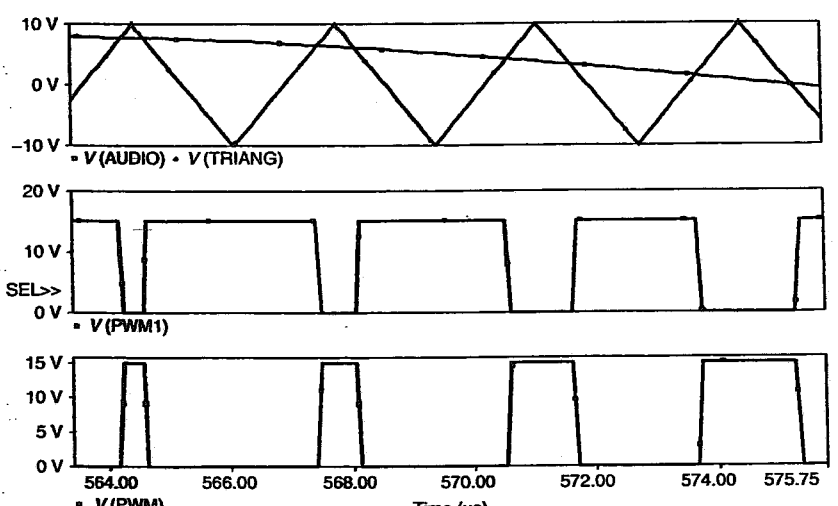

Figure 10.81 Input and output waveforms of the PWM modulator.

to the PWM modulator is an audio signal instead of a DC value (as it is used for a DC–DC converter), then the output voltage will track the variations of the reference audio signal achieving power amplification. The switching converter is said to work in the inverter mode. This type of switching audio amplifier is classified as a class-D amplifier.

In the full-bridge topology shown in Figure 10.79, Q_1 and Q_4 conduct during positive output voltages and Q_2 and Q_3 conduct during negative output voltages. For the case of a sinusoidal input, Q_1 and Q_4 conduct for longer portions of each switching period during the positive part of the sinusoidal input than Q_2 and Q_3. Likewise, for the negative portion of the sinusoidal, Q_2 and Q_3 conduct for a longer part of each switching period. It should be noted that Q_1 and Q_2, or Q_3 and Q_4, must never be switched on at the same time. Otherwise, a catastrophic "shoot-through" failure of the output transistors will occur. To avoid this situation, a dead time is introduced between the turn-off of one transistor and the turn-on of the other transistor on the same leg. Figure 10.82 shows the PSpice model for a dead time generator. The circuit accepts a PWM input and it generates the appropriate signals to drive the two MOSFETs on the same leg by adding a 180° phase shift and a 50 ns dead time between the turn-off of one transistor and the turn-on of the other. The dead time is programmable by changing the time parameter in the delay block. The circuit of Figure 10.82 also provides driver capabilities for the MOSFETs by amplifying the TTL output voltage levels of the logic gates up to 15 V and providing floating output voltages to connect to the gate and source of the MOSFETs. The connectors, gate1_Hi, and gate1_Lo, should be connected to the upper MOSFET's gate and source pins, respectively. The connectors, gate2_Hi and gate2_Lo, should be connected to the lower MOSFET's gate and source pins, respectively.

The high-frequency PWM train fed to the four transistors is amplified to the voltage rails of the power supply. The low-frequency component of

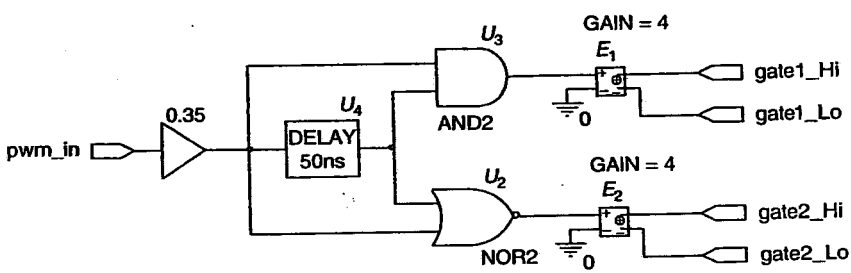

Figure 10.82 PSpice schematic of a dead time generator.

the amplified pulse train, namely the input signal, is usually recovered at an amplified state by a low-pass filter formed by L_o and C_o. The values for L_o and C_o are chosen such that the corner frequency is slightly above the upper audio range of 20 kHz. However, the low-pass filter increases the cost of the amplifier and introduces distortion due to nonlinearities of the components. A reduced bandwidth, known as phase distortion, is another important source of distortion.

The switching frequency in an open-loop PWM switching audio amplifier is normally chosen to be at least two decades above the corner frequency of the output filter to reduce output switching ripple. Since the highest audible frequency is 20 kHz, the switching frequency should be at least 2 MHz to avoid excessive output switching ripple. Fortunately, negative feedback can be used to reduce the switching frequency. The corner frequency of the output filter can be reduced to 2 kHz. Negative feedback is then used to extend the closed-loop gain bandwidth to 20 kHz. Thus, a switching frequency of 200 kHz is sufficient to obtain a low output-switching ripple. The use of negative feedback also renders the switching audio amplifier less sensitive to noise introduced by the power supply and nonideality of the sawtooth signal.

The input and output voltage waveforms obtained from the circuit of Figure 10.80 are shown in Figure 10.83 for a 20 kHz input signal. The output

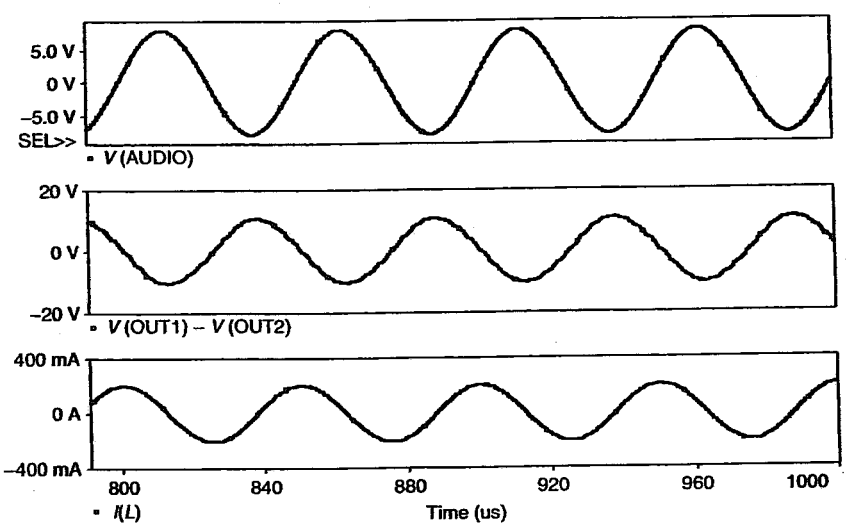

Figure 10.83 Input and output waveforms of the open-loop Class-D amplifier with an output low-pass filter.

voltage waveform is 180° out-of-phase with respect to the input voltage waveform and some distortions can be clearly seen. However, the output current waveform is smoother due to the filtering effect of the speaker inductance. Notice that the ripple present in the output waveforms corresponds to the switching frequency, which is much higher than the audio signal frequency.

10.8.1 Case Study

A PWM switching audio amplifier was designed for automotive applications with a nominal 12-V supply. The maximum output power was specified at 18 W for a 4 Ω and 400 μH speaker. The maximum output power can be readily increased by increasing the magnitude of the supply voltage. Also, the output ripple was minimized so that its total harmonic distortion (THD) was less than 0.05%. The number of components was kept to a minimum without sacrificing performance. A low-pass output filter was not used in this design; instead, the distortion in the output waveform was minimized by using negative feedback. Three nested feedback loops accomplish this task. Ultimately, the entire amplifier can be integrated into a single-chip integrated circuit. Figure 10.84 shows the block diagram of the multi-loop PWM switching audio amplifier. Starting with the inner loop, each loop was designed with the aid of PSpice simulations. A linear model was used to calculate the phase compensation of each loop. The phase shift due to the time delay at the crossover frequency of the loop gain was calculated and added to the unity-gain phase to obtain the phase margin. This procedure gives a good approximation if a close estimation of the time delay can be made. Once the frequency compensation is calculated, the results can be checked using time-domain simulations.

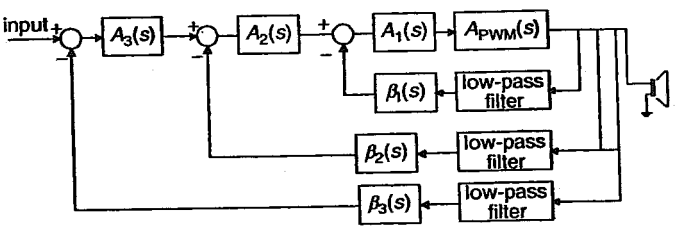

Figure 10.84 Block diagram representation of the multiloop amplifier. (From Figure 3 of Oliva, A.R., Ang, S.S., Vo, T.V., A multi-loop voltage feedback filterless Class-D switching audio amplifier using unipolar pulse-width-modulation, *IEEE Trans. on Consumer Electronics*, Vol. 50, No. 1, February 2004, pp. 312–319. With permission.)

10.8.1.1 The Output Stage

An H-bridge configuration was chosen for the output stage because the switching amplifier must exhibit two-quadrant operation and have bi-directional current flow with respect to the load. The H-bridge configuration also allows the use of a single supply voltage for the output stage. HIP2060AS2 power MOSFETs in surface-mount packaging were chosen for their high switching speeds and simpler drive requirements compared to their bipolar counterparts. Using less expensive *n*-channel devices also eliminates the need for matched devices thereby minimizing cost. To turn on the high-side power MOSFET, a gate voltage higher than the drain voltage is needed. Since the drain voltage of the high-side power MOSFET is equal to the supply voltage, an International Rectifiers' IR2110 high-voltage MOS gate driver with independent high-side and low-side driving capabilities was used.

The gate drive requirement for the high-side power MOSFET is achieved via a bootstrap technique using an external capacitor and a charging diode. The value of the bootstrap capacitor is dictated by the gate charge requirements, switching frequency, and duty cycle. Once the turn-on charge has been delivered to the gate of the power MOSFET, a minimum gate voltage must be maintained during the entire conduction period. The current drawn from the bootstrap capacitor, I_{QBS}, is equal to the quiescent current of the high-side channel of the IR2110. The minimum bootstrap capacitance, C_B, is given as [9]

$$C_B \geq \frac{2I_{QBS}t_{on}}{(V_{cc} - 1.5 - 10)}, \tag{10.95}$$

where a voltage drop of 1.5 V on the charging path of the bootstrap capacitor and a voltage drop due to the internal leakage, equal to half the excess gate voltage is assumed. Assuming a quiescent current of 100 μA, a switching frequency of 300 kHz with a maximum duty cycle of 90%, and a supply voltage of 12 V, gives a minimum value of 0.6 nF for the bootstrap capacitor. A very conservative value of 0.1 μF was chosen for the bootstrap capacitor. A 1N4153 fast-switching diode, with a voltage rating of 75 V and a reverse recovery time of 2 ns, was chosen for the charging diode. To help reduce noise, and supply the transient current needed for switching the capacitive loads, bypass capacitors between V_{CC} and common, and V_{DD} and V_{SS} pins in the IR2110 were used. All bypass capacitors, including the reservoir capacitors, should be connected as close to the IR2110 as possible. A 0.1 μF ceramic disk capacitor in parallel with a 1 μF tantalum capacitor is recommended for V_{CC} bypass [9].

The reconstruction of the original signal was accomplished without a low-pass filter. The combined action of the three feedback loops and the inductive speaker was sufficient to achieve a high-fidelity (hi-fi) THD level. However, this topology is restricted for those applications where the amplifier can be kept close to the voice coil in a shielded environment, like in shielded powered speakers, to maintain EMI within admissible levels.

As with any switching converter, a certain amount of output switching ripple will be associated with the switching frequency. The higher the switching frequency, the lower is the output ripple. As a general rule, the switching frequency must be at least two decades above the upper frequency of the audio band. For audio applications, the upper frequency must be at least 200 kHz to provide a flat frequency response out to 20 kHz. Thus, the switching frequency was chosen at 300 kHz as a trade-off between the distortions that would be introduced by the dead time and the attenuations of the aliased frequency components. Another drawback of a very high switching frequency is that the linearity of the sawtooth waveform becomes hard to maintain, which adds additional distortion to the output. Such problems can be mitigated by using negative feedback.

10.8.1.2 The Error Amplifier

The error amplifier of each feedback loop is a TLE2082 operational amplifier configured into a differential amplifier, as shown in Figure 10.85. A high slew rate amplifier is required because the error signal has very fast transients due to the absence of an output low-pass filter. Since a triangular carrier waveform of -5 to 5 V peak-to-peak is used, no offset voltage is needed to yield a duty cycle of 50% when there is no input signal. The stages following the error amplifier are used for phase compensation and to provide additional loop gain. A 330 μF input decoupling capacitor is connected in series with R_1 to eliminate any DC voltage that the signal source might otherwise introduce.

10.8.1.3 PWM Modulator

For the generation of the PWM waveforms, the unipolar-PWM modulator shown in Figure 10.86 was used. The input and output waveforms are shown in Figure 10.87. For the unipolar-PWM modulator, the triangular carrier is compared with the audio signal as well as the same signal shifted 180° to yield the unipolar-PWM signals. The main advantage of unipolar-PWM is that no spectral bins appear at the odd multiples of the switching frequency, and no multiples of the switching frequency are present. The first spectral bin that appears outside of the base-band corresponds to $2f_s - f_o$, as shown in Figure 10.88. This essentially doubles the switching frequency,

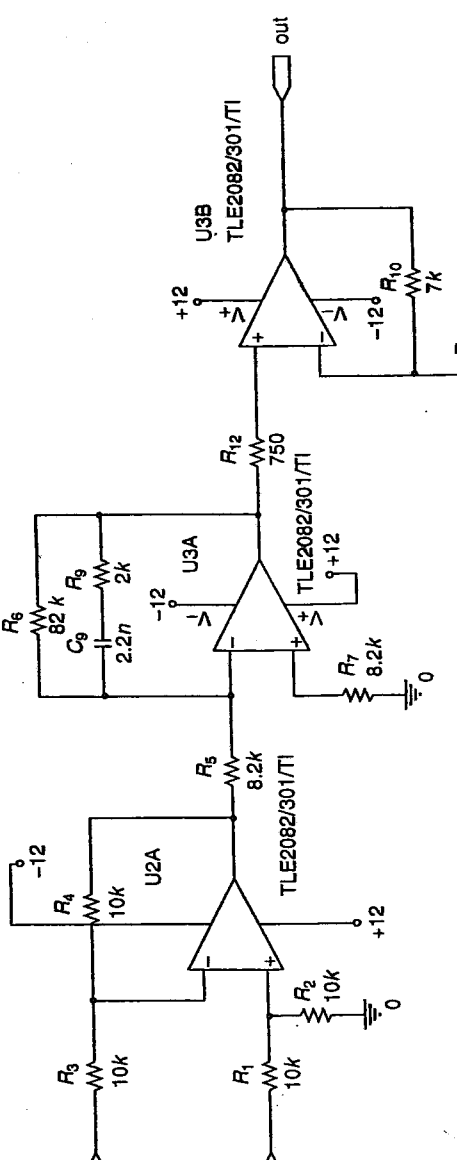

Figure 10.85 Error amplifier and phase compensation. (From Figure 16 of Oliva, A.R., Ang, S.S., Vo, T.V., A multi-loop voltage feedback filterless class-d switching audio amplifier using unipolar pulse-width-modulation, *IEEE Trans. on Consumer Electronics*, Vol. 50, No. 1, February 2004, pp. 312–319. With permission.)

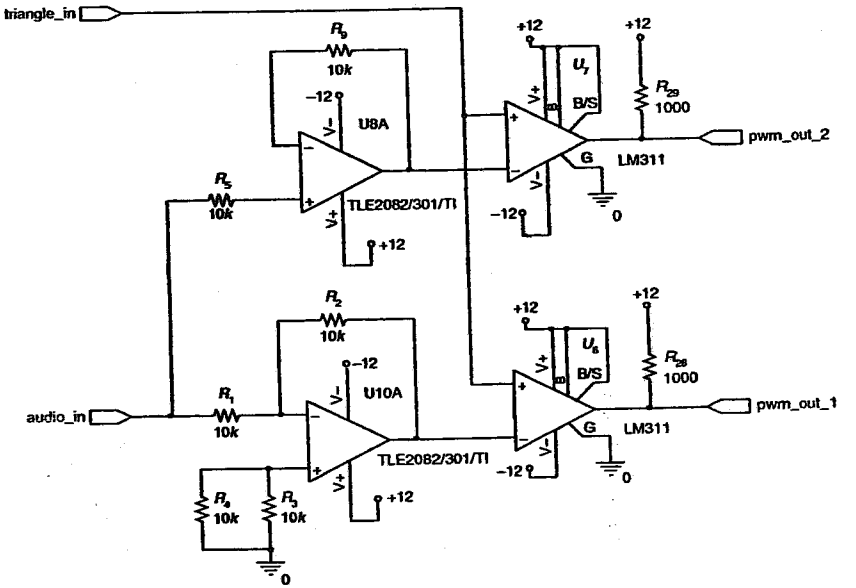

Figure 10.86 Schematic diagram of the unipolar-PWM modulator.

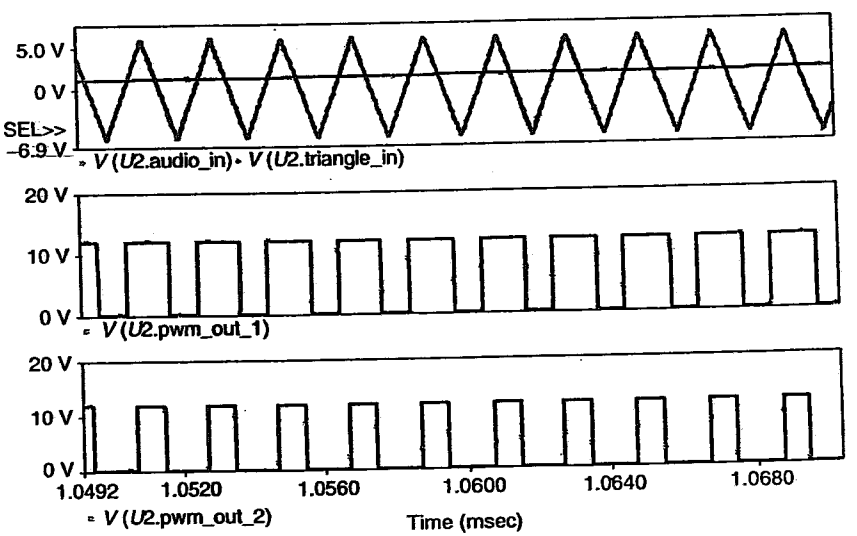

Figure 10.87 Input and output waveforms of the unipolar-PWM modulator.

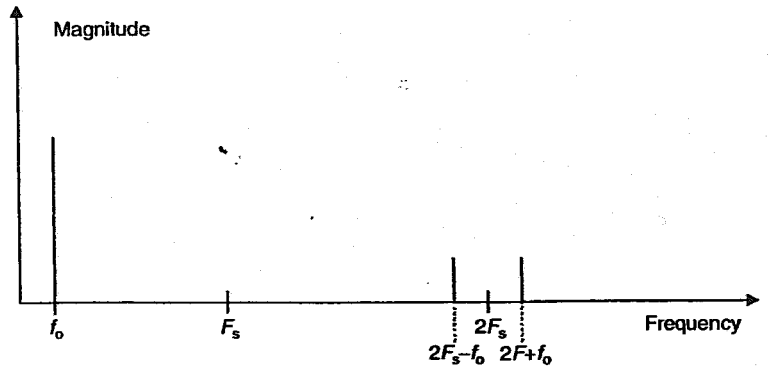

Figure 10.88 Frequency spectrum of unipolar PWM.

moving the unwanted frequency components far away from the audio band. A triangular carrier is preferred over a sawtooth carrier due to its lower harmonic contents.

10.8.1.4 The Feedback Loop

Because the speaker load in the H-bridge is floating so that neither side is referenced to ground, a differential amplifier must be used to sample the voltage across the load. Since there is no output filter, the voltage waveform at the load is a square wave. A low-pass filter was added at the input of the voltage-sensing amplifier to avoid slew rate distortion at this stage (Figure 10.89). This means that almost all unwanted upper frequency oscillations and distortion are attenuated by the filter. The gain of the differential amplifier is determined by resistors R_{13}, R_{14}, R_{15}, and R_{16} according to

$$V_{out} = (In_+ - In_-)\frac{R_{13}}{R_{16}} \tag{10.96}$$

with

$$\begin{aligned} R_{13} &= R_{14}, \\ R_{15} &= R_{16}. \end{aligned} \tag{10.97}$$

The voltage gain was selected as 1 V/V to avoid slew rate distortion.

10.8.1.5 Evaluation

The PWM switching audio amplifier was constructed on a double-sided printed-circuit board. All measurements were performed with a $\pm$ 12 V

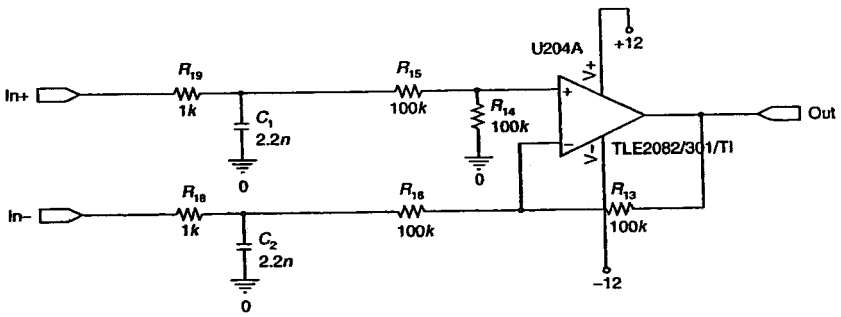

Figure 10.89 Voltage sensing amplifier.

supply for the signal stage and a +12 V supply for the output stage. THD+N characteristics were characterized using an Audio Precision System One® Audio analyzer. Audio standards establish that the measurements of the hi-fi parameters of the audio amplifiers have to be performed within the audio band. As such, an active LPF with the required characteristics[1] was connected in parallel with the load and measurements were taken at this output. All voltage and current measurements were performed using a Tektronix TDS540 oscilloscope and an AM503A current probe. A quiescent current of less than 10 mA was measured at a 50% duty cycle or with no input signal for the output stage.

10.8.1.5.1 Open-loop response. The THD+N versus frequency response of the open-loop amplifier is shown in Figure 10.90. The distortion is below 0.7% up to 1 kHz and increases after this frequency.

10.8.1.5.2 Closed-loop response. The simulated and measured closed-loop frequency responses are shown in Figure 10.91 and Figure 10.92, respectively. The measurements were taken using a fourth-order low-pass filter having a corner frequency at 30 kHz. The simulation results show a flat magnitude response up to 100 kHz and a flat phase response up to 20 kHz, which is in good agreement with the calculations. However, the measured frequency response is flat up to 20 kHz and then decreases very rapidly due to the influence of the low-pass filter used for the measurements.

10.8.1.5.3 Total harmonic distortion plus noise analysis. Figure 10.93 to Figure 10.95 show the THD+N analysis for the closed-loop amplifier

[1] Pass-band response deviation: $\leq \pm 0.1$ dB for 10 Hz $\leq f \leq$ 20 kHz; stop-band attenuation: >60 dB for f >24 kHz.

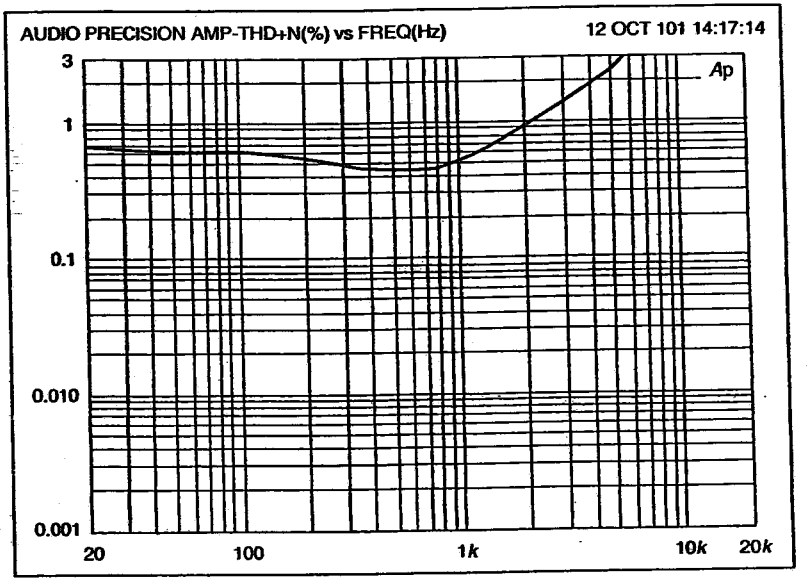

Figure 10.90 THD+N versus frequency for the open-loop amplifier. (From Figure 11 of Oliva, A.R., Ang, S.S., Vo, T.V., A multi-loop voltage feedback filterless Class-D switching audio amplifier using unipolar pulse-width-modulation, *IEEE Trans. on Consumer Electronics*, Vol. 50, No. 1, February 2004, pp. 312–319. With permission.)

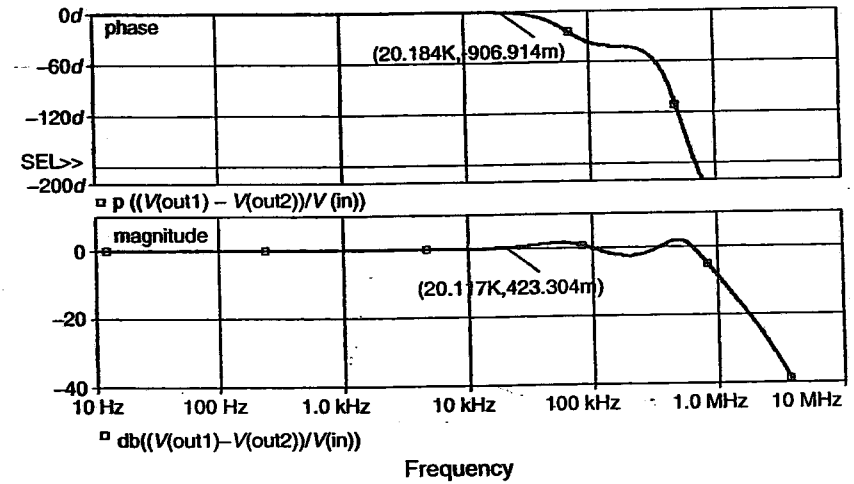

Figure 10.91 Simulated closed-loop frequency response.

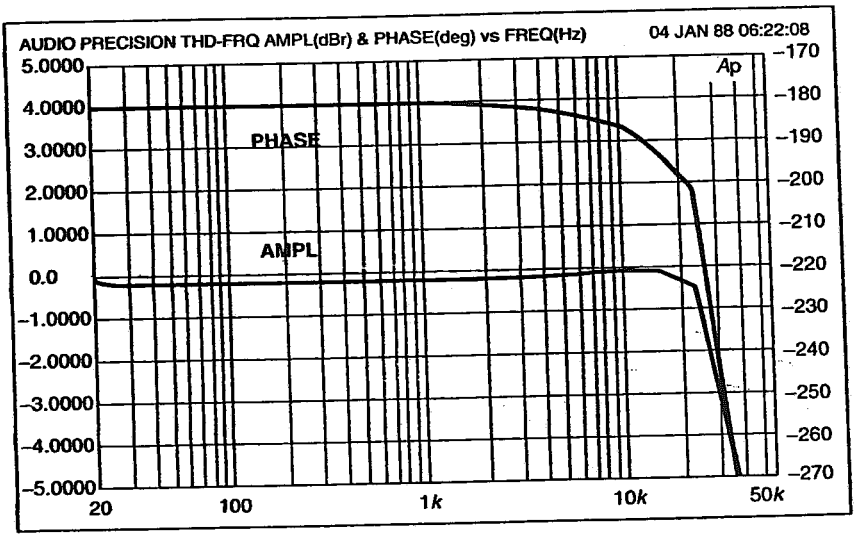

Figure 10.92 Measured closed-loop frequency response. (From Figure 9 of Oliva, A.R., Ang, S.S., Vo, T.V., A multi-loop voltage feedback filterless Class-D switching audio amplifier using unipolar pulse-width-modulation, *IEEE Trans. on Consumer Electronics*, Vol. 50, No. 1, February 2004, pp. 312–319. With permission.)

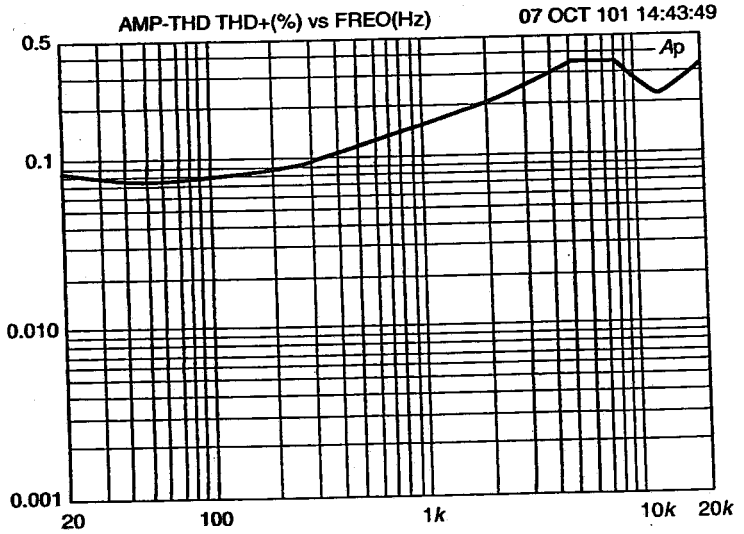

Figure 10.93 THD+N versus frequency for one loop feedback. (From Figure 12 of Oliva, A.R., Ang, S.S., Vo, T.V., A multi-loop voltage feedback filterless Class-D switching audio amplifier using unipolar pulse-width-modulation, *IEEE Trans. on Consumer Electronics*, Vol. 50, No. 1, February 2004, pp. 312–319. With permission.)

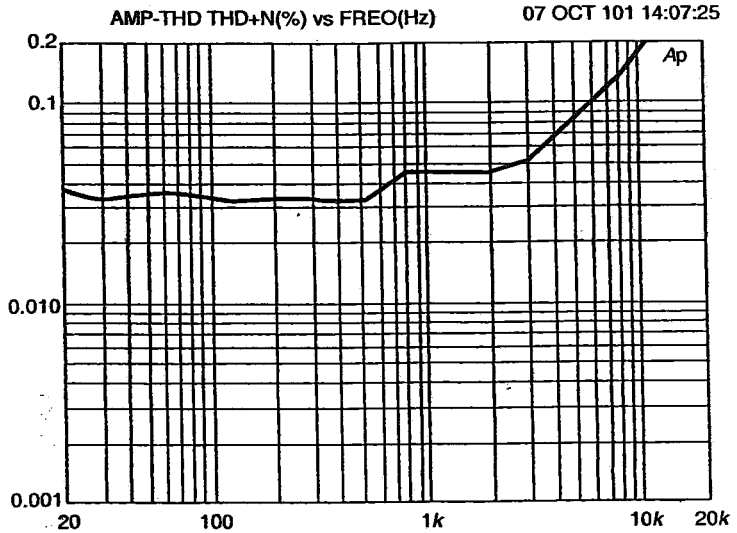

Figure 10.94 THD+N versus frequency for two feedback loops. (From Figure 13 of Oliva, A.R., Ang, S.S., Vo, T.V., A multi-loop voltage feedback filterless Class-D switching audio amplifier using unipolar pulse-width-modulation, *IEEE Trans. on Consumer Electronics*, Vol. 50, No. 1, February 2004, pp. 312–319. With permission.)

when one, two, and three feedback loops are closed, respectively. The measurements were taken using a 1 kHz 10 V_{pp} sinusoidal input. Notice that the curves are fairly flat up to 1 kHz but they start to increase after this frequency. Also, notice that every time a loop is added, the distortion reduces. As can be seen, there is not much of an improvement in THD+N in going from the two-loop configuration to the three-loop configuration. We attribute this to the background noise and the influence of the low-pass filter used to make these measurements, which has a THD of 0.008% in the audio band.

10.8.1.5.4 Input and output waveforms. Figure 10.96 shows the input audio signal and output current waveform across the speaker load for a frequency of 1 kHz. As can be seen, there is a phase shift of 43° between the input voltage and output current signals due to the inductive nature of the speaker. The output-switching ripple is barely visible on the output current waveform. It should be noted that an increase in the audio input signal increases the amplitudes of both the output voltage and output current, with a concomitant increase in output power.

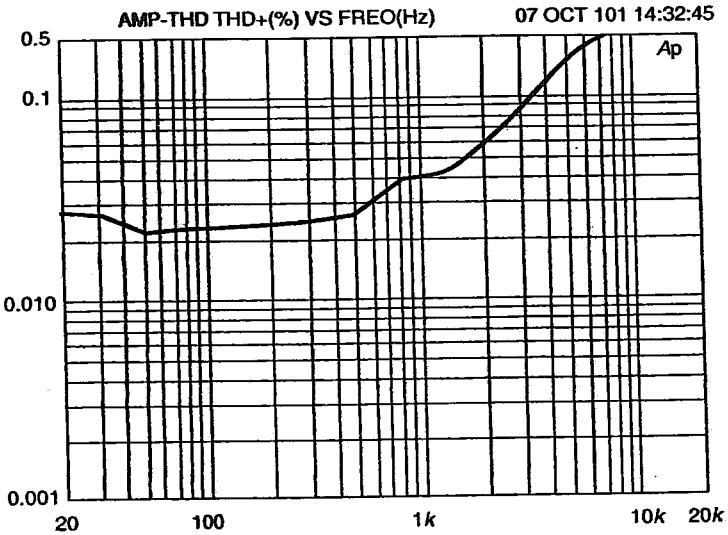

Figure 10.95 THD+N versus frequency for three feedback loops. (From Figure 14 of Oliva, A.R., Ang, S.S., Vo, T.V.,A multi-loop voltage feedback filterless Class-D switching audio amplifier using unipolar pulse-width-modulation, *IEEE Trans. on Consumer Electronics*, Vol. 50, No. 1, February 2004, pp. 312–319. With permission.)

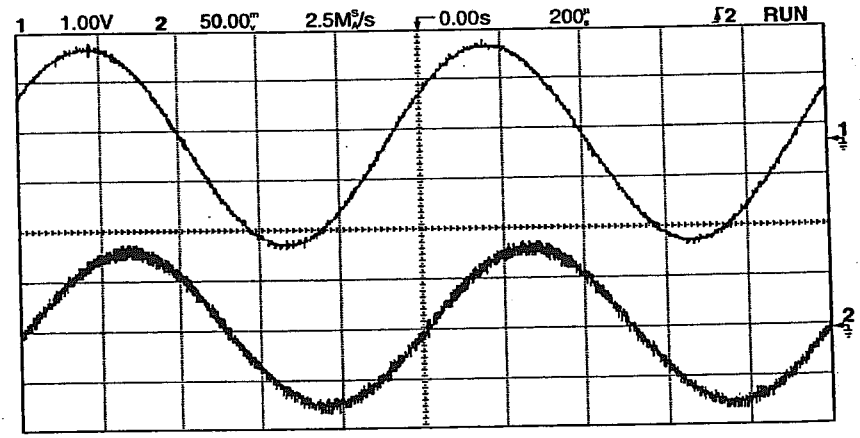

Figure 10.96 Input voltage and output current waveforms.

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