

DATA SHEET

TDA1308; TDA1308A Class AB stereo headphone driver

Product specification
Supersedes data of 2002 Feb 27

2002 Jul 19

Class AB stereo headphone driver

TDA1308; TDA1308A

FEATURES

- Wide temperature range
- No switch ON/OFF clicks
- Excellent power supply ripple rejection
- Low power consumption
- Short-circuit resistant
- High performance
 - high signal-to-noise ratio
 - high slew rate
 - low distortion
- Large output voltage swing.

GENERAL DESCRIPTION

The TDA1308; TDA1308A is an integrated class AB stereo headphone driver contained in an SO8, DIP8 or a TSSOP8 plastic package. The device is fabricated in a 1 mm CMOS process and has been primarily developed for portable digital audio applications.

The difference between the TDA1308 and the TDA1308A is that the TDA1308A can be used at low supply voltages.

QUICK REFERENCE DATA

$V_{DD} = 5\text{ V}$; $V_{SS} = 0\text{ V}$; $T_{amb} = 25\text{ °C}$; $f_i = 1\text{ kHz}$; $R_L = 32\text{ }\Omega$; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DD}	supply voltage	TDA1308				
	single		3.0	5.0	7.0	V
	dual		1.5	2.5	3.5	V
	supply voltage	TDA1308A				
	single		2.4	5.0	7.0	V
	dual		1.2	2.5	3.5	V
V_{SS}	negative supply voltage		–1.5	–2.5	–3.5	V
I_{DD}	supply current	no load	–	3	5	mA
P_{tot}	total power dissipation	no load	–	15	25	mW
P_o	maximum output power	THD < 0.1%; note 1	–	60	–	mW
(THD + N)/S	total harmonic distortion plus noise-to-signal ratio	note 1				
			–	0.03	0.06	%
			–	–70	–65	dB
		$R_L = 5\text{ k}\Omega$; note 2	–	–92	–89	dB
		$R_L = 5\text{ k}\Omega$; note 3	–	–52	–40	dB
		$R_L = 5\text{ k}\Omega$	–	–101	–	dB
S/N	signal-to-noise ratio		100	110	–	dB
α_{CS}	channel separation		–	70	–	dB
		$R_L = 5\text{ k}\Omega$	–	105	–	dB
PSRR	power supply ripple rejection	$f_i = 100\text{ Hz}$; $V_{ripple(p-p)} = 100\text{ mV}$	–	90	–	dB
T_{amb}	ambient temperature		–40	–	+85	°C

Notes

1. $V_{DD} = 5\text{ V}$; $V_{O(p-p)} = 3.5\text{ V}$ (at 0 dB).
2. $V_{DD} = 2.4\text{ V}$; $V_{O(p-p)} = 1.62\text{ V}$ (at –4.8 dBV); for TDA1308A only.
3. $V_{DD} = 2.4\text{ V}$; $V_{O(p-p)} = 1.19\text{ V}$ (at –7.96 dBV); for TDA1308A only.

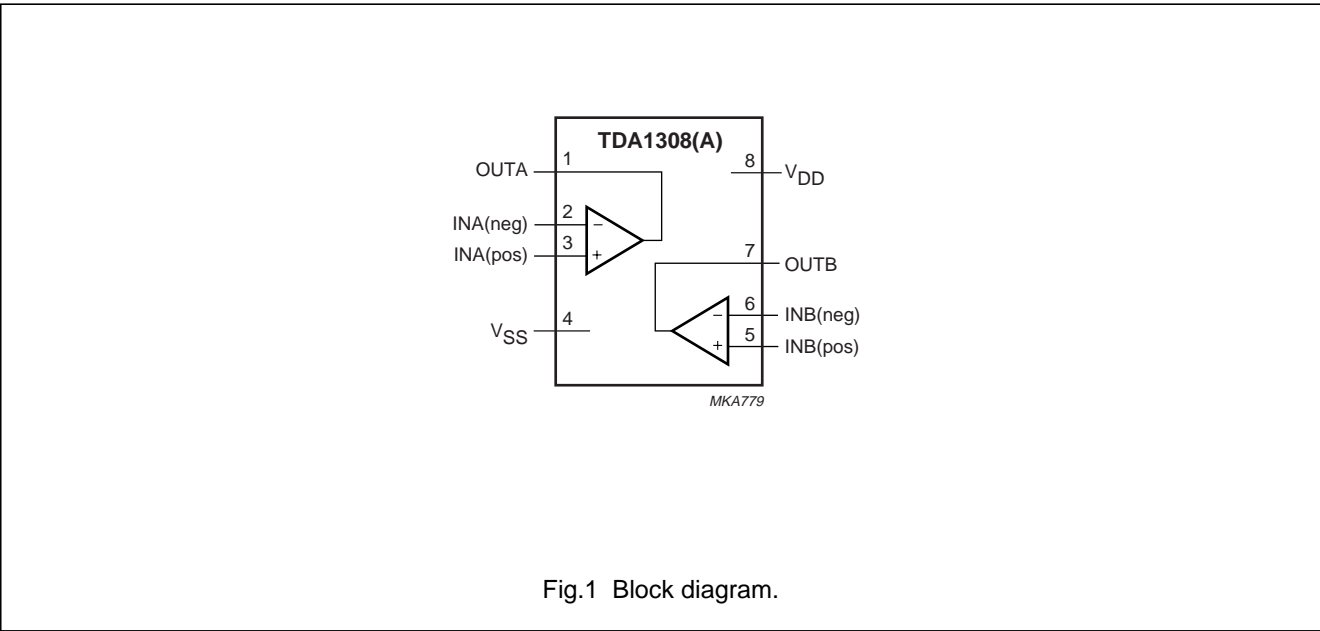
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ORDERING INFORMATION

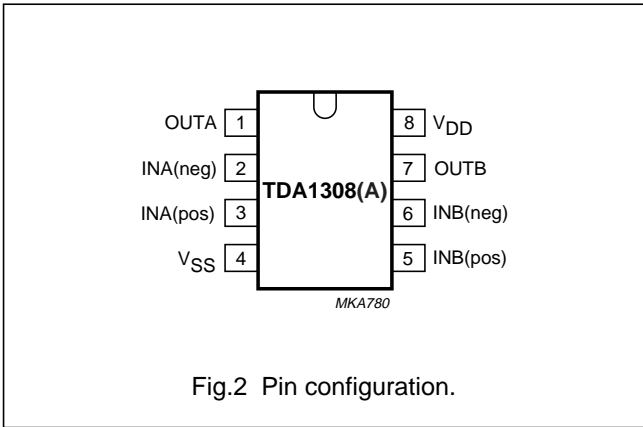
TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA1308	DIP8	plastic dual in-line package; 8 leads (300 mil)	SOT97-1
TDA1308T	SO8	plastic small outline package; 8 leads; body width 3.9 mm	SOT96-1
TDA1308AT	SO8	plastic small outline package; 8 leads; body width 3.9 mm	SOT96-1
TDA1308TT	TSSOP8	plastic thin shrink small outline package; 8 leads; body width 3 mm	SOT505-1

BLOCK DIAGRAM



PINNING

SYMBOL	PIN	DESCRIPTION
OUTA	1	output A
CD)	2	inverting input A
INA(pos)	3	non-inverting input A
VSS	4	negative supply
INB(pos)	5	non-inverting input B
INB(neg)	6	inverting input B
OUTB	7	output B
VDD	8	positive supply



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CHARACTERISTICS

$V_{DD} = 5\text{ V}$; $V_{SS} = 0\text{ V}$; $T_{amb} = 25\text{ °C}$; $f_i = 1\text{ kHz}$; $R_L = 32\text{ }\Omega$; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
V_{DD}	supply voltage single	TDA1308	3.0	5.0	7.0	V
			1.5	2.5	3.5	V
	supply voltage dual	TDA1308A	2.4	5.0	7.0	V
			1.2	2.5	3.5	V
V_{SS}	negative supply voltage		−1.5	−2.5	−3.5	V
I_{DD}	supply current	no load	–	3	5	mA
P_{tot}	total power dissipation	no load	–	15	25	mW
DC characteristics						
$V_{I(0s)}$	input offset voltage		–	10	–	mV
I_{bias}	input bias current		–	10	–	pA
V_{CM}	common mode voltage		0	–	3.5	V
G_V	open-loop voltage gain	$R_L = 5\text{ k}\Omega$	–	70	–	dB
I_O	maximum output current	$(THD + N)/S < 0.1\%$	–	60	–	mA
R_O	output resistance		–	0.25	–	Ω
V_O	output voltage swing	note 1	0.75	–	4.25	V
		$R_L = 16\text{ }\Omega$	1.5	–	3.5	V
		$R_L = 5\text{ k}\Omega$	0.1	–	4.9	V
PSRR	power supply rejection ratio	$f_i = 100\text{ Hz}$; $V_{ripple(p-p)} = 100\text{ mV}$	–	90	–	dB
α_{CS}	channel separation		–	70	–	dB
		$R_L = 5\text{ k}\Omega$	–	105	–	dB
C_L	load capacitance		–	–	200	pF
AC characteristics						
(THD + N)/S	total harmonic distortion plus noise-to-signal ratio	note 2	–	−70	−65	dB
			–	0.03	0.06	%
		note 3	–	−52	−40	dB
			–	0.25	1.0	%
		$R_L = 5\text{ k}\Omega$; note 2	–	−101	–	dB
			–	0.0009	–	%
S/N	signal-to-noise ratio		100	110	–	dB
f_G	unity gain frequency	open-loop; $R_L = 5\text{ k}\Omega$	–	5.5	–	MHz
P_o	maximum output power	$(THD + N)/S < 0.1\%$	–	60	–	mW
C_i	input capacitance		–	3	–	pF
SR	slew rate	unity gain inverting	–	5	–	V/ μ s
B	power bandwidth	unity gain inverting	–	20	–	kHz

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Notes

1. Values are proportional to V_{DD} ; $(THD + N)/S < 0.1\%$.
2. $V_{DD} = 5.0\text{ V}$; $V_{O(p-p)} = 3.5\text{ V}$ (at 0 dB).
3. $V_{DD} = 2.4\text{ V}$; $V_{O(p-p)} = 1.13\text{ V}$ (at -7.96 dBV); for TDA1308A only.

TEST AND APPLICATION INFORMATION

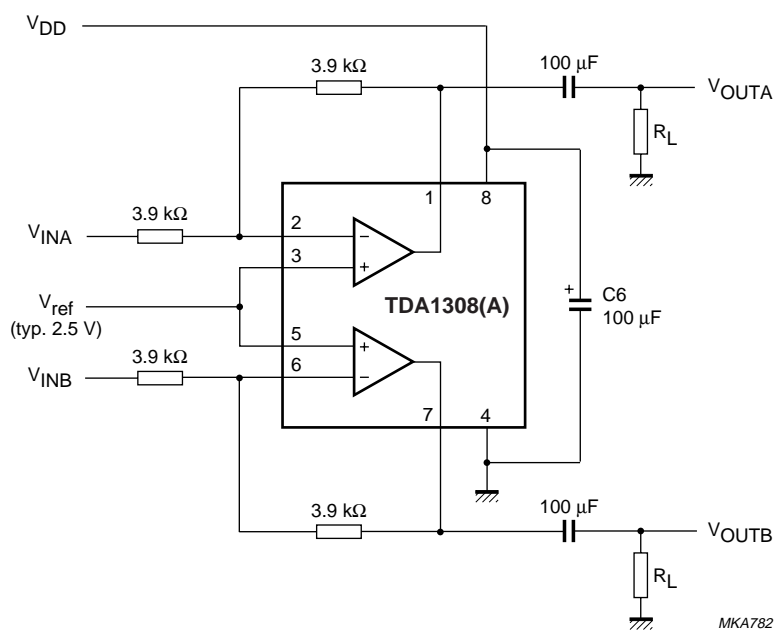
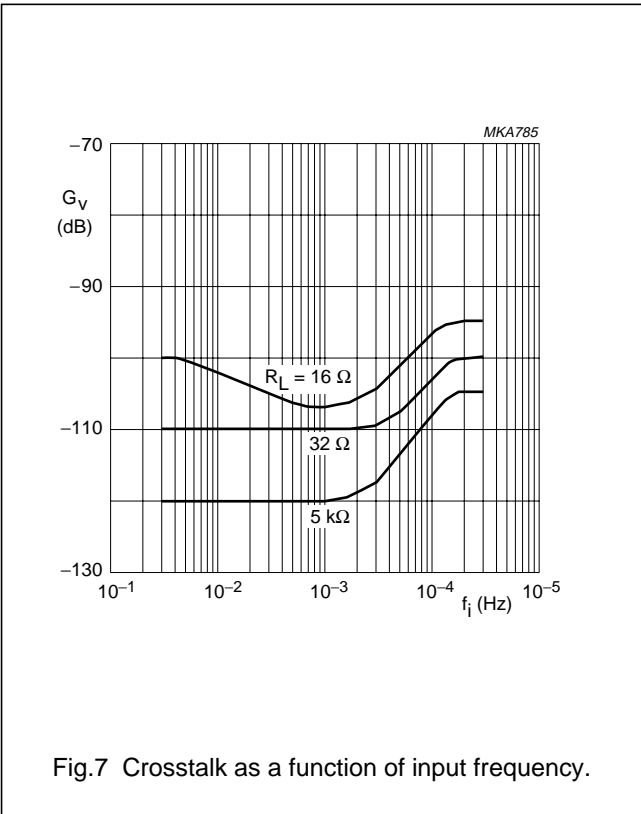
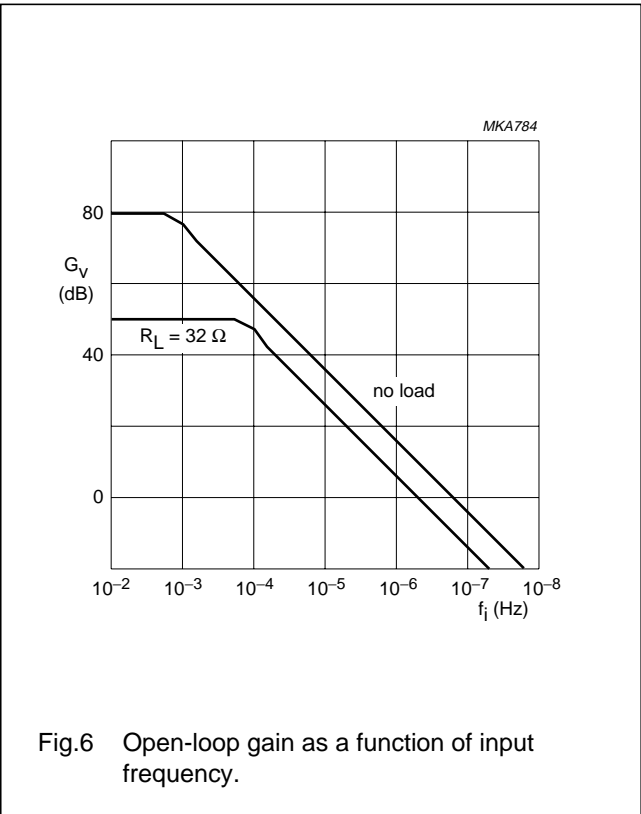
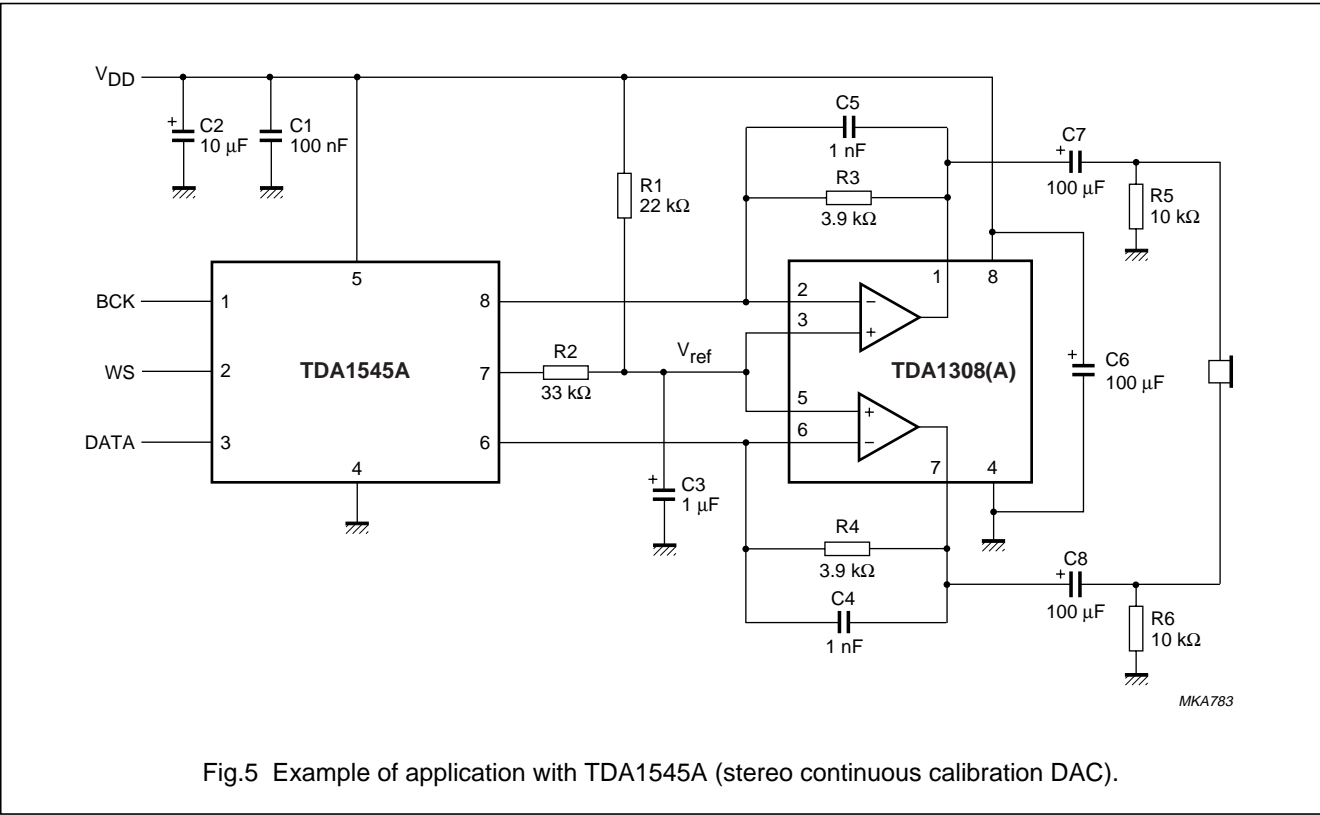


Fig.4 Measurement circuit for inverting application.

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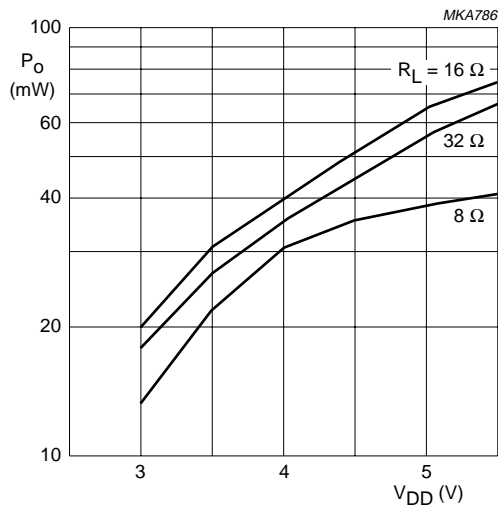


Fig.8 Output power as a function of supply voltage.

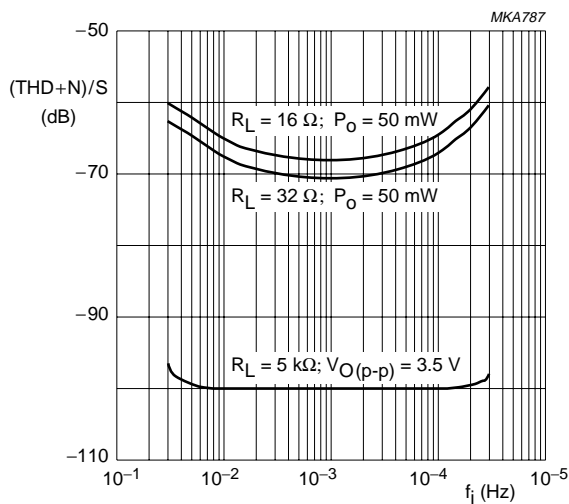


Fig.9 Total harmonic distortion plus noise-to-signal ratio as a function of input frequency.

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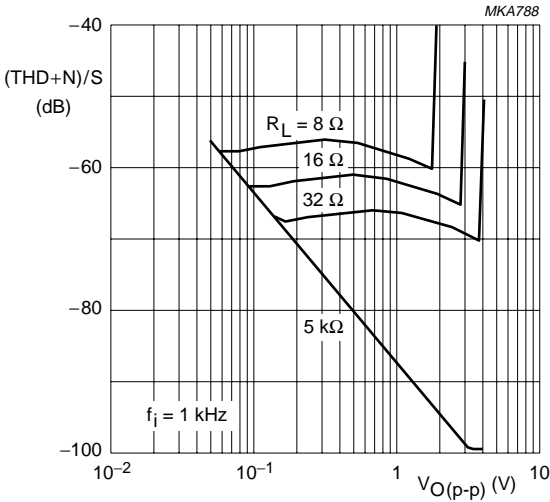


Fig.10 Total harmonic distortion plus noise-to-signal ratio as a function of output voltage level.

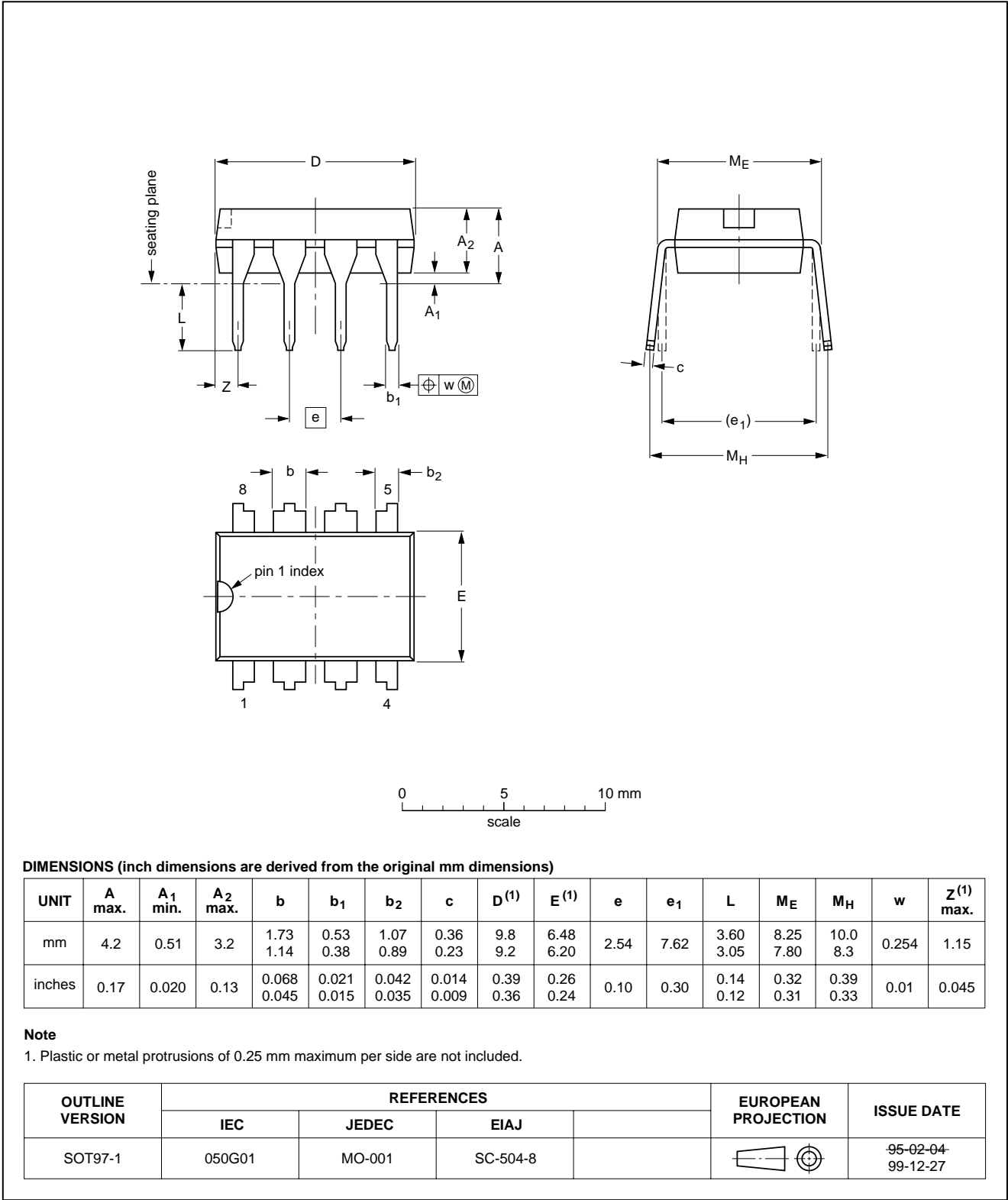
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PACKAGE OUTLINES

DIP8: plastic dual in-line package; 8 leads (300 mil)

SOT97-1

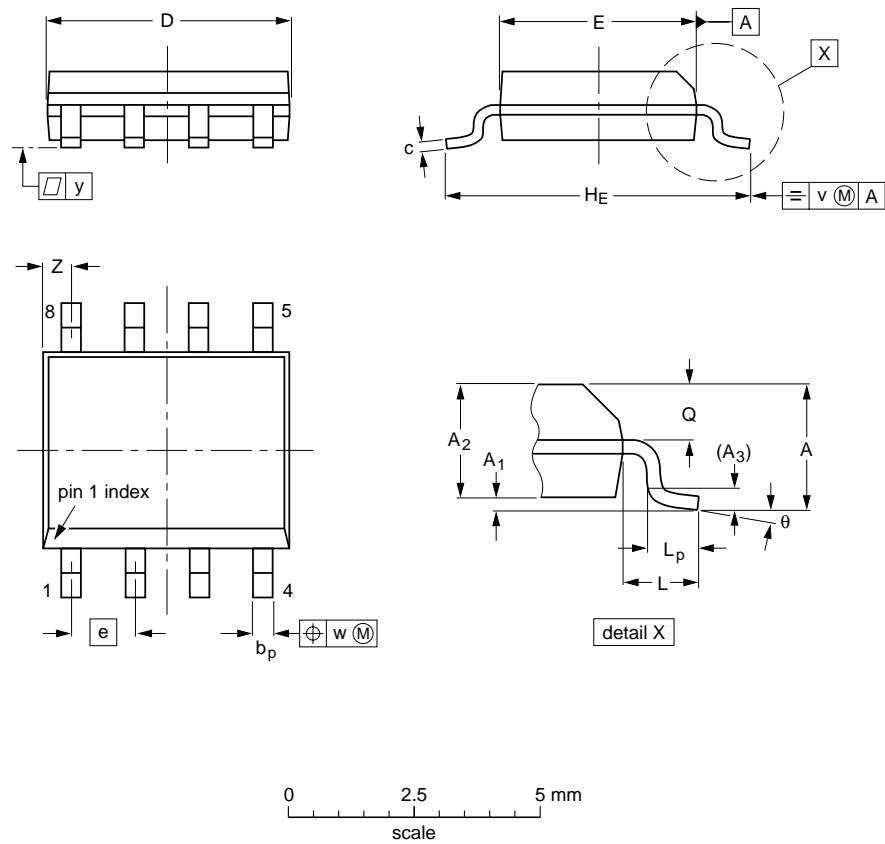


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SO8: plastic small outline package; 8 leads; body width 3.9 mm


SOT96-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽²⁾	e	H _E	L	L _p	Q	v	w	y	z ⁽¹⁾	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	5.0 4.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.20 0.19	0.16 0.15	0.050	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

- Notes
1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
 2. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

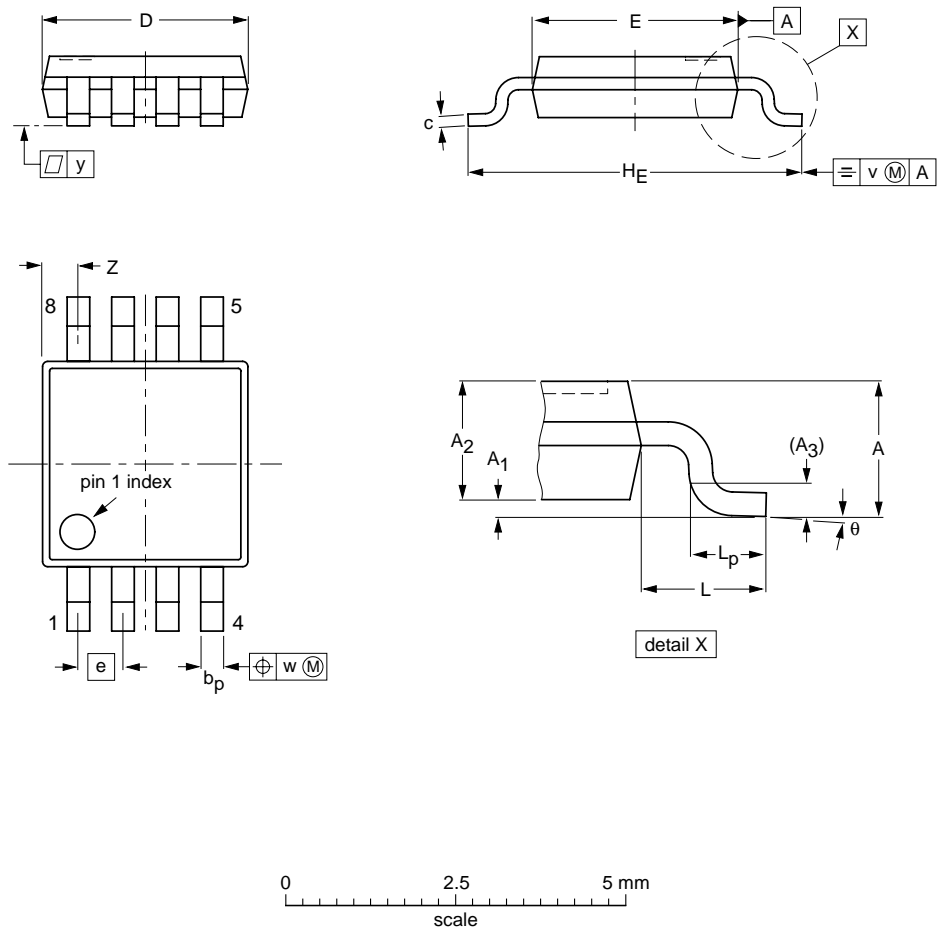
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT96-1	076E03	MS-012				97-05-22- 99-12-27

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TSSOP8: plastic thin shrink small outline package; 8 leads; body width 3 mm

SOT505-1



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽²⁾	e	H _E	L	L _p	v	w	y	z ⁽¹⁾	θ
mm	1.10	0.15 0.05	0.95 0.80	0.25	0.45 0.25	0.28 0.15	3.10 2.90	3.10 2.90	0.65	5.10 4.70	0.94	0.70 0.40	0.1	0.1	0.1	0.70 0.35	6° 0°

Notes

- 1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
- 2. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT505-1						99-04-09

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SOLDERING

Introduction

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (document order number 9398 652 90011).

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mount components are mixed on one printed-circuit board. Wave soldering can still be used for certain surface mount ICs, but it is not suitable for fine pitch SMDs. In these situations reflow soldering is recommended.

Through-hole mount packages

SOLDERING BY DIPPING OR BY SOLDER WAVE

The maximum permissible temperature of the solder is 260 °C; solder at this temperature must not be in contact with the joints for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified maximum storage temperature ($T_{\text{stg(max)}}$). If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

MANUAL SOLDERING

Apply the soldering iron (24 V or less) to the lead(s) of the package, either below the seating plane or not more than 2 mm above it. If the temperature of the soldering iron bit is less than 300 °C it may remain in contact for up to 10 seconds. If the bit temperature is between 300 and 400 °C, contact may be up to 5 seconds.

Surface mount packages

REFLOW SOLDERING

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, convection or convection/infrared heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 250 °C. The top-surface temperature of the packages should preferably be kept below 220 °C for thick/large packages, and below 235 °C for small/thin packages.

WAVE SOLDERING

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
 - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
 - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

The footprint must incorporate solder thieves at the downstream end.

- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

MANUAL SOLDERING

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

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Suitability of IC packages for wave, reflow and dipping soldering methods

MOUNTING	PACKAGE	SOLDERING METHOD		
		WAVE	REFLOW ⁽¹⁾	DIPPING
Through-hole mount	DBS, DIP, HDIP, SDIP, SIL	suitable ⁽²⁾	–	suitable
Surface mount	BGA, HBGA, LFBGA, SQFP, TFBGA	not suitable	suitable	–
	HBCC, HLQFP, HSQFP, HSOP, HTQFP, HTSSOP, HVQFN, SMS	not suitable ⁽³⁾	suitable	–
	PLCC ⁽⁴⁾ , SO, SOJ	suitable	suitable	–
	LQFP, QFP, TQFP	not recommended ⁽⁴⁾⁽⁵⁾	suitable	–
	SSOP, TSSOP, VSO	not recommended ⁽⁶⁾	suitable	–

Notes

1. All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the “*Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods*”.
2. For SDIP packages, the longitudinal axis must be parallel to the transport direction of the printed-circuit board.
3. These packages are not suitable for wave soldering as a solder joint between the printed-circuit board and heatsink (at bottom version) can not be achieved, and as solder may stick to the heatsink (on top version).
4. If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
5. Wave soldering is only suitable for LQFP, QFP and TQFP packages with a pitch (e) equal to or larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.
6. Wave soldering is only suitable for SSOP and TSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

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DATA SHEET STATUS

DATA SHEET STATUS ⁽¹⁾	PRODUCT STATUS ⁽²⁾	DEFINITIONS
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Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
Product data	Production	This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Changes will be communicated according to the Customer Product/Process Change Notification (CPCN) procedure SNW-SQ-650A.

Notes

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2. The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL <http://www.semiconductors.philips.com>.

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Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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Printed in The Netherlands

753503/03/pp16

Date of release: 2002 Jul 19

Document order number: 9397 750 09985

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